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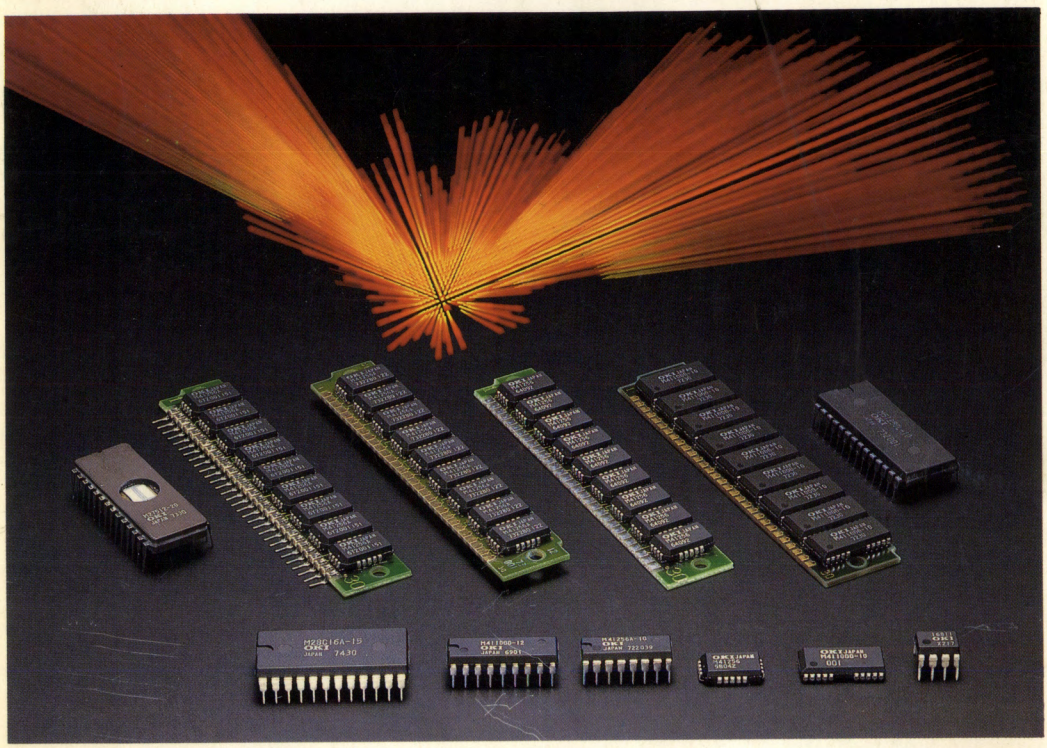
MEMORY DATA BOOK



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1 IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS

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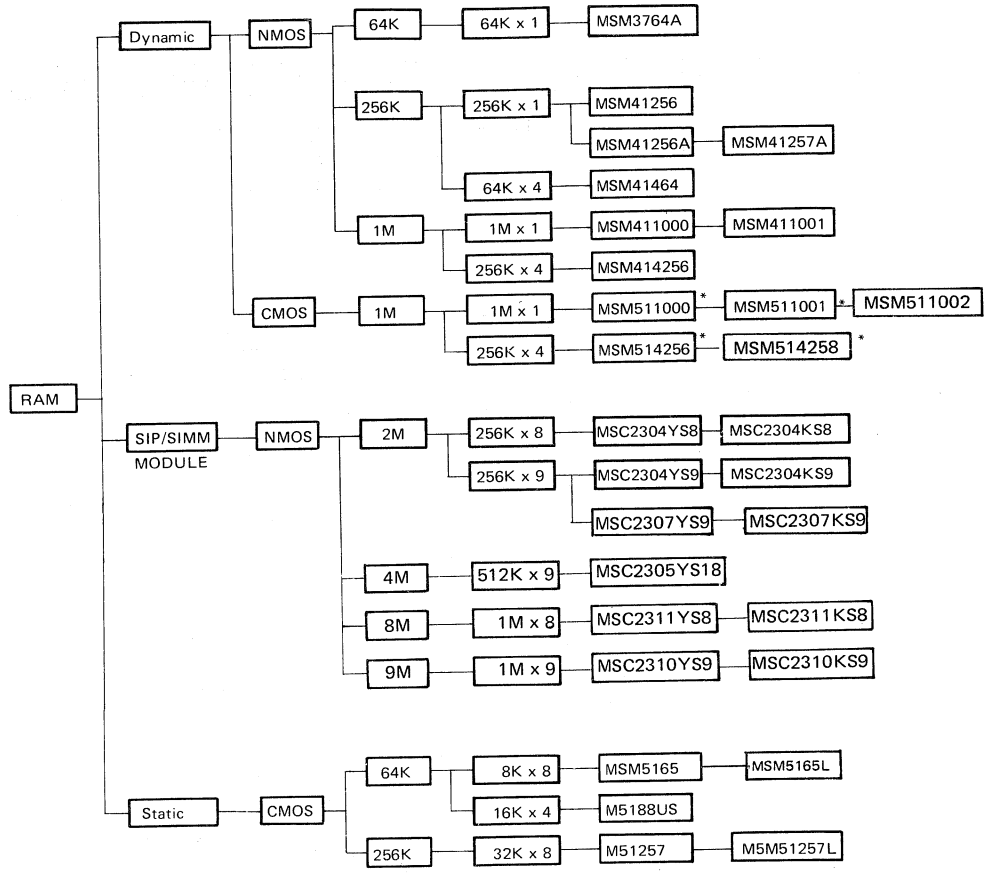
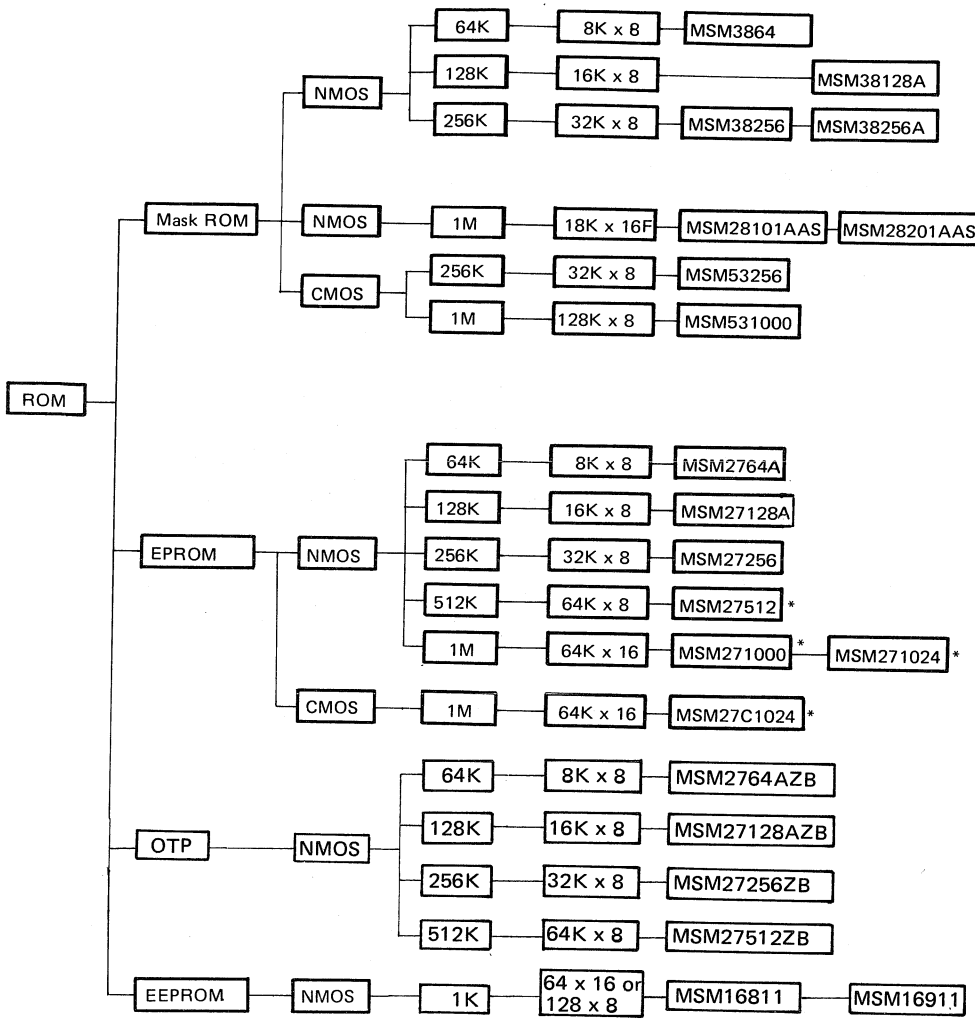
IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS



*Under development

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■



*Under development

• DYNAMIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3764A-12	64k	Dynamic	65,536x1	16	120	230	330/28	+5	
MSM3764A-15					150	260	330/28		
MSM3764A-20					200	330	330/28		
MSM41256-15	256k	Dynamic	262,144x1	16	150	260	385/28	+5	
MSM41256-20					200	330	385/28		
MSM41256A-10	250k	Dynamic	262,144x1	16	100	200	385/28	+5	
MSM41256A-12					120	220	385/28		
MSM41256A-15					150	260	385/28		
MSM41257A-10	256k	Dynamic	262,144x1	16	100	200	385/28	+5	
MSM41257A-12					120	220	385/28		
MSM41257A-15					150	260	385/28		
MSM41464-10	256k	Dynamic	65,536x4	18	100	200	385/28	+5	
MSM41464-12					120	230	385/28		
MSM41464-15					150	260	385/28		
MSM414256-10	256k	Dynamic	262,144x4	20	100	200	413/28	+5	
MSM414256-12					120	230	385/28		
MSM411000-10	1M	Dynamic	1,048,576x1	18	100	200	413/28	+5	
MSM411000-12					120	230	385/28		
MSM411001-10	1M	Dynamic	1,048,576x1	18	100	200	413/28	+5	
MSM411001-12					120	230	385/28		
MSM511000-10	1M	Dynamic	1,048,576x1	18	100	190	385/11	+5	
MSM511000-12					120	220	330/11		
MSM511001-10	1M	Dynamic	1,048,576x1	18	100	190	385/11	+5	
MSM511001-12					120	220	330/11		
MSM511002-10	1M	Dynamic	1048576x9	18	100	190	385/11	+5	
MSM511002-12					120	220	330/11		
MSM514256-10	1M	Dynamic	262,144x4	20	100	190	413/11	+5	
MSM514256-12					120	220	385/11		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM514258-10	1M	20 Pin Dynamic	262.144x4	20	100	190	413/11	+5	
MSM514258-12					120	220	385/11		

• SIP/SIMM MODULE

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (nw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSC2304-12YS8/KS8	2M	Socket Insertable Module	262144x8	30	120	120	—	+5	
MSC2304-15YS8/KS8					150	150	—		
MSC2304-12YS9/KS9	2M	Socket Insertable Module	262144x9	30	120	120	—	+5	
MSC2304-15YS9/KS9					150	150	—		
MSC2307-12YS9/KS9	2M	Socket Insertable Module	262144x9	30	120	120		+5	
MSC2307-15YS9/KS9					150	150			
MSC2305-12YS18A	4M	Socket Insertable Module	524288x9	30	120	120		+5	
MSC2305-15YS18A					150	150			
MSC2311-10YS8/KS8	8M	Socket Insertable Module	524288x9	30	100	100		+5	
MSC2311-12YS8/KS8					120	120			
MSC2310-10YS9/KS9	9M	Socket Insertable Module	1,048,576x1	30	100	200	—	+5	
MSC2310-12YS9/KS9					120	230	—		

• CMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM5165-12	64k	Fully Static Common I/O	8192x8	28	120	120	248/5.5	+5	
MSM5165-15					150	150	248/5.5		
MSM5165-20					200	200	248/5.5		
MSM5165L-12	64k	Fully Static Common I/O	8192x8	28	120	120	248/0.55	+5	
MSM5165L-15					150	150	248/0.55		
MSM5165L-20					200	200	248/0.55		
MSM5188-45	64k	Fully Static Common I/O	16384x4	22	45	45	605/11	+5	
MSM5188-55					55	55	605/11		
MSM5188-70					70	70	605/11		
MSM51257-85	256k	Fully Static Common I/O	32768x8	28	85	85	385/5.5	+5	
MSM51257-100					100	100	385/5.5		
MSM51257-120					120	120	385/5.5		
MSM51257L-85	256k	Fully Static Common I/O	32768x8	28	85	85	385/0.55	+5	
MSM51257L-100					100	100	385/0.55		
MSM51257L-120					120	120	385/0.55		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

● MASK ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3864	64k	Fully Static	8192x8	28	250	250	550/165	+5	
MSM38128A	128k	Fully Static	16384x8	28	250	250	550/165	+5	
MSM38256	256k	Fully Static	32768x8	28	250	250	660/165	+5	
MSM38256A	256k	Fully Static	32768x8	28	150	150	330/33	+5	
MSM28101A	1M	40 Pin MASK RAM 18x16 Chinese-character font output	3760x16 x 18	40	10μs	22μs	893	+5	JIS-Chinese-character coding system 0~7, 16~47
MSM28201A									JIS-Chinese-character coding system 48~87
MSM53256	256k	Fully Static	32768x8	28	150	150	83/0.6	+5	
MSM531000	1M	Fully Static	131072x8	28	250	250	83/0.6	+5	

• EPROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2764A	64k	EPROM	8192x8	28	200	200	790/185	+5	2764
MSM27128A	128k	EPROM	16,384x8	28	250	250	788/184	+5	27128
MSM27256	256k	EPROM	32,768x8	28	150	150	525/184	+5	27256
MSM27512	512k	EPROM	65,536x8	28	150	150	525/184	+5	27512
MSM271000	1M	EPROM	131,072x8	32	120	120	525/184	+5	271000
MSM271024	1M	EPROM	65,536x16	40	120	120	525/184	+5	271024
MSM27C1024	1M	EPROM	65,536x16	40	100	100	175/0.55	+5	27C1024

• OTP (ONE TIME PROGRAMMABLE READ-ONLY MEMORY)

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (nw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2764AZB	64k	OTP	8,192x8	28	150	150	525/184	+5	
MSM27128AZB	128k	OTP	16,384x8	28	150	150	525/184	+5	
MSM27256ZB	256k	OTP	32,768x8	28	170	170	525/184	+5	
MSM27512ZB	512k	OTP	65,536x8	28	200	200	525/184	+5	

• E^2P ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (nw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM16811	1k	E^2P ROM	64x16 or 128x8	8	1,000	1,000	–	+5	
MSM16911	1k	E^2P ROM	64x16 or 128x8	8	1,000	1,000	–	+5	

MOS MEMORY HANDLING PRECAUTIONS

MOS MEMORY HANDLING PRECAUTIONS

1. STATIC ELECTRICITY COUNTER-MEASURES

Since voltage is generally controlled by means of the transistor gate oxide film in MOS memories, the input impedance is high and the insulation tends to be destroyed more readily by static electricity.

Although Oki MOS memories incorporate built-in protector circuits to protect all input terminals from such destruction, it is not considered possible to give complete protection against heat destruction due to overcurrents and insulation film destruction due to irregular high voltages. It is, therefore, necessary to observe the following precautionary measures.

1) Under no circumstances must voltages or currents in excess of the specified ratings be applied to any input terminal.
2) Always use an electrically conductive mat or shipping tubes for storage and transporting purposes.
3) Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also avoid handling devices with bare hands. If handling with bare hands cannot be avoided, make sure that the body is grounded, and that a 1MΩ resistor is always connected between the body and ground in order to prevent the generation of static electricity.
4) Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially during dry seasons.
5) When using a soldering iron, the iron should be grounded from the tip. And as far as possible, use low power soldering irons (12 V or 24 V irons).

2. POWER SUPPLY AND INPUT SIGNAL NOISE

2.1 Power supply noise absorption

In dynamic memories, the flow of power supply current differs greatly between accessing and standby modes.

Although very little power is consumed by CMOS memories during standby mode, considerable current is drawn for charging and discharging (instantaneous current requirements) during access mode. In order to absorb the "spike noise" generated by these current requirements, the use of relatively large capacitance capacitors (about one 10μF capacitor for every 8 to 10 RAMs) is recommended along with good high frequency response capacitors of about 0.1μF for each memory element. Power line wiring with as little line impedance as possible is also desirable.

2.2 Input signal noise absorption

Overshooting and undershooting of the input signal should be kept to a bare minimum. Undershooting in particular can result in loss of cell data stability within the memory. For this reason,

(1) Avoid excessive undershooting when using an address common bus for memory board RAMs and ROMs.
(2) Since noise can be generated very easily when using direct drive for applying memory board RAM addresses from other driver boards, it is highly recommended that these addresses be first received by buffer.
(3) Methods available for eliminating undershooting generated in the address line include
   a) Clamping of the undershooting by including a diode.
   b) Connect 10~20Ω in series with driver outputs.
   c) Smooth the rising edge and falling edge waveforms.

3. CMOS MEMORY OPERATING PRECAUTIONS

3.1 Latch-Up

If the CMOS memory input signal level exceeds the Vcc power line voltage by +0.3 V, or drops below the ground potential by −0.3 V, the latch-up mechanism may be activated. And once this latch-up mode has been activated, the memory power has to be switched off before normal operating mode can be restored. Destruction of the memory element is also possible if the power is not switched off.

Although Oki CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided.

3.2 Battery Back-Up

Take special note of the following 4 points when designing battery back-up systems.

(1) Do not permit the input signal H level to exceed Vcc +0.3 V when the memory Vcc power is dropped. To achieve this, it is recommended that a CMOS driver using a Vcc power common with the CMOS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMOS memory be used for driving purposes.
(2) Set the chip select input signal CE to the same H level as the CMOS memory Vcc power line. And in order to minimize memory power consumption, set the write enable input $\overline{WE}$ level, the address input and the data input to either ground level or to the same H level as the CMOS memory Vcc power line.
(3) Make sure that the CMOS memory Vcc power line is increased without "ringing" or temporary breaks when restoring the battery back-up mode.
(4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that accessing occurs after elapse of the chip enable off time (t_{CC}) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range.

For further details, refer to "CMOS Memory Battery Back-up" at the end of this manual.

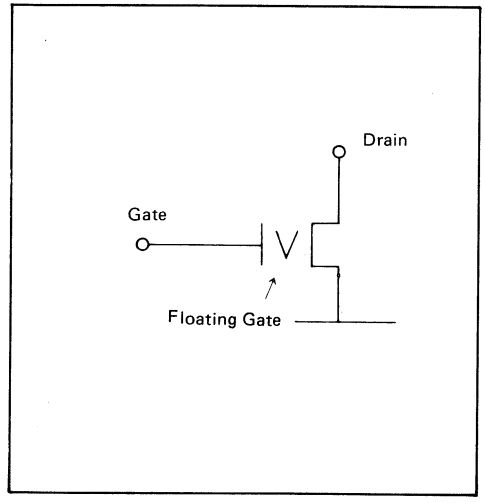
EPROM WRITING AND ERASURE

EPROM WRITING AND ERASURE

1. EPROM WRITING ERASURE

1.1 EPROM MSM2764 writing

Writing in the MSM2764RS involves setting the drain and gate voltages of the floating gate stage to a high voltage. When the drain voltage exceeds 15 V and the gate voltage 20 V, the channel charge (electrons) becomes highly energized and flow over the oxide film barrier into the floating gate. And since the high gate voltage is positive polarity, electrons will flow into the floating gate very easily. When electrons build up in the floating gate, the memory element "threshold voltage" is changed, and subsequently stored as memory data. Once the charge has been built up, the surrounding oxide film (high insulation) prevents escape of electrons. The data is thus stored as "non-volatile" data.



When the MSM2764RS is shipped from the factory, the floating gate is left in discharged status (all bits "1"), i.e. "blank" status. During writing processes, +25 V is applied to the Vpp terminal and V_{IH} to the $\overline{OE}$ input. The data to be programmed is applied in parallel to the outputs ($O_0 - 7$). After the address and data have been set up, application of V_{IH} level for 50 ms to the $\overline{CE}$ input will enable writing of data. Since the +25 V applied to Vpp is fairly close to the element's withstanding voltage, make sure that the voltage setting is maintained strictly within the 25 V ±1 V range. Application of voltages in excess of the rated voltage, and overshooting, to the Vpp terminal can result in permanent damage to the element.

Although MSM2764RS rewriting should be checked about 100 times by sample testing, in actual practice 5 to 10 times is usually the limit. This will not likely result in any problem.

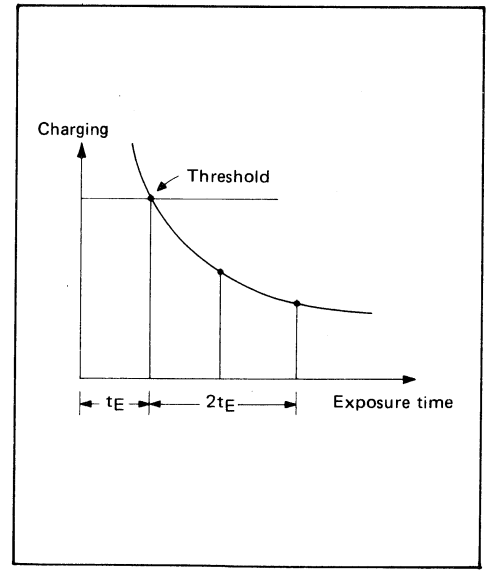
1.2 PROM programmer

Oki Electric employs a system whereby the various programmer available on the market are examined, and agreements reached with different programmer manufacturers. The purpose of this system is to check compatibility between programmer manufacturers and Oki Electric devices, and making modifications whenever required. Users are thus ensured trouble-free use.

In the event of EPROM trouble with Oki devices and approved programmer, problems will be handled by both Oki and driver manufacturer except where such problems have been caused purposely.

1.3 Erasure

Erasure of data written in the MSM2764RS can be effected by ultra-violet radiation of the memory element. In this case, the charge is discharged into the substrate or electrode by the ultra-violet energy, but note that the following erasure conditions must be met. If a memory which has not been properly erased is used, writing problems and operating failures are likely to arise. Also note that excessively long erasure times (of several hours duration) can also result in failure.



Lengthy exposure to direct sunlight can also result in loss of bits. Direct exposure of MSM2764 to the strong summer sun for a single day can result in bit changes. Although normal fluorescent lights have practically no effect, light rays beamed onto elements can cause special changes. It is therefore recommended that the glass face be covered with a screening label.

2. EPROM HANDLING

2.1 Defects caused by static electricity

The generation of static electricity on the EPROM glass face can result in changes in the memory contents. This, however, can be restored by brief exposure (several seconds) to ultra-violet radiation. But this exposure must be kept short. Exposure for 30 seconds or more can cause changes in the normal bits.

2.2 Handling precautions

(1) Avoid carpets and clothes etc where static electricity is generated.
(2) Make sure the programmer and mounting system are securely grounded.
(3) Also make sure that any soldering iron employed is properly grounded.
(4) Always carry in an electrically conductive plastic mat.
(5) Written ROMs are also to be kept in an electrically conductive plastic mat.
(6) Do not touch the glass seal by hand since this can result in deterioration of the ultra-violet permeability required for erasure, and subsequently lead to poor erasure.

2.3 System debugging precautions

During system debugging, check operations with a voltage of ±5% (oscillating).

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

The mask ROM custom program code programming method is outlined below.

1. USABLE MEDIA

(1) Magnetic tape
(2) EPROM

Magnetic tape and EPROM are used as standard.

2. MAGNETIC TAPE SPECIFICATIONS

2.1 Use the following types of magnetic tape in magnetic tape units compatible with IBM magnetic tape units.

(1) Length: 2400 feet, 1200 feet or 600 feet
(2) No label
(3) Width: 1/2 feet
(4) Channels: 9 channels
(5) Bit density: 800BPI standard, although 1600BPI can also be employed.
(6) Block size: Integer multiples of 256 bytes possible with 256 bytes as standard. 1 block, 1 record is standard.

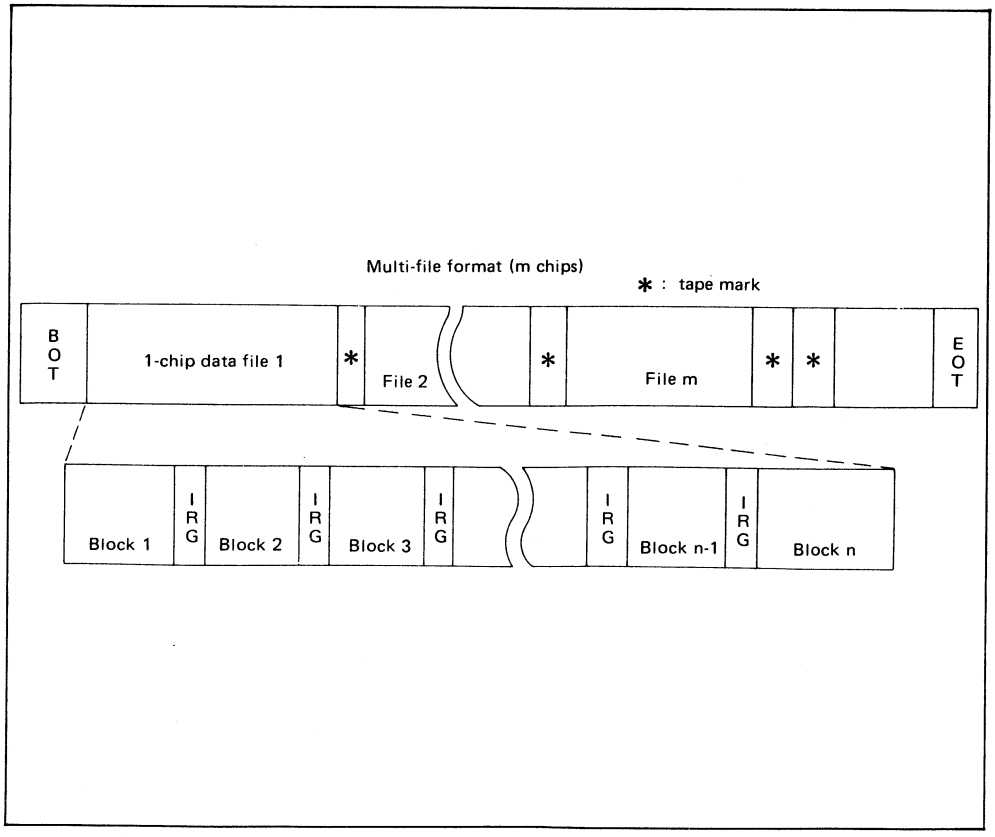
2.2 Magnetic tape format

(1) The data for a single chip should not extend into several tapes. Data for several chips are allowed to be included in a single magnetic tape, multiple file format being permitted. In this case, include the data of a single chip in one file.
(2) Use tape marks for file partitions when employing multiple file formats.
(3) Denote the completion of a magnetic tape file by two successive tape marks.

2.3 Magnetic tape data format

(1) The data contained in a single file on magnetic tape must be inserted from the head address $(0000)_{hex}$ of the device up to the final address in succession for a single chip.
(2) In this case, the LSB of the data should correspond to D_0, and the MSB to D_7.
(3) "1" bits in the data denote high device output, while "0" denotes low output.

2.4 Magnetic tape examples



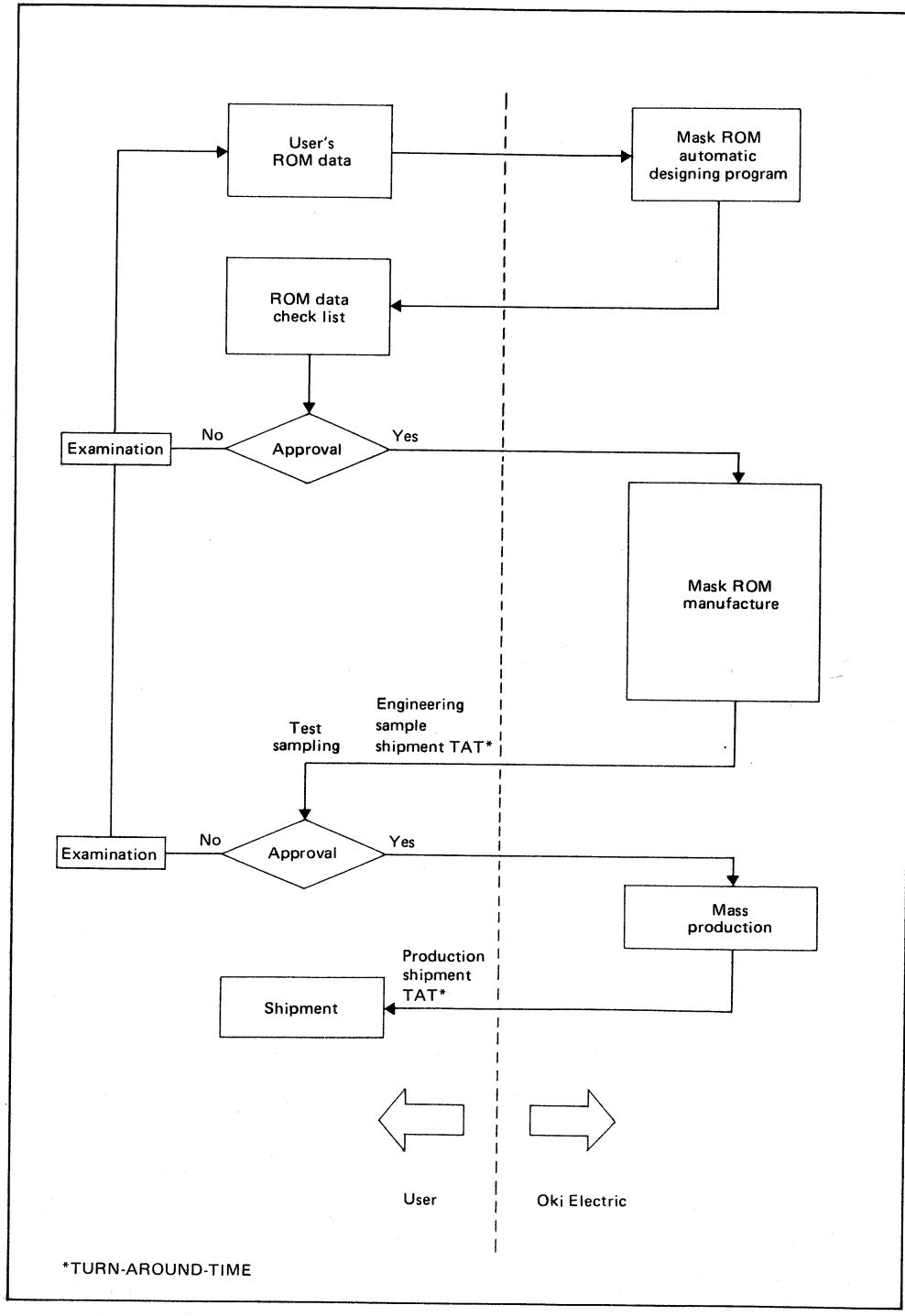
3. EPROM SPECIFICATIONS

(1) MSM2764, Intel 2764 or 27128 equivalent device may be used.

(2) Prepare 2 EPROMs containing identical data.

MASK ROM DEVELOPMENT FLOWCHART

MASK ROM DEVELOPMENT FLOWCHART



TERMINOLOGY AND SYMBOLS

TERMINOLOGY AND SYMBOLS

1. PIN TERMINOLOGY

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power Supply Voltage Pin	V_{DD}, V_{CC} V_{GG}, V_{BB}	V_{CC}	V_{CC}	V_{DD}, V_{CC}
Address Input Pin	$A_0 \sim A_{12}$	$A_0 \sim A_{13}$	$A_0 \sim A_{11}$	$A_0 \sim A_7$
Data Input Pin			DI	D IN
Data Output Pin	$O_0 \sim O_7$	$D_0 \sim D_{15}$	DO	D OUT
Data Input/Output Pin			$I/O_1 \sim I/O_8$	
Chip Enable Pin	CE	CE	CE	
Output Enable Pin	OE	OE	OE	
Address Enable Pin		AE		
Chip Select Pin	CS		CS	
Write Enable Pin	WE		WE	$\overline{WE}$
Row Address Strobe Pin				$\overline{RAS}$
Column Address Strobe Pin				$\overline{CAS}$
Program Input Pin	Program, V_{PP}			
Data Valid Pin		DV		
Clock Input Pin		ϕT		
Ground Pin	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Vacant Terminal	NC	NC		

2. ABSOLUTE MAXIMUM RATINGS

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{SS}
Terminal voltage	V_T		V_T	V_T
Input voltage	V_I	V_I	V_I	V_I
Output voltage	V_O	V_O	V_O	V_O
Input current				
Output current			I_O	
Output short circuit current				I_{OS}
Load capacitance				
Power dissipation	P_D	P_D	P_D	P_D
Operating temperature	Topr	Topr	Topr	Topr
Storage temperature	Tstg	Tstg	Tstg	Tstg

3. RECOMMENDED OPERATION CONDITIONS

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power Supply Voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{BB} V_{SS}
"H" Clock Input Voltage				V_{IHC}
"H" Input Voltage	V_{IH}	V_{IH}	V_{IH}	V_{IH}
"L" Input Voltage	V_{IL}	V_{IL}	V_{IL}	V_{IL}
Data Pretention Voltage			V_{CCH}	
Load Capacitance		C_L	C_L	
Fan-out	N	N	N	
Operating Temperature	Topr	Topr	Topr	Topr

4. DC CHARACTERISTICS

Term	EPROM	ROM	Static RAM	Dynamic RAM
"H" output voltage	V_{OH}	V_{OH}	V_{OH}	V_{OH}
"L" output voltage	V_{OL}	V_{OL}	V_{OL}	V_{OL}
"H" output current			I_{OH}	
"L" output current				
Input leakage current	I_{LI}	I_{LI}	I_{LI}	I_{LI}
Output leakage current	I_{LO}	I_{LO}	I_{LO}	I_{LO}
I/O leak current			I_{LO}	
Program terminal current	I_{PP1}, I_{PP2}			
Peak power on current		I_{PO}	I_{PO}, I_{SBP}	
Power supply current	I_{DD}, I_{CC} I_{BB}, I_{CC1} I_{CC2}	I_{CC}, I_{CCS} I_{CCA}	I_{CC}, I_{CCA} I_{CC1}, I_{CC2} I_{CCS}, I_{CCS1} I_{SB}	I_{DD1}, I_{CC1}, I_{BB1} I_{DD2}, I_{CC2}, I_{BB2} I_{DD3}, I_{CC3}, I_{BB3} I_{DD4}, I_{CC4}, I_{BB4}

5. AC CHARACTERISTICS

(1) Read cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Read cycle time		t_C, t_{RC}, t_{CYC}	t_{RC}	t_{RC}
Address access time	t_{ACC}	t_{AA}, t_{ACC}	t_A, t_{AC}, t_{ACC}, t_{AA}	
Chip select access time	t_{CO}	t_{CS}	t_{CO}, t_{ACS1}, t_{ACS2}	
Chip enable access time	t_{CE}	t_{ACE}	t_{AC}	
Output enable access time	t_{OE}	t_{CO}	t_{OE}	
Output setting time		t_{LZ}	t_{CX}, t_{LZ}	
Output valid time	t_{OH}	t_{OH}	t_{OH}, t_{OHA}	
Output disable time	t_{DF}	t_{HZ}	t_{OTD}, t_{HZ}, t_{OFF}	t_{OFF}
Address set-up time		t_{AS}	t_{AS}	
Address hold time		t_{AH}	t_{AH}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CE}	
Power-up time		t_{PU}	t_{PU}	
Power-down time		t_{PD}	t_{PD}	
Address enable pulse width		t_{AE}		
Data valid access time		t_{VA}		
Data valid delay time		t_{VD}		
Clock delay time		t_{VH}		
Clock pule width		t_H		
Clock delay time		t_L		
Output delay time		t_{DD}		
Output access time		t_{DA}		
Output hold time		t_{DH}		
Address enable set-up time		t_{AES}		

(2) Write Cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Write cycle time			t_{WC}	t_{RC}
Address set-up time	t_{AS}		t_{AS}, t_{AW}	
Write pulse width	t_{PW}		t_{W}, t_{WP}	t_{WP}
Write recovery time			t_{WR}	
Data set-up time	t_{DS}		t_{DS}, t_{DW}	t_{DS}
Data hold time	t_{DH}		t_{DH}	t_{DH}
Output off-time	t_{DF}		t_{OTW}, t_{WZ}	t_{OFF}
Chip select set-up time	t_{CSS}		t_{CW}	
Address hold time	t_{AH}		t_{AH}, t_{WR}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CW}, t_{CE}	
Write enable set-up time			t_{WS}	
Write enable read time			t_{WCL}	
Write enable hold time			t_{WH}	
Address/write enable setting time			t_{AW}	
Write enable output activation			t_{OW}	
Output enable set-up time	t_{OES}			
Output enable hold time	t_{OEH}			
Program read delay time	t_{DPR}			
Output enable delay time	t_{OE}			
Chip enable data valid time	t_{DV}			
Program pulse rising edge time	t_{PRT}			
Program pulse falling edge time	t_{PFT}			
V_{PP} restoration time	t_{VR}			
Chip enable hold time	t_{CH}			

PACKAGING

2

2

2 PACKAGING 37

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- 16 PIN PLASTIC 40
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PACKAGING

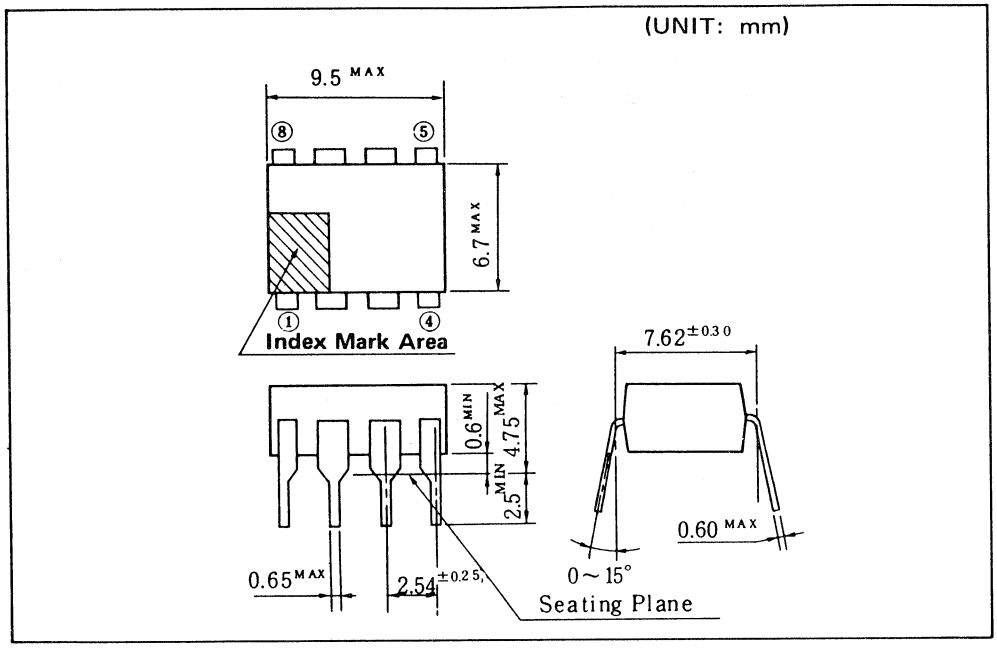
Name	No. of Pins	PACKAGES							
		RS	GS	JS	RS	YS	KS	AS	
		PLASTIC DIP	PLASTIC FLAT	PLASTIC LCC	PLASTIC SKINNY	MODULE	MODULE	SIDE-BRAZED	CERDIP
MSM3764A	16	○							
	18	○		○					
41256	16	○							
	18			○					
41256A	16	○							
	18			○					
41257A	16	○							
	18			○					
41464	18	○							
	18			○					
411000	18	○							
411001	18	○							
414256	20	○							
511000	18	○							
511001	18	○							
511002	18	○							
514256	20	○							
514258	20	○							
	26			○					
2304(8)	30					○			
	30						○		
2304(9)	30					○			
	30						○		
2307(9)	30					○			
	30						○		
2305(8)	30					○			
2310(9)	30					○			
	30						○		
2311(8)	30					○			
	30						○		
5165	28	○							
	32			○					
5165L	28	○							
	32			○					
5188	22				○				
51257	28	○							
	32			○					
51257L	28	○							
	32			○					
3864	28	○							
38128A	28	○							
38256	28	○							
38256A	28	○							
28101A	40							○	
28201A	40							○	
531000	28	○							
53256	28	○							
2764A	28								○

■ PACKAGING ■

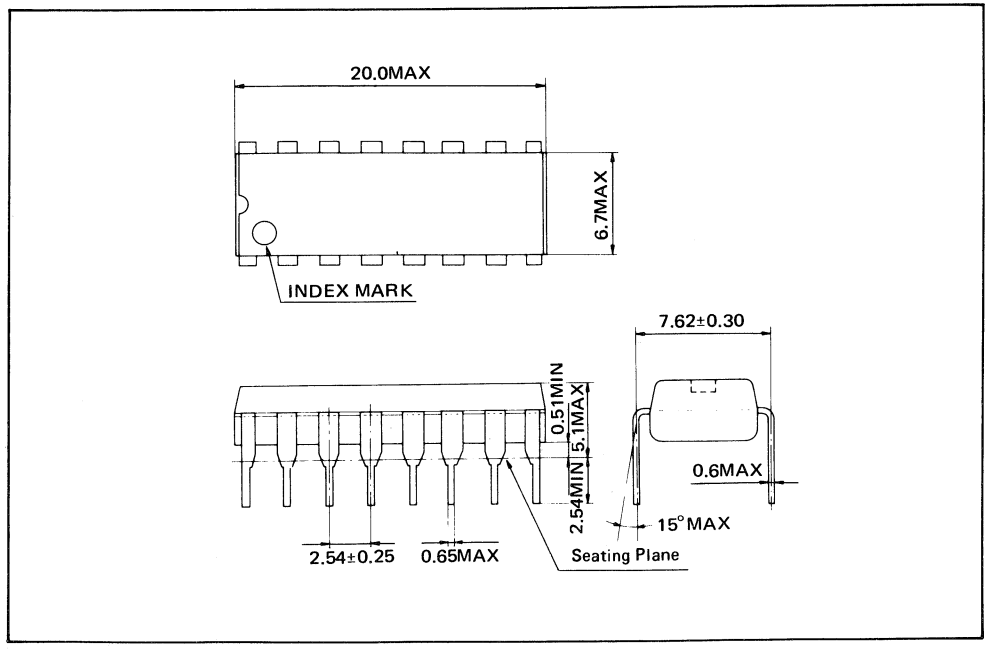
2

Name	No. of Pins	PACKAGES							
		RS	GS	JS	US	YS	KS	AS	
		PLASTIC DIP	PLASTIC FLAT	PLASTIC LCC	PLASTIC SKINNY	MODULE	MODULE	SIDE-BRAZED	CERDIP
27128A	28								○
27256	28								○
27512	28								○
271000	32								○
271024	40								○
27C1024	40								○
2764AZB	28	○							
27128AZB	28	○				○	○		
27256ZB	28	○				○	○		
27512ZB	28	○							
16811	8	○							
16911	8	○							

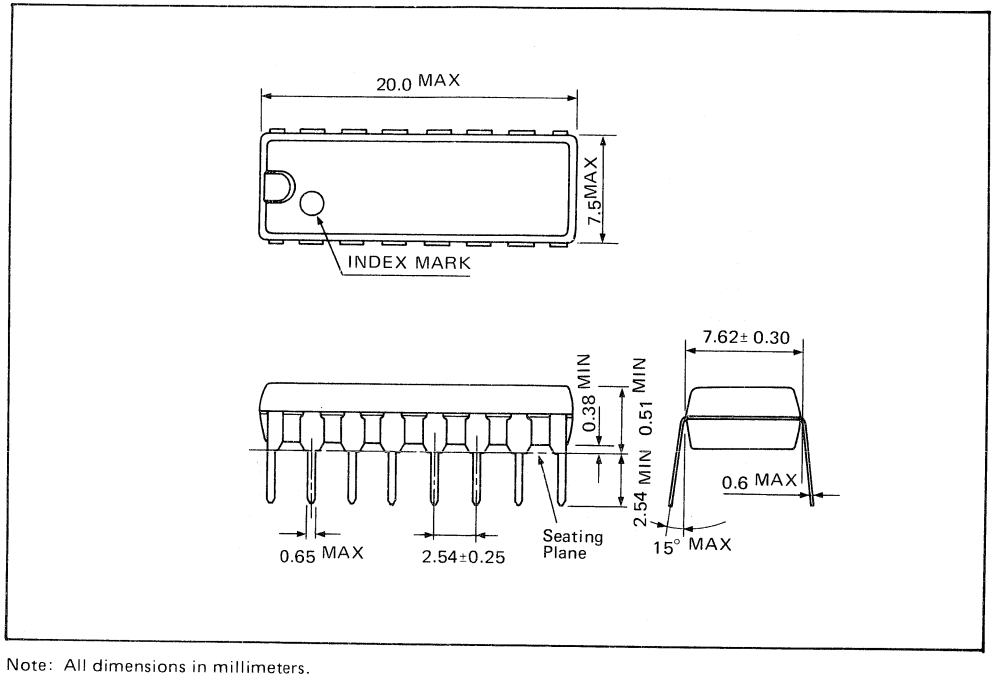
• 8 PIN PLASTIC



• 16 PIN PLASTIC

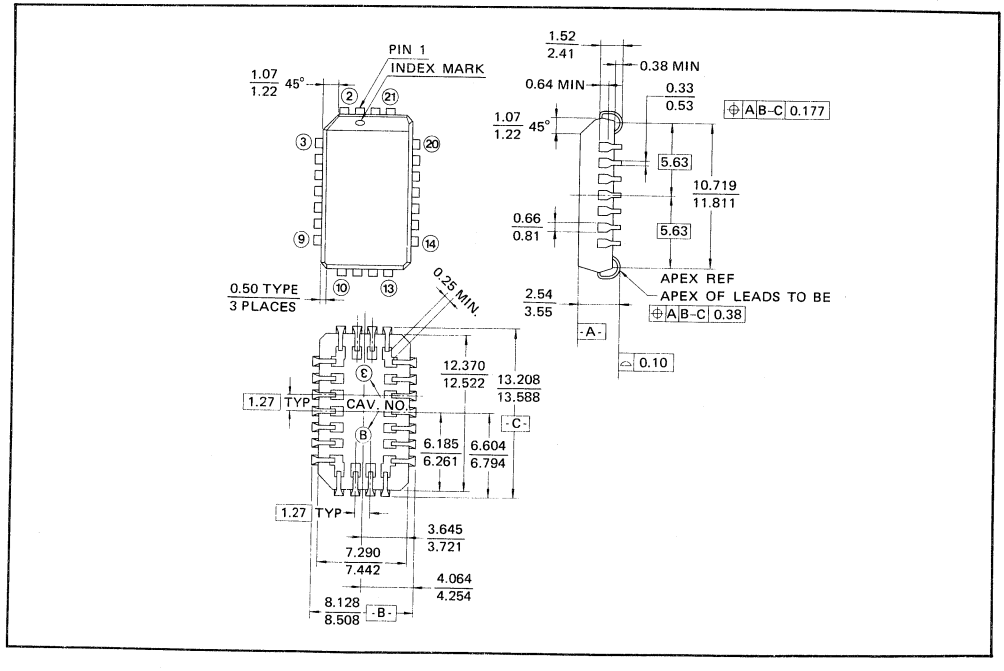


• 16 PIN PLASTIC

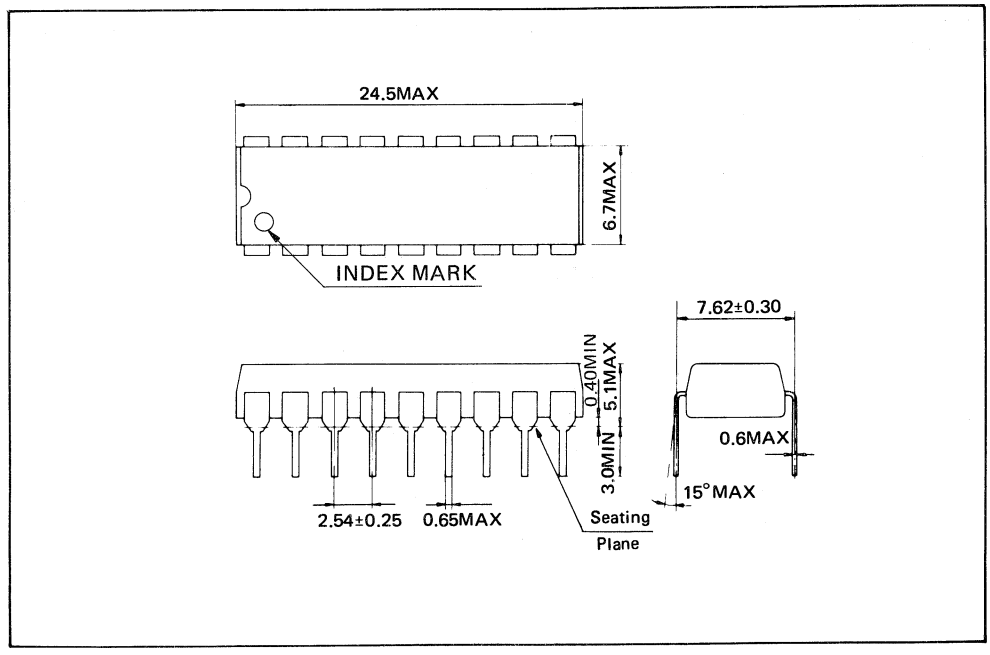


Note: All dimensions in millimeters.

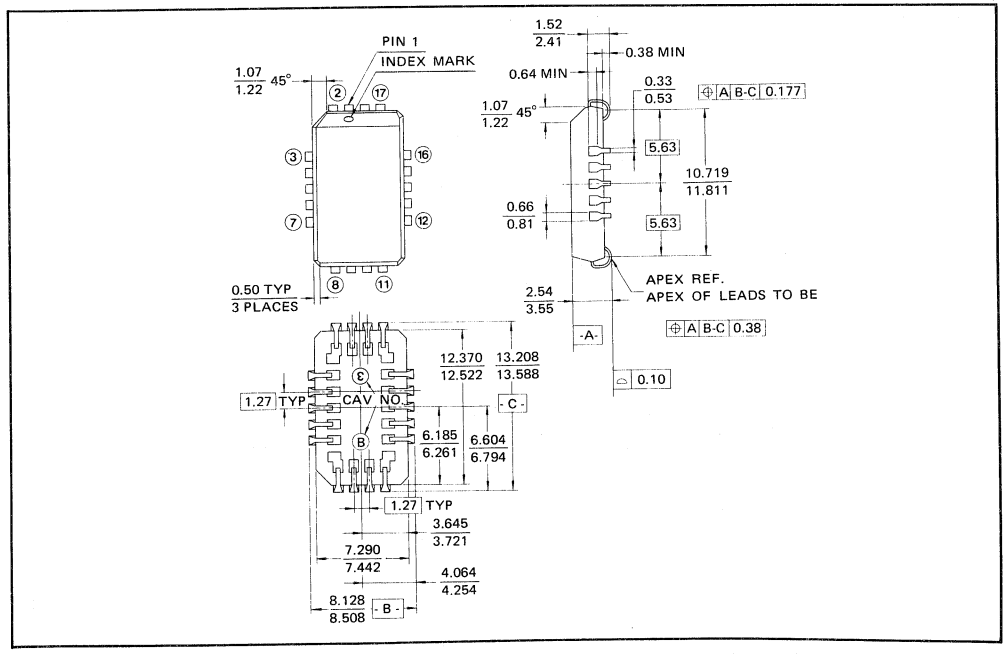
• 18 PIN PLCC



• 18 PIN PLASTIC



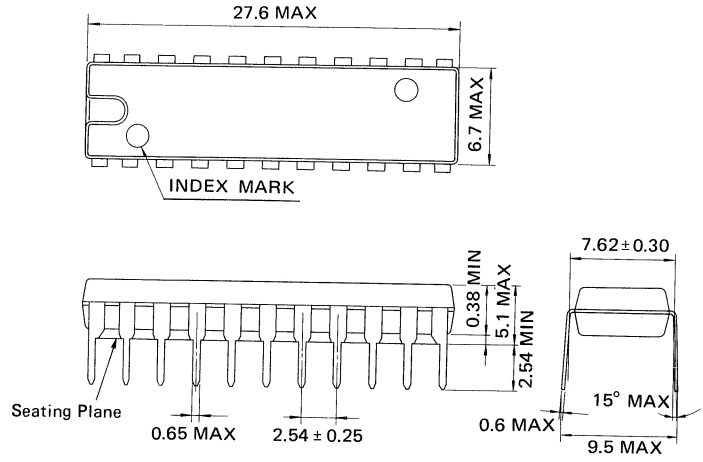
• 22 PIN PLCC



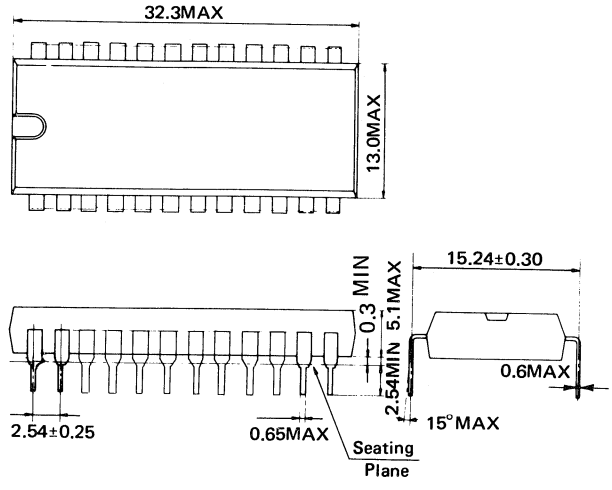
■ PACKAGING ■

2

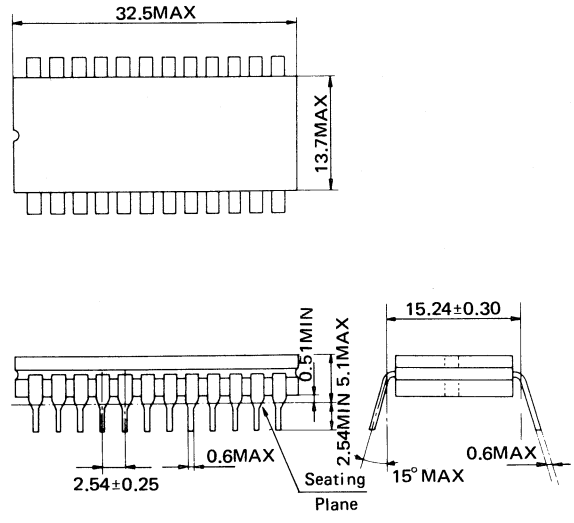
• 22 PIN PLASTIC



• 24 PIN PLASTIC

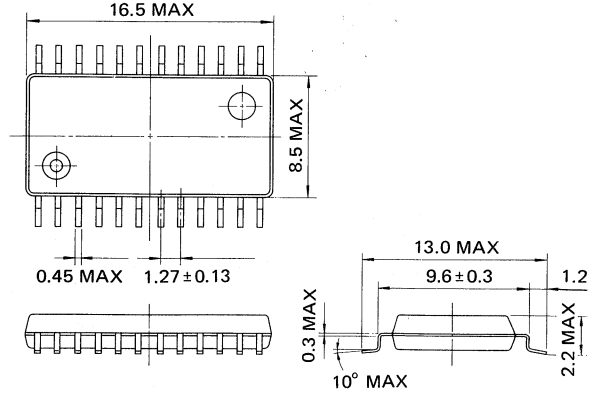


• 24 PIN CERDIP



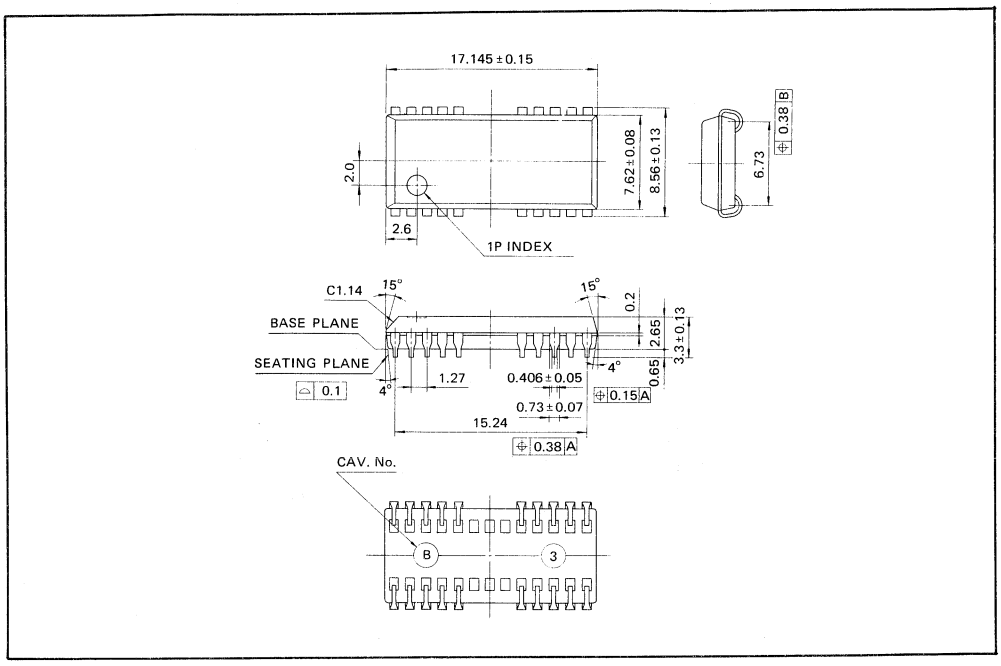
Note: All dimensions in millimeters.

• 24 PIN PLASTIC FLAT

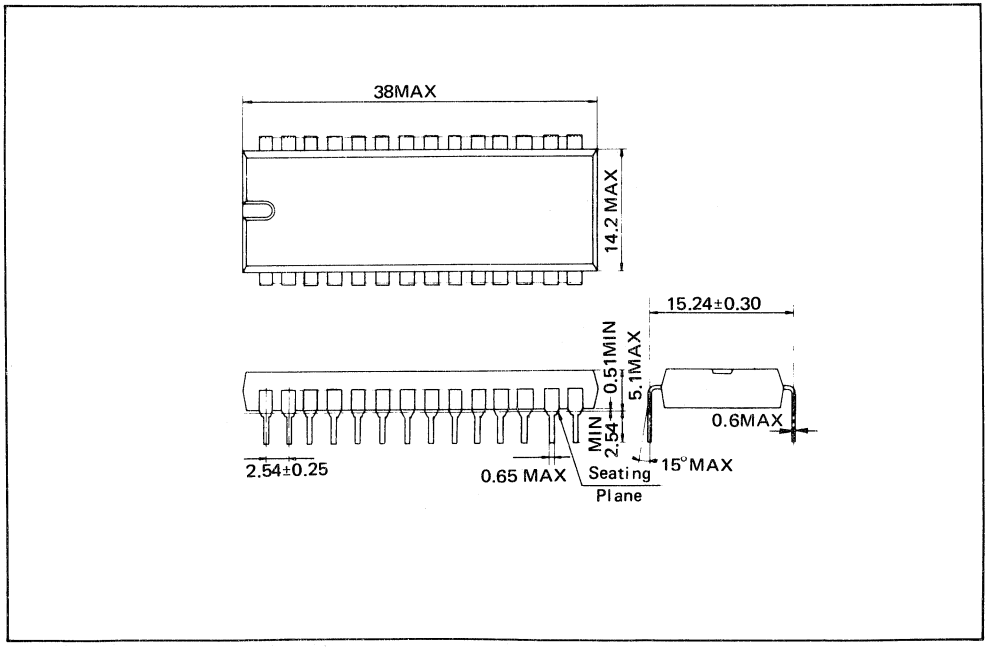


2

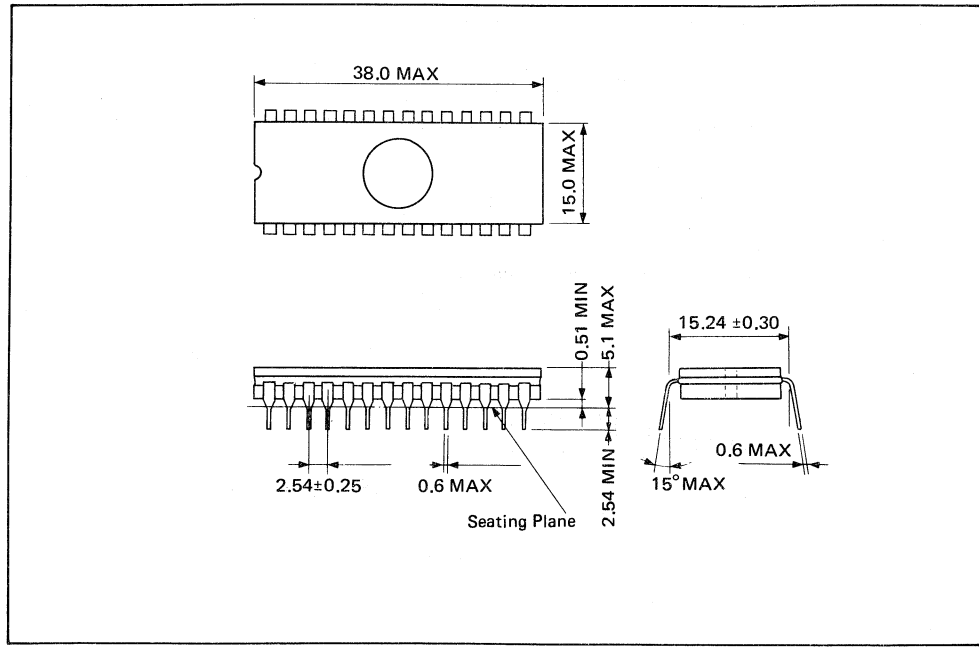
• 26 PIN SOJ



• 28 PIN PLASTIC

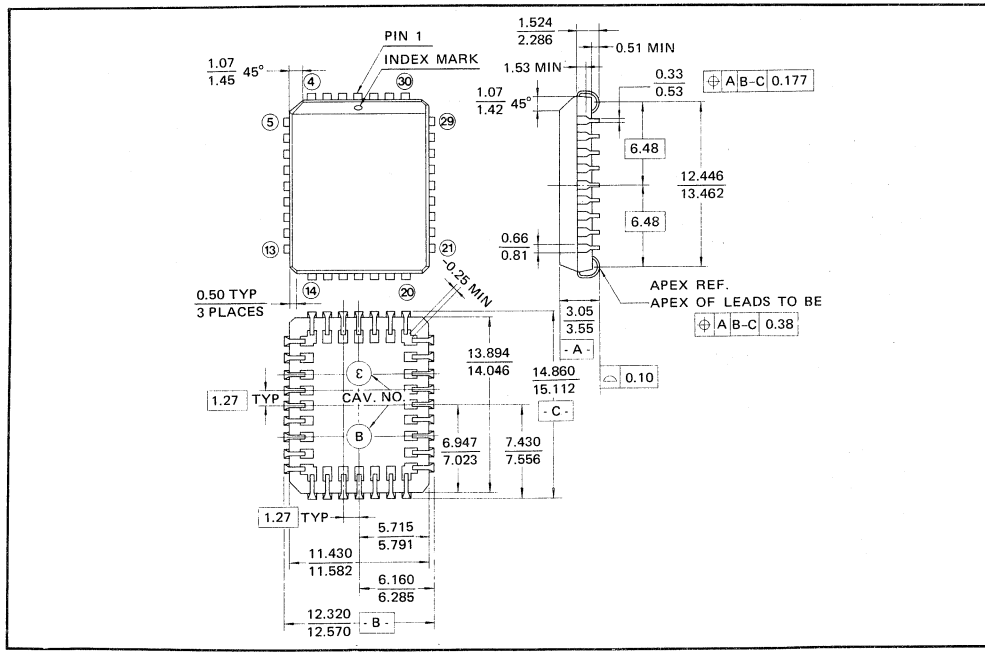


• 28 PIN CERDIP



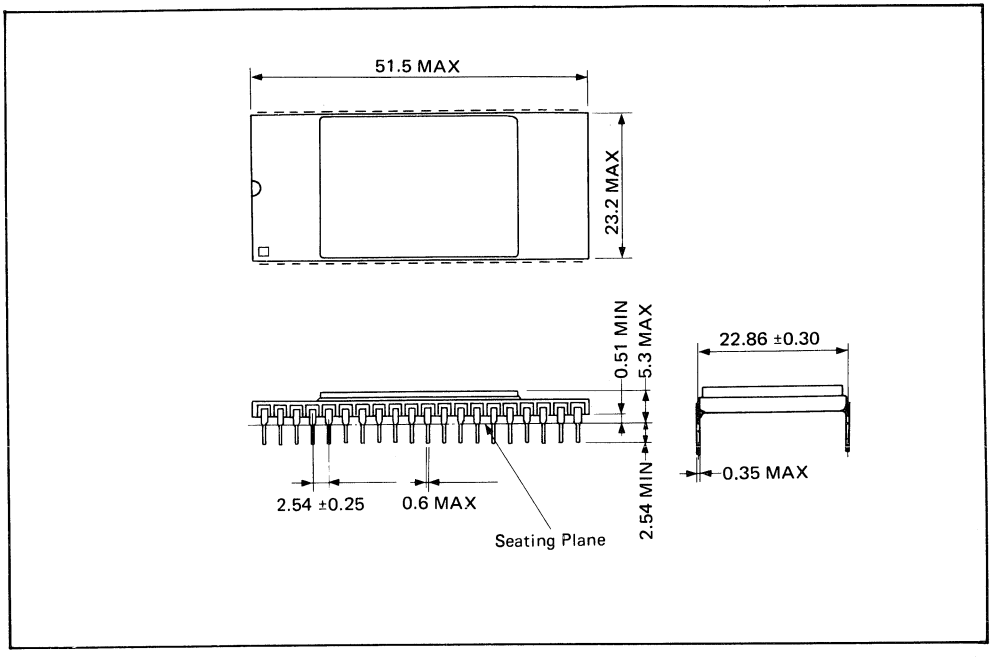
Note: All dimensions in millimeters.

• 32 PIN PLCC

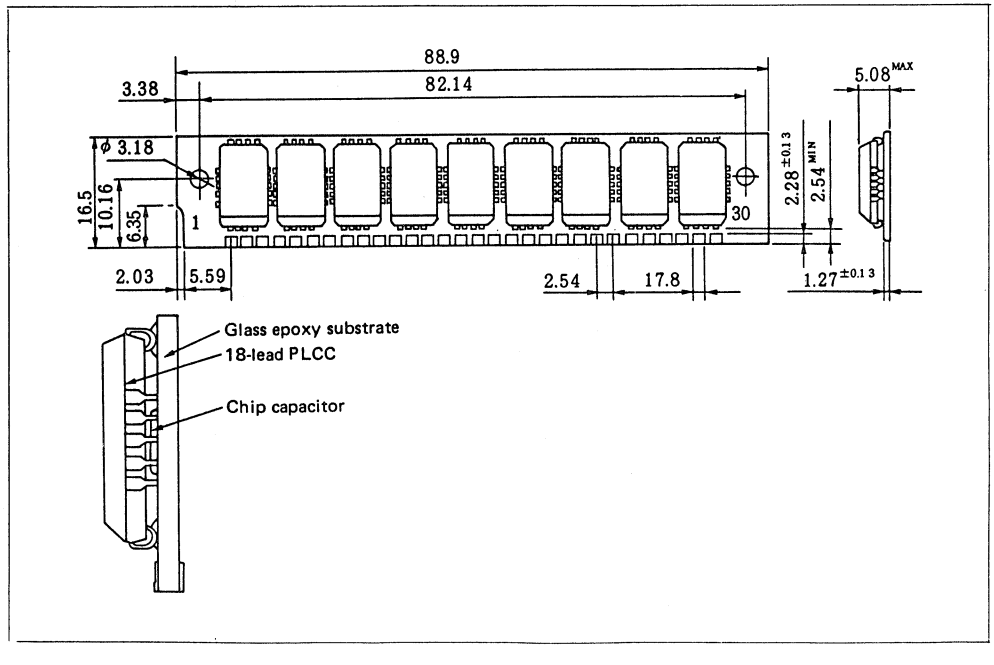


2

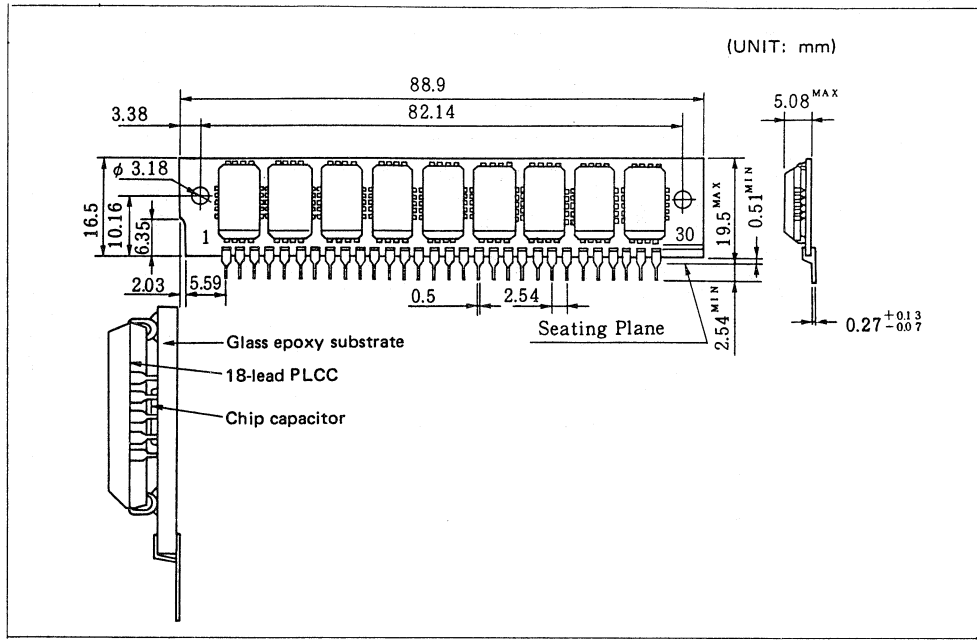
• 40 PIN SIDE-BRAZED



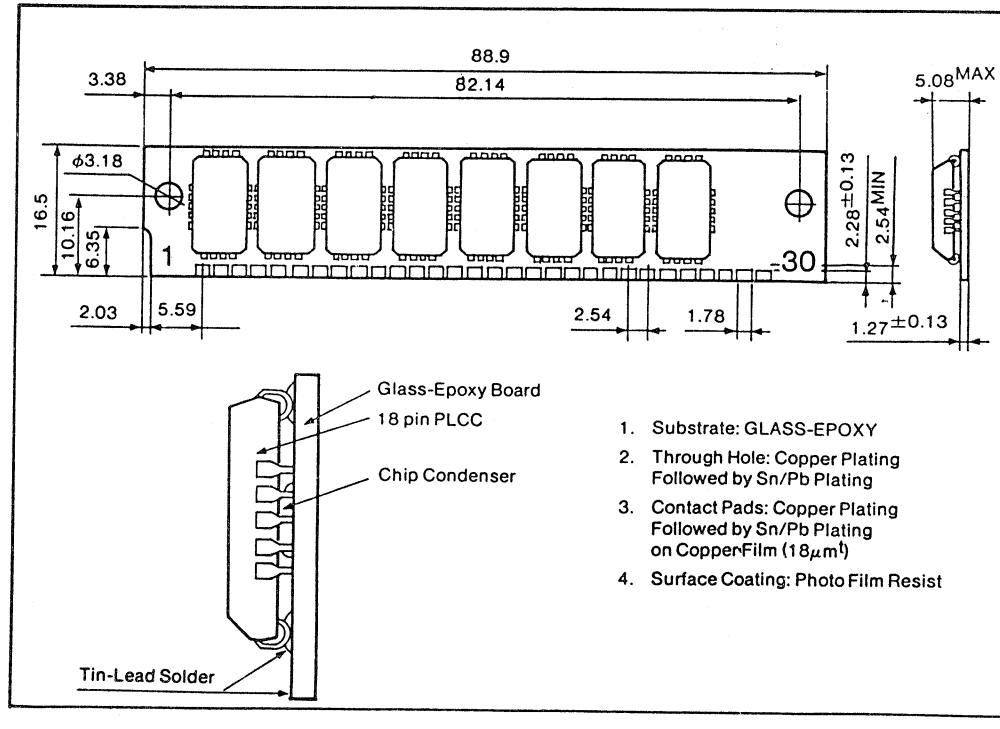
• 30 PIN SIMM (FOR MSC 2304/2307 YS9)



• 30 PIN SIMP (FOR MSC 2304/2307 KS9)

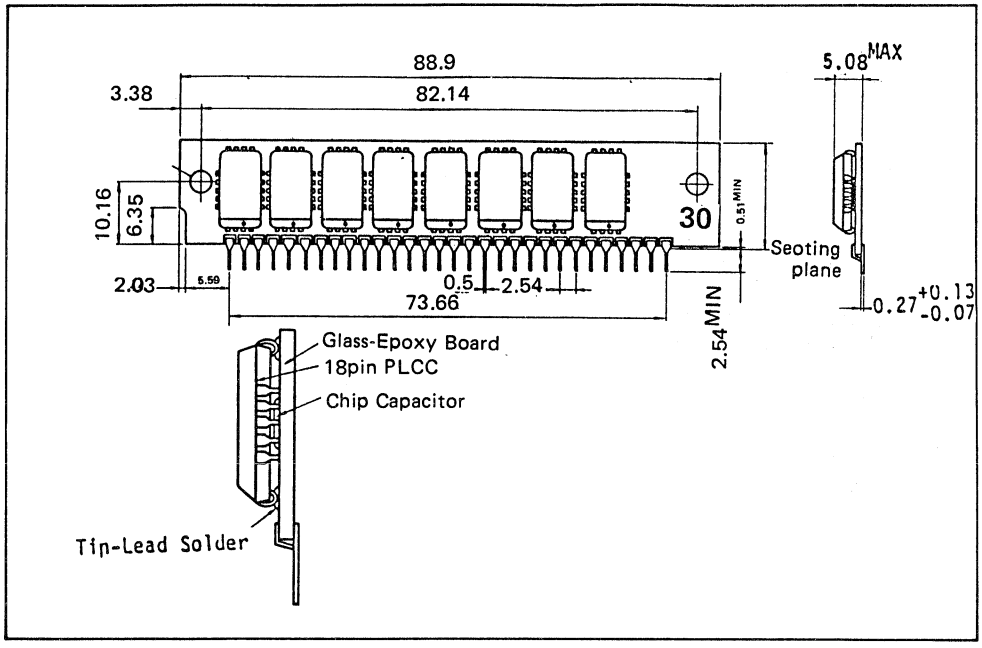


• 30 PIN SIMM (FOR MSC 2304 YS8)

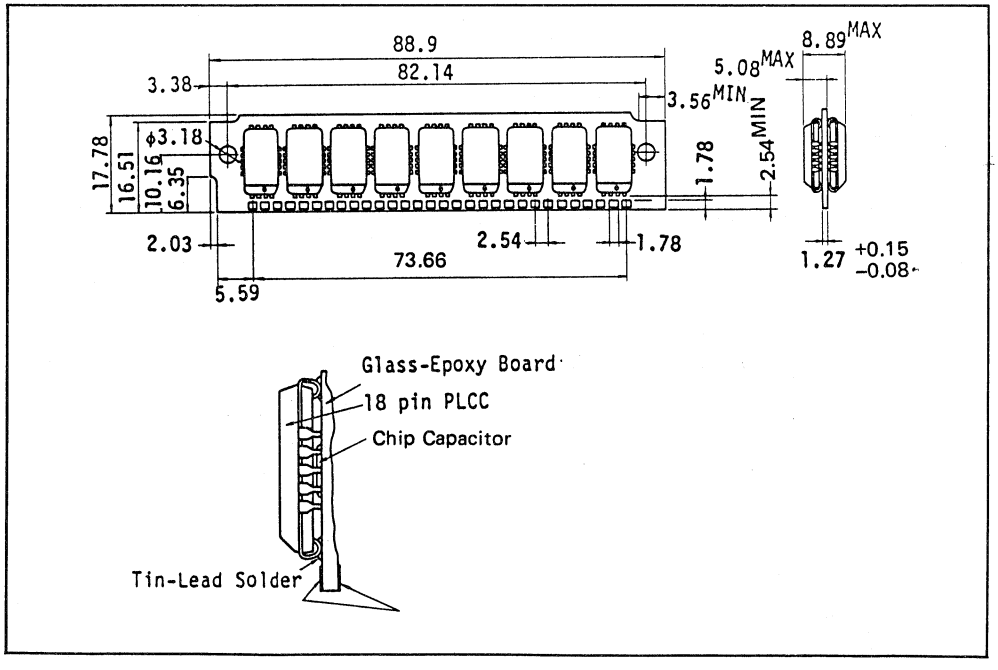


■ PACKAGING ■

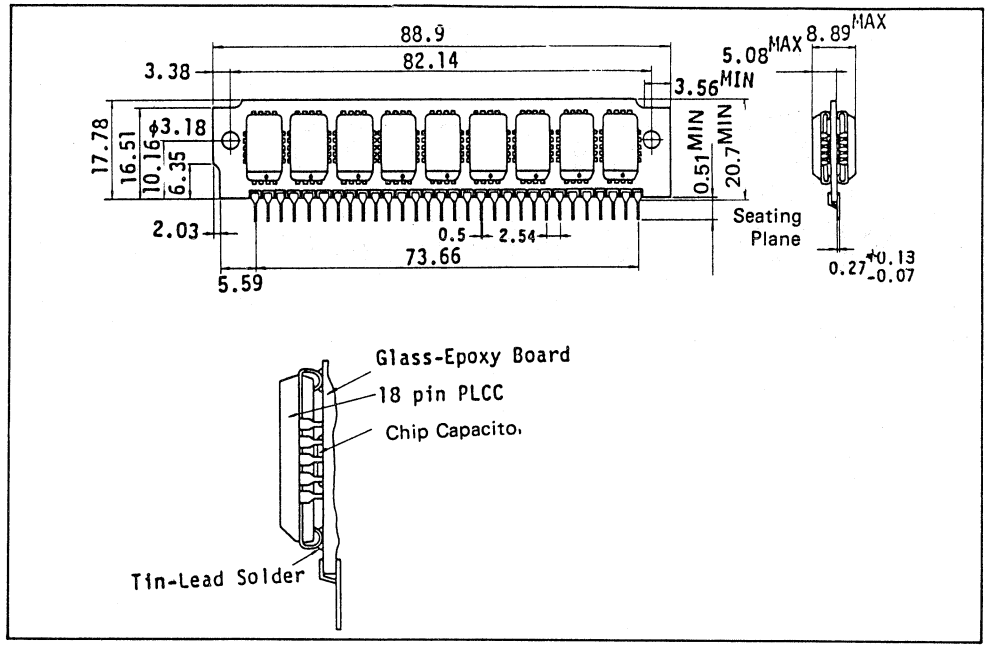
• 30 PIN SIMP (FOR MSC 2304 KS8)



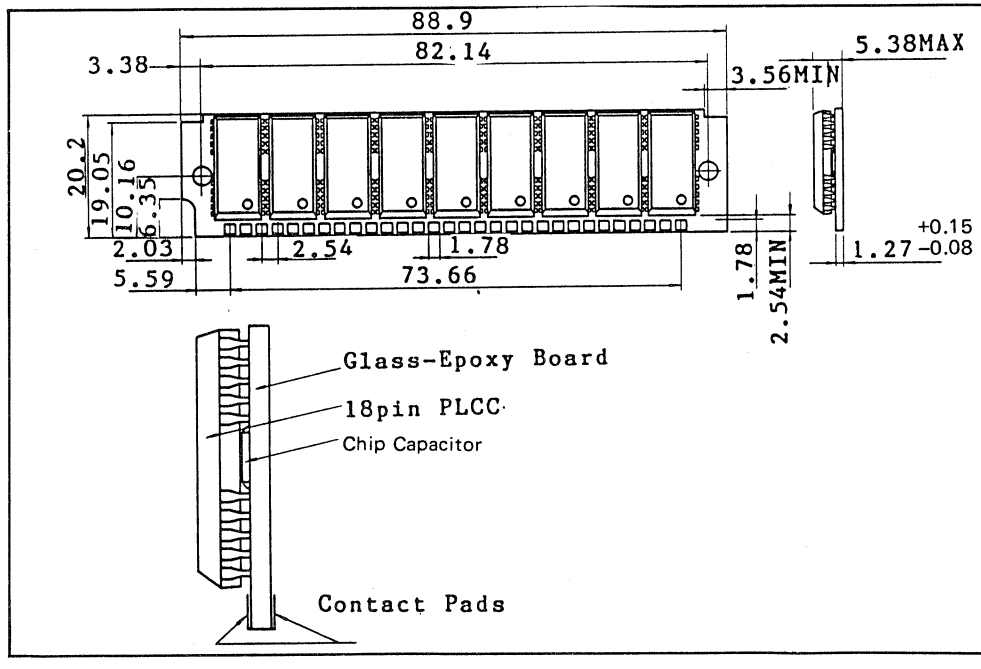
• 30 PIN SIMM (FOR MSC 2305 YS9)



• 30 PIN SIMP (FOR MSC 2305 KS9)

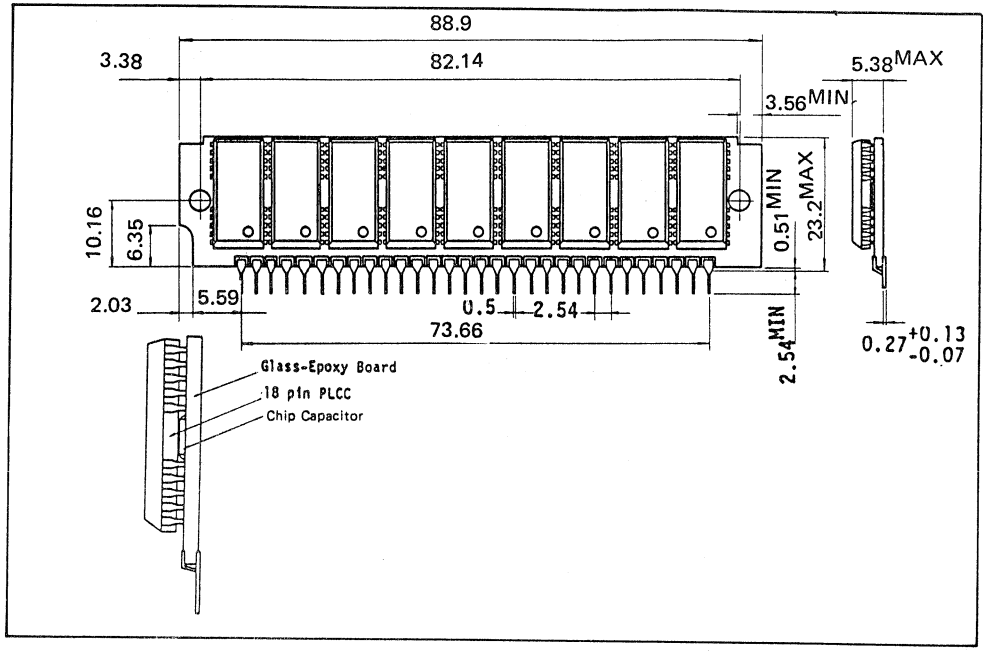


• 30 PIN SIMM (FOR MSC 2310 YS9)

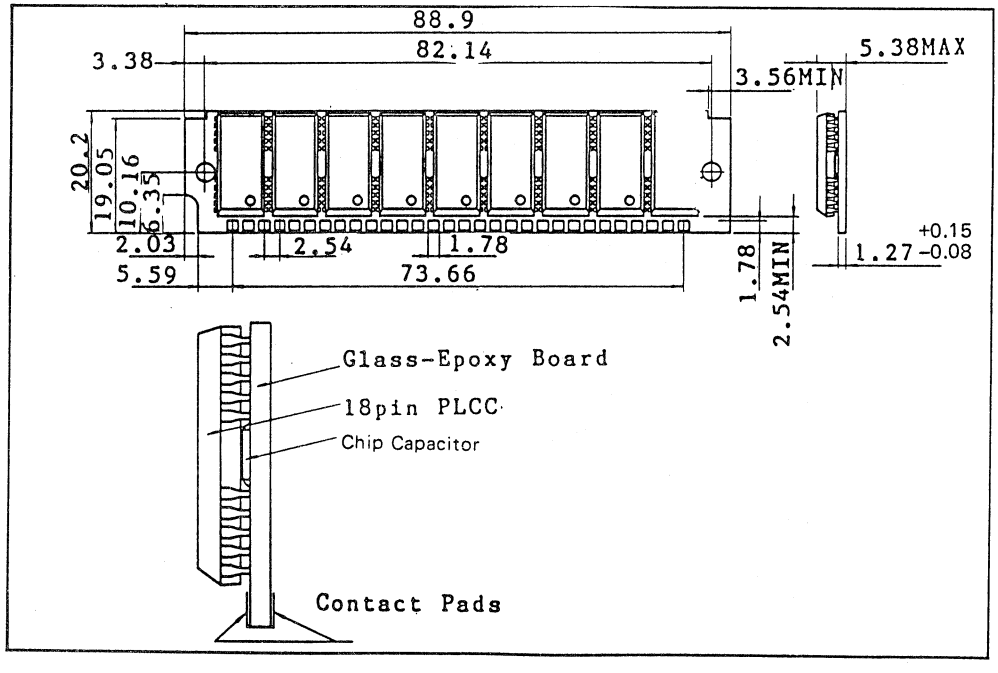


■ PACKAGING ■

• 30 PIN SIMP (FOR MSC 2310 KS9)



• 30 PIN SIMM (FOR MSC 2311 YS8)



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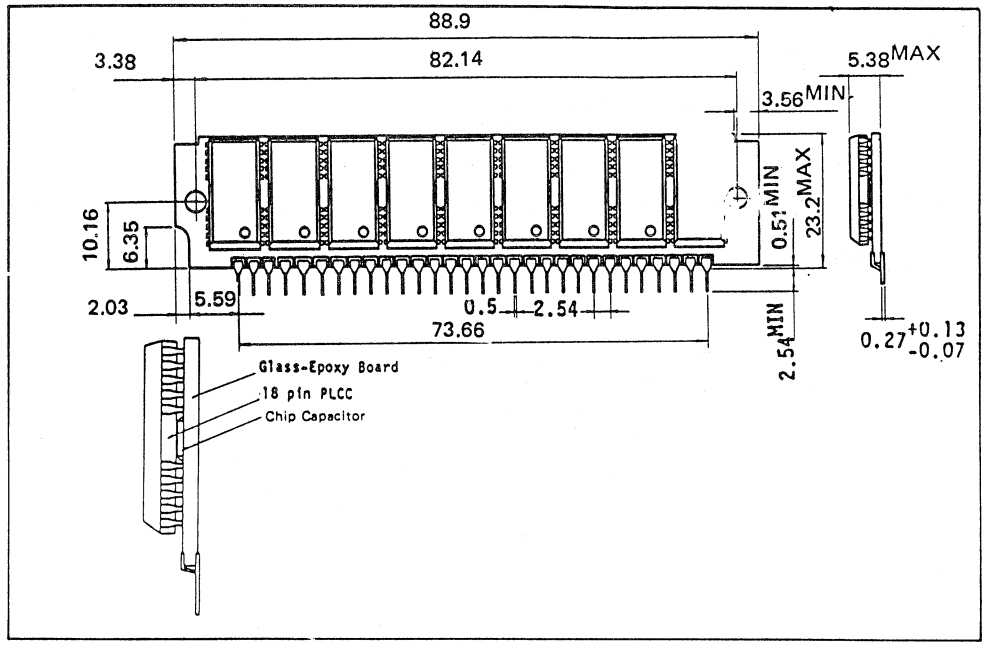
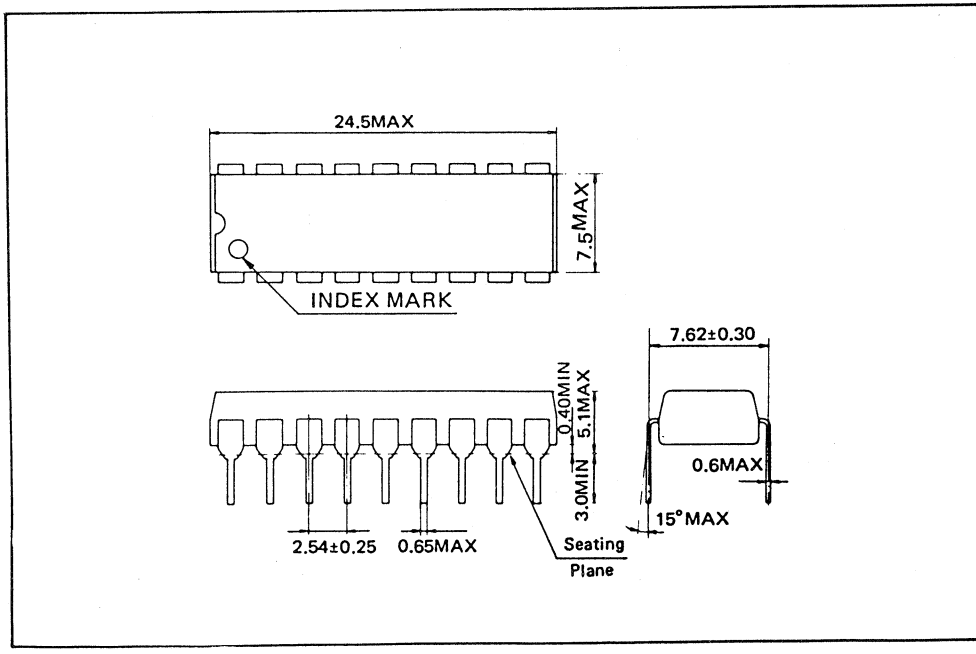
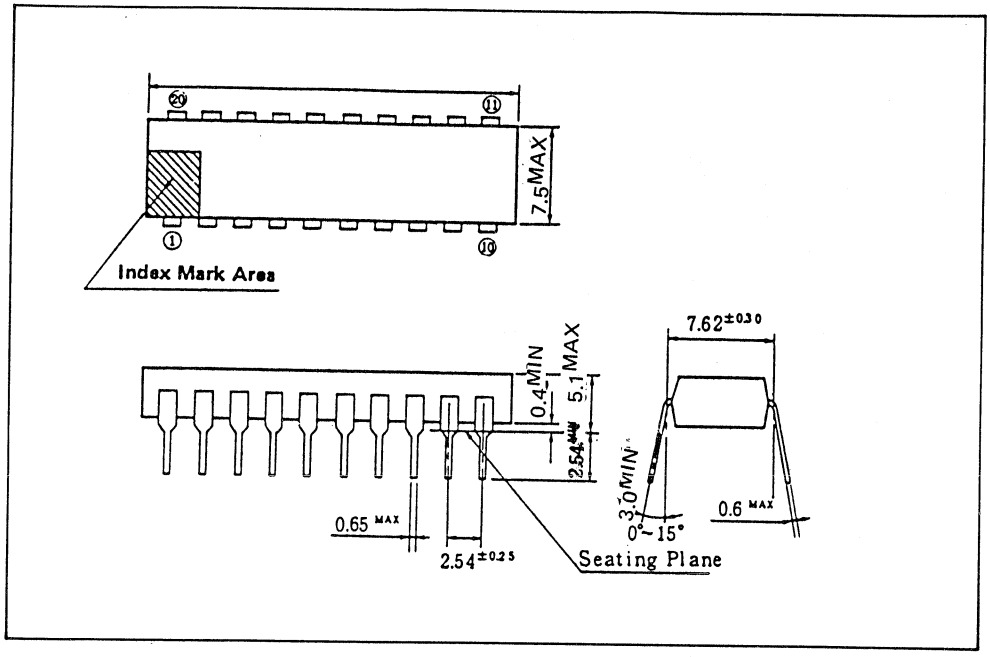


• 18 PIN PLASTIC

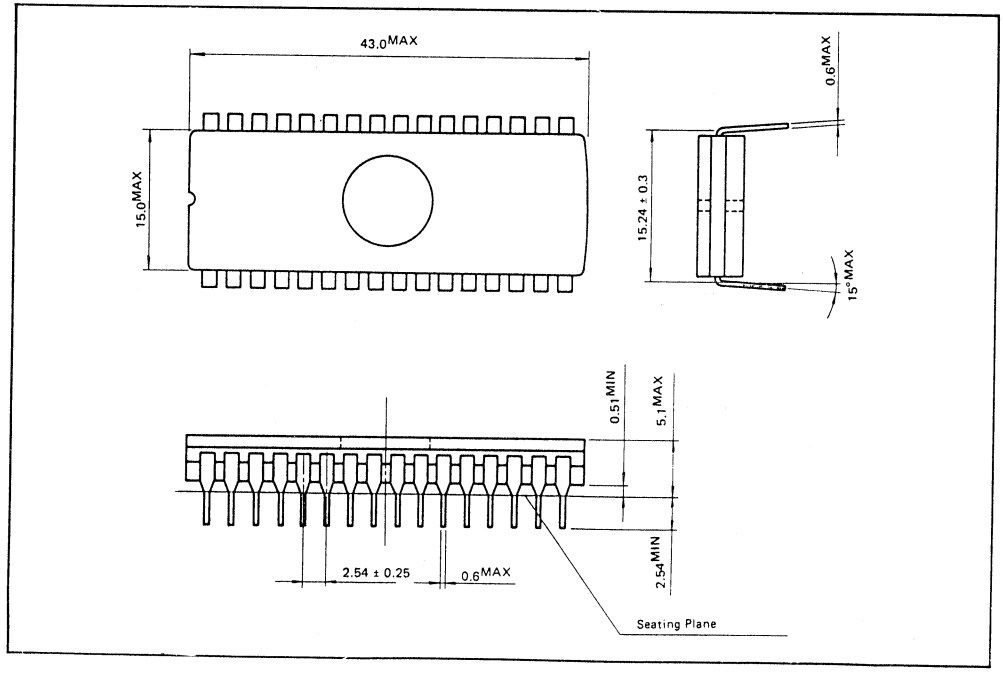


■ PACKAGING ■

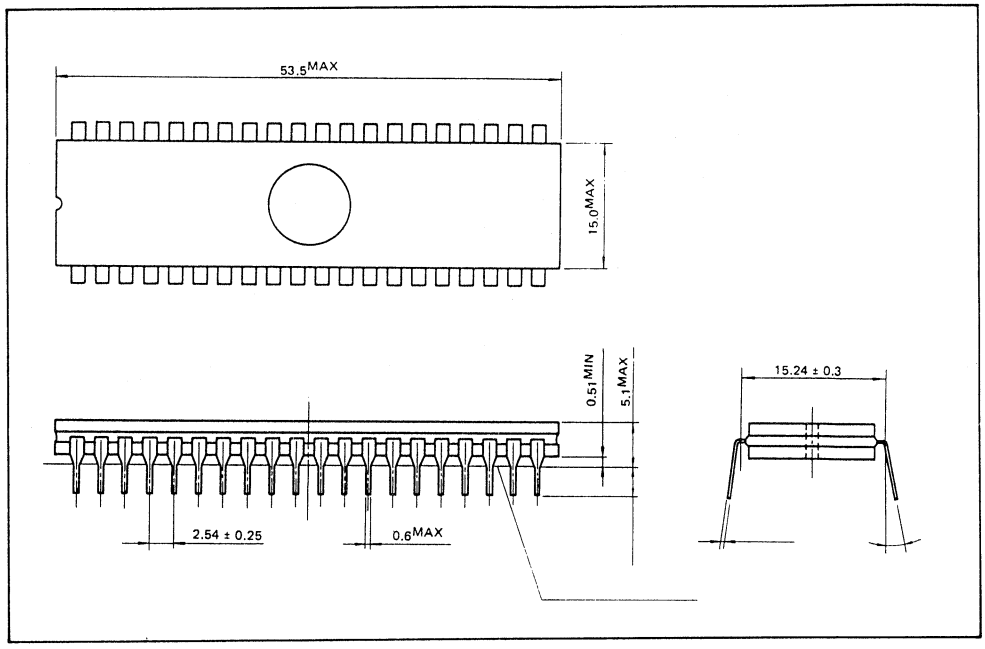
• 20 PIN PLASTIC DIP



• 32 PIN CERDIP



• 40 PIN CERDIP



RELIABILITY INFORMATION

3

3 RELIABILITY INFORMATION

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2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS 57
3. EXAMPLE OF RELIABILITY TEST RESULTS 60
4. SEMICONDUCTOR MEMORY FAILURES 64

RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

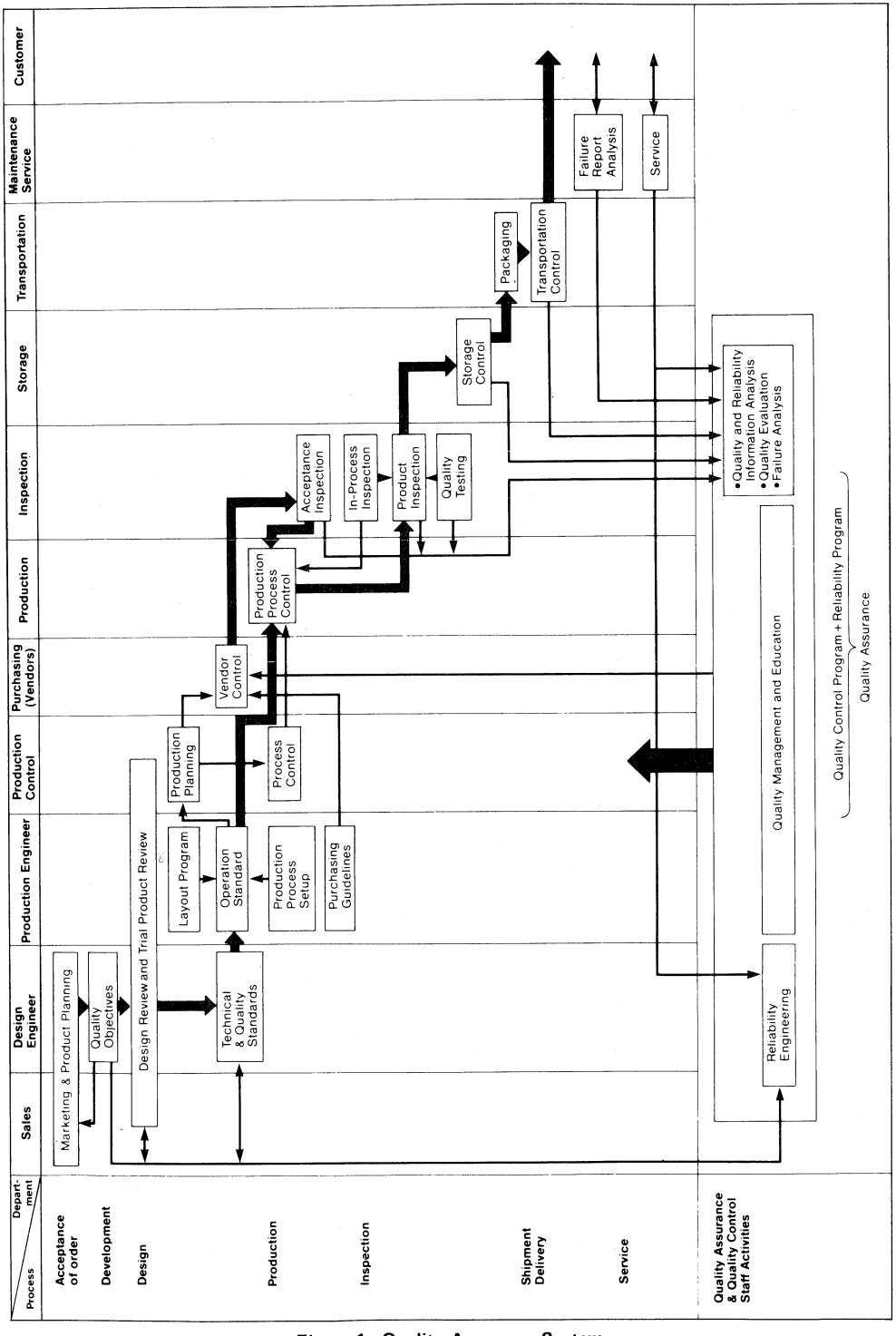


Figure 1 Quality Assurance System

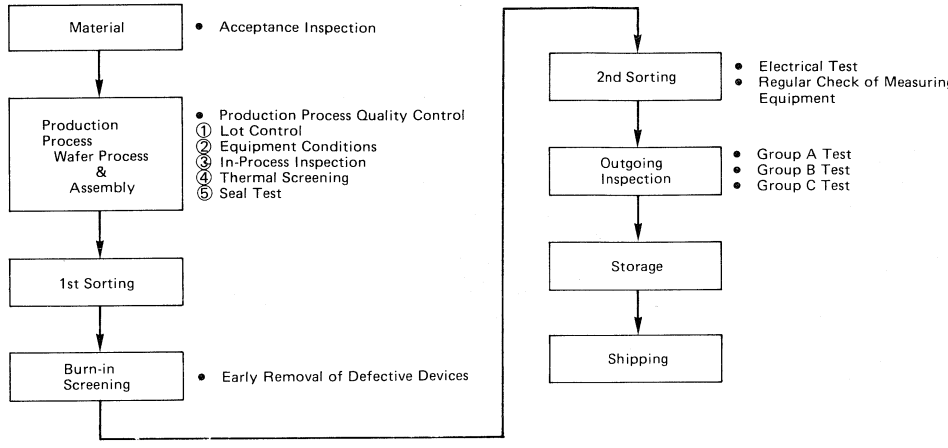


Figure 2 Manufacturing Process

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

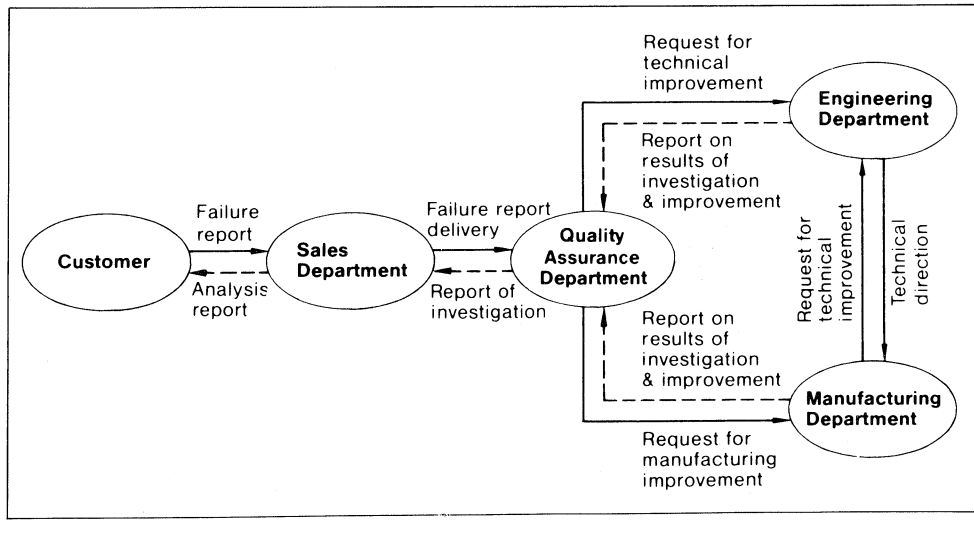
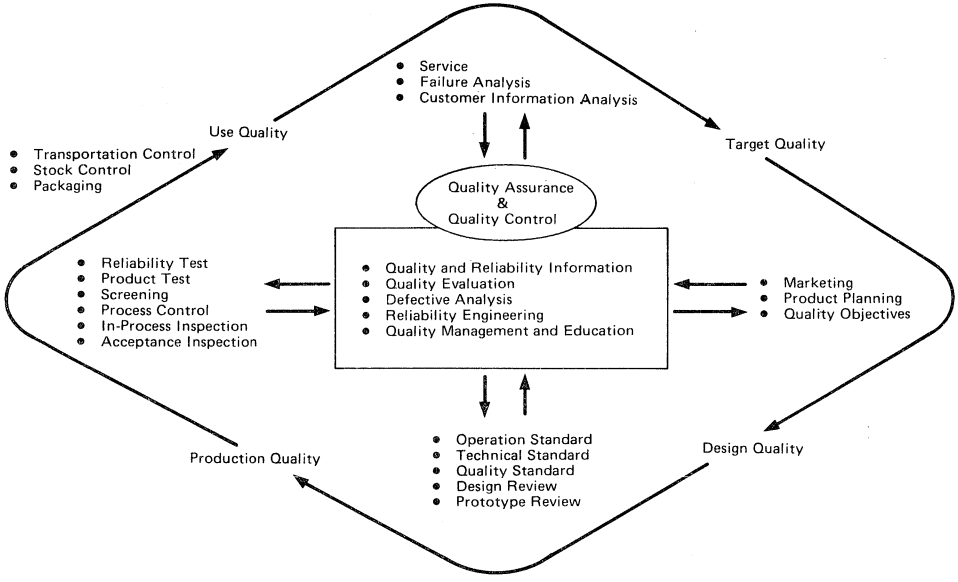


Figure 3 Failure report process



3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.

By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in LSI elements and their analysis are described on next page.

OKI MEMORY LSI LIFE TEST RESULTS

Test item	Test condition	Device name	MSM411000RS			MSM41256ARS			MSC2304AKS		
		Function	1048576 x 1 bit DYNAMIC RAM			262144 x 1 bit DYNAMIC RAM			262144 x 9 bit DYNAMIC RAM		
		Structure	Si gate N-MOS 18P plastic package			Si gate N-MOS 16P plastic package			Si gate N-MOS 30P sip		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V		300	2000	1*	500	2000	0	40	1000	0
	Ta = 150°V Vcc = 5.5V		45	2000	0	45	4000	0	–	–	–
Temperature humidity test	130°C 85% Vcc = 5.5V		100	120	0	100	120	0	–	–	–
	85°C 85% Vcc = 5.5V		100	2000	0	300	2000	0	40	1000	0
Pressure cooker test	121°C 100% No bias		50	500	0	100	500	0	–	–	–
Low temperature life test	Ta = –55 ~ –10°C Vcc = 7.0V		22	2000	0	60	2000	0	–	–	–
Temperature cycling test	–55°C ~ 25°C ~ 150°C (70min/cycle)		100	500 cycles	0	200	1000 cycles	0	40	2000 cycles (0 ~ 125°C) (20min/C)	0

Test item	Test condition	Device name	MSM51257RS			MSM27512AS			MSM531000RS		
		Function	32768 x 8 bit STATIC RAM			65536 x 8 bit UV erasable EP ROM			131072 x 8 bit Mask ROM		
		Structure	Si gate C-MOS 28P plastic package			Si gate N-MOS 28P cerdip			Si gate C-MOS 28P plastic package		
			Sample size	Test hours	Failures	Sample size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V		45	1000	0	88	2000	0	88	2000	0
	Ta = 150°C Vcc = 5.5V		–	–	–	–	–	–	–	–	–
Temperature humidity test	130°C 85% Vcc = 5.5V		22	120	0	–	–	–	22	120	0
	85°C 85% Vcc = 5.5V		50	1000	0	50	1000	0	80	2000	0
Pressure cooker test	121°C 100% No bias		50	500	0	–	–	–	50	200	0
Low temperature life test	Ta = –55 ~ –10°C Vcc = 7.0V		22	1000	0	22	2000	0	22	2000	0
Temperature cycling test	–55°C ~ 25°C 150°C (70min/cycle)		45	500 cycles	0	50	300 cycles	0	100	300 cycles	0

*: SINGLE BIT FAIL

OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

Test item		Test condition	MSM411000RS Sample size	MSM411000RS Failures	MSM41256ARS Sample size	MSM41256ARS Failures	MSC2304AKS Sample size	MSC2304AKS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	** 22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	20000G 1 min in each X, Y, Z					—	—
Electrical Environmental test	ESD	200pF, 0Ω, 5 times ±200V	10	0	10	0	—	—

Test item		Test condition	MSM51257RS Sample size	MSM51257RS Failures	MSM27512AS Sample size	MSM27512AS Failures	MSM531000RS Sample size	MSM531000RS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	200pF, 0Ω, 5 times ±200V	10	0	10	0	10	0

**: TEMPERATURE CYCLING: −40°C ~ 25°C ~ 125°C (20 cycles)
(30 min) (30 min)

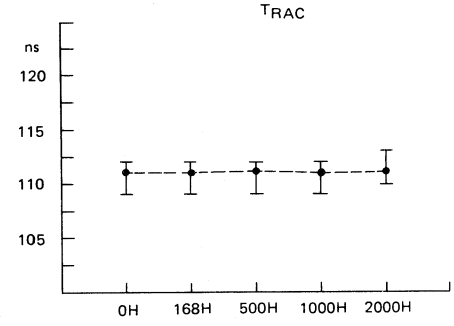
HIGH TEMPERATURE OPERATING LIFE TEST

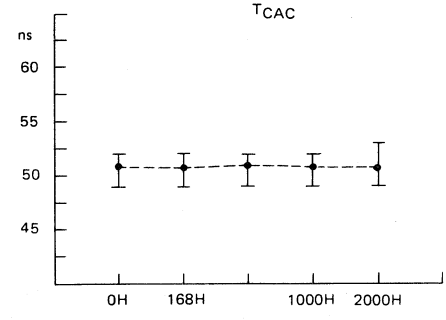
(Ta = 125°C, V_{CC} = 5.5V, t_{cycle} = 3 μs)

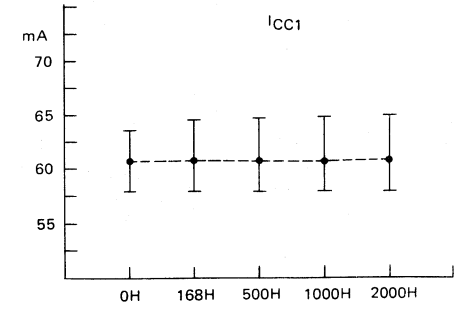
SAMPLE SIZE = 300 pcs.

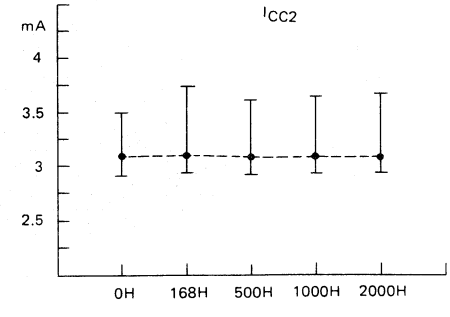
MSM41256-12RS

		0H	168H	500H	1000H	2000H	
I_{CC1} mA	MAX.	63.54	64.58	64.70	64.86	64.98	
	MIN.	57.92	57.94	57.86	57.90	57.96	
	MEAN	60.700	60.710	60.620	60.700	60.740	
	S.D.	1.339	1.370	1.376	1.389	1.394	
	DEL.	0.00	1.04	1.16	1.32	1.44	
I_{CC2} mA	MAX.	3.50	3.74	3.62	3.66	3.68	
	MIN.	2.92	2.94	2.92	2.94	2.94	
	MEAN	3.083	3.097	3.068	3.084	3.084	
	S.D.	.113	.144	.119	.119	.120	
	DEL.	0.00	0.68	0.20	0.24	0.26	
T_{RAC} ns	MAX.	112	112	112	112	113	
	MIN.	109	109	109	109	110	
	MEAN	110.9	110.9	111.1	110.9	111.0	
	S.D.	.7	.7	.8	.7	.8	
	DEL.	0	−1	1	−1	−1	
T_{CAC} ns	MAX.	52	52	52	52	53	
	MIN.	49	49	49	49	49	
	MEAN	50.8	50.6	51.0	50.6	50.6	
	S.D.	.7	.6	.7	.6	.7	
	DEL.	0	−1	1	−1	−1	





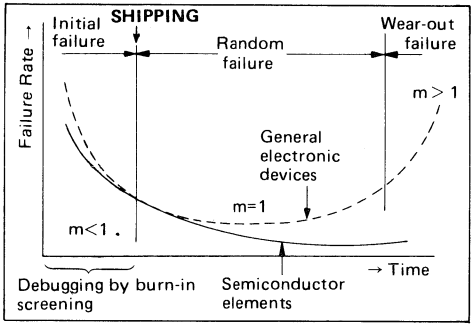




4. SEMICONDUCTOR MEMORY FAILURES

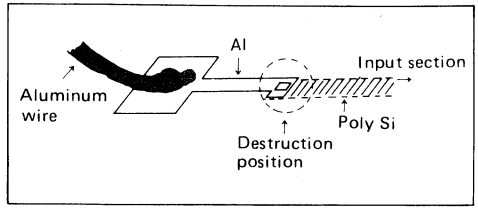
The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

Semiconductor Element Failure Rate Curve



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.
At Oki, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

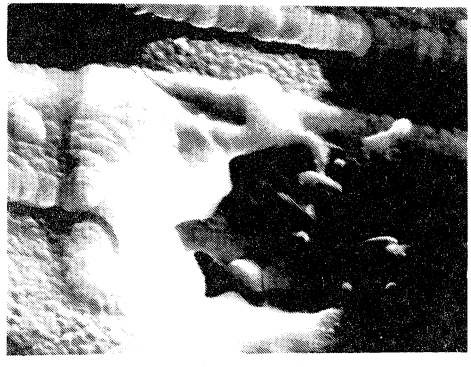
Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

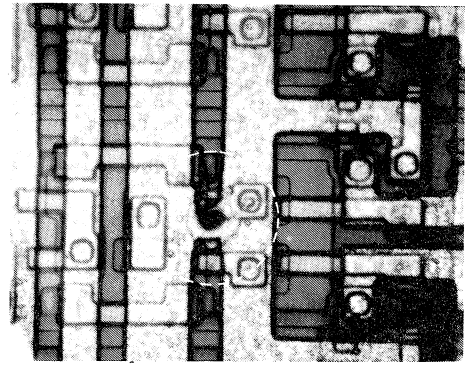
Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 cm through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.



Example of surge destruction



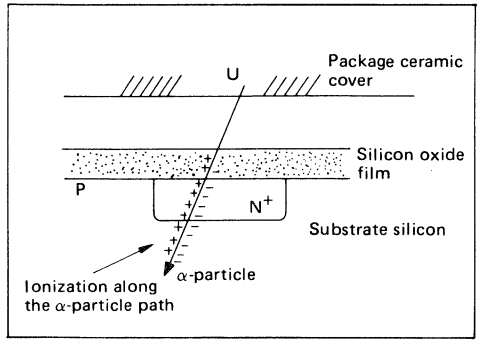
Photolithographic Defect

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

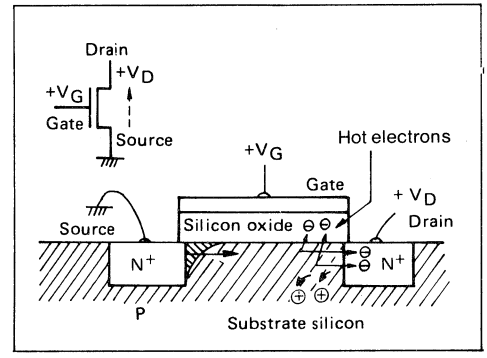
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

MOS DYNAMIC RAMS

4 MOS DYNAMIC RAMS

MSM3764AAS/JS	65,536-Word x 1-Bit RAM (NMOS)	67
MSM41256RS/JS	262,144-Word x 1-Bit RAM (NMOS) <Page Mode>	83
MSM41256ARS/JS	262,144-Word x 1-Bit RAM (NMOS) <Page Mode>	97
MSM41257ARS/JS	262,144-Word x 1-Bit RAM (NMOS) <Nibble Mode>	112
MSM41464RS/JS	65,536-Word x 4-Bit RAM (NMOS)	128
MSM414256RS	262,144-Word x 4-Bit RAM (NMOS)	143
MSM411000RS	1,048,576-Word x 1-Bit RAM (NMOS)	156
MSM411001RS	1,048,576-Word x 1-Bit RAM (NMOS) <Nibble Mode>	169
MSM511000RS	1,048,576-Word x 1-Bit RAM (CMOS) <Fast Page>	182
MSM511001RS	1,048,576-Word x 1-Bit RAM (CMOS) <Static Column>	197
MSM511002RS	1,048,576-Word x 1-Bit RAM (CMOS) <Static Column>	212
MSM514256RS	262,144-Word x 4-Bit RAM (CMOS) <Fast Page>	225
MSM514258RS	262,144-Word x 4-Bit RAM (CMOS) <Static Column>	238
MSC2304YS8/KS8	262,144-Word x 8-Bit RAM (NMOS)	252
MSC2304YS9/KS9	262,144-Word x 9-Bit RAM (NMOS)	267
MSC2307YS9/KS9	262,144-Word x 9-Bit RAM (NMOS) <Nibble Mode>	282
MSC2305YS18A	524,288-Word x 9-Bit RAM (NMOS) <Page Mode>	297
MSC2310YS9/KS9	1,048576-Word x 9-Bit RAM (NMOS)	310
MSC2311YS8/KS8	1,048576-Word x 8-Bit RAM (NMOS)	322

OKI semiconductor

MSM3764 ARS/JS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out.

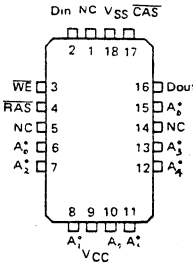
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

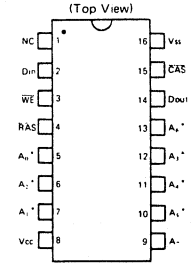
- 65,536 x 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
- Cycle time,
  220 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
- Low power: 330 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

PIN CONFIGURATION



Pin Names	Function
A_0 ~ A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address



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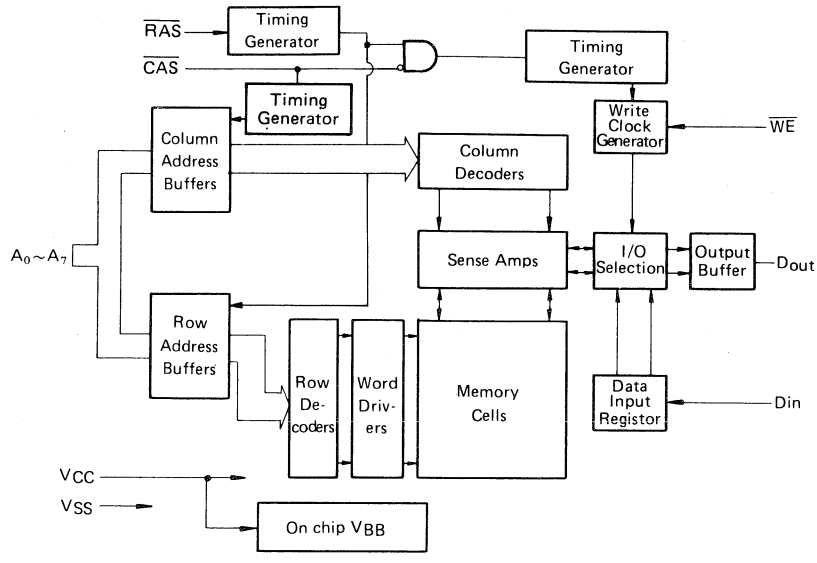
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	−1.0	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	–	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	8	pF
Output Capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

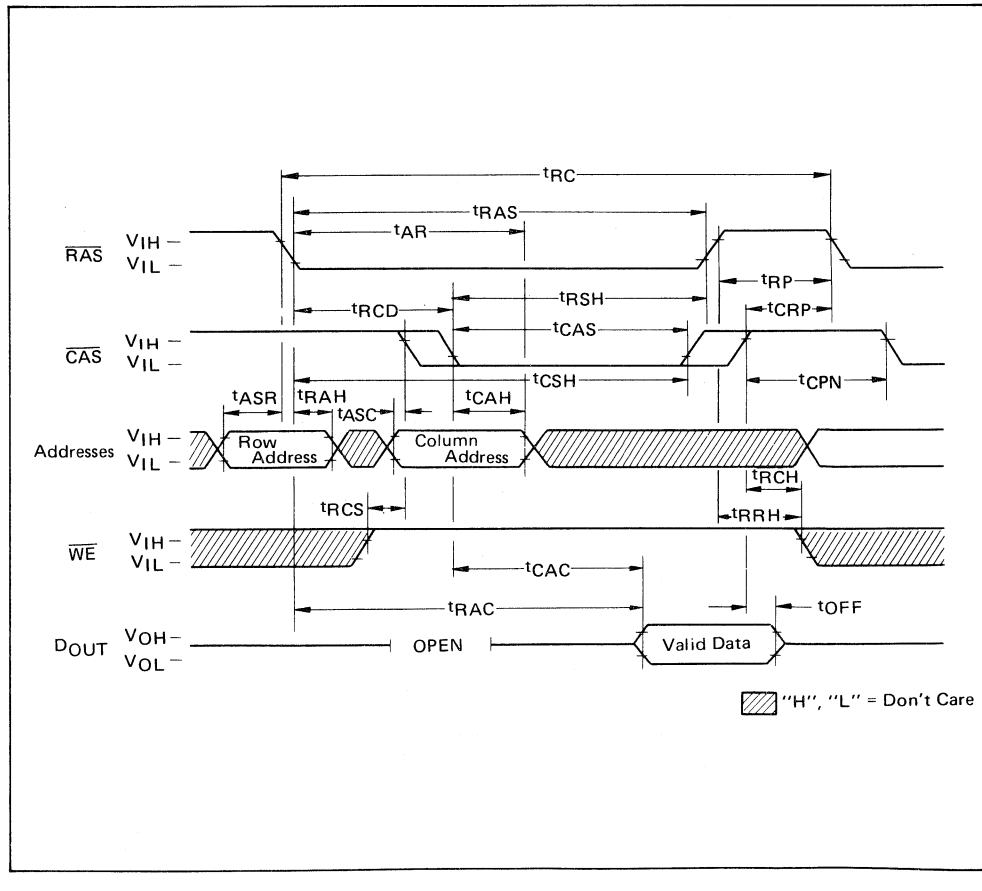
(Recommended operating conditions unless otherwise noted.) Note 1,2,3

Parameter	Symbol	Units	MSM3764A-12		MSM3764A-15		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	220		260		
Read-write cycle time	t_{RWC}	ns	245		280		
Page mode cycle time	t_{PC}	ns	120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	
Transition time	t_T	ns	3	35	3	35	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	ns	50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		15		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	20		20		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	80		95		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		45		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	0		0		
$\overline{CAS}$ precharge time	t_{CPN}	ns	30		35		

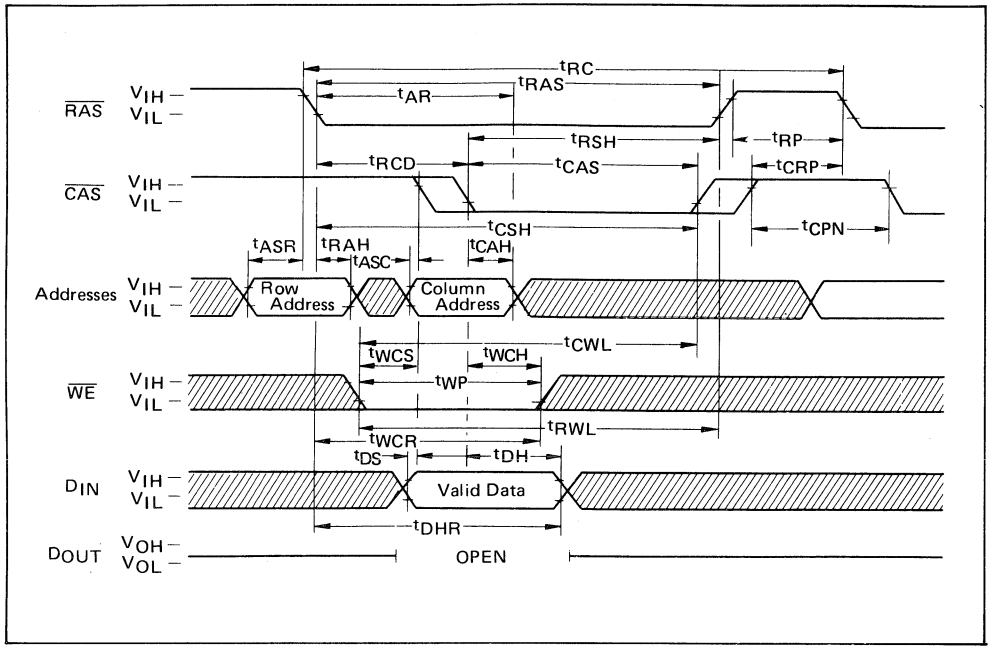
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

4

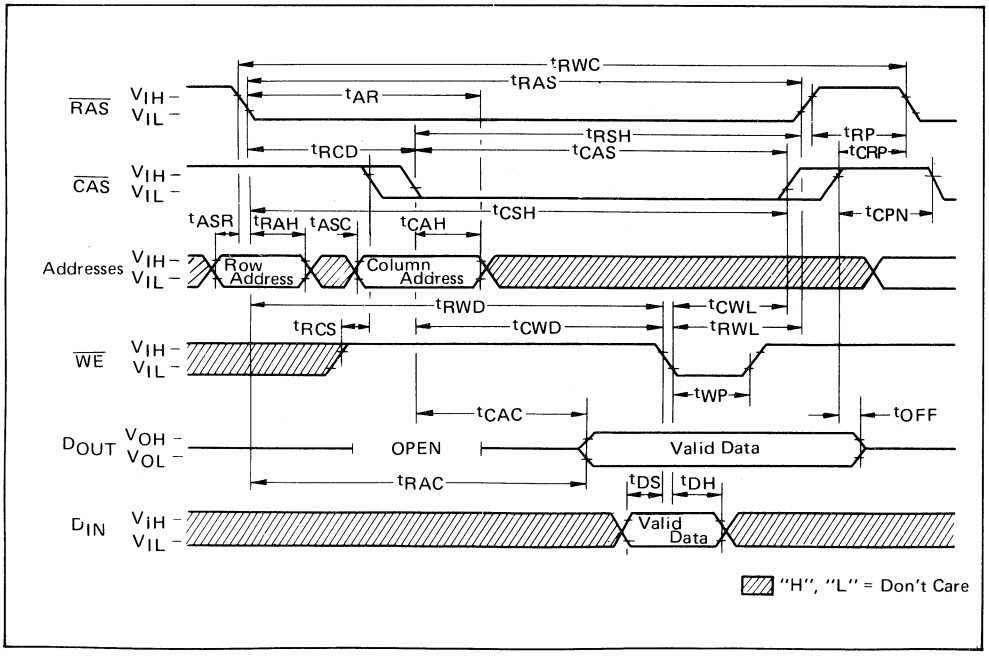
READ CYCLE TIMING



WRITE CYCLE TIMING
(EARLY WRITE)

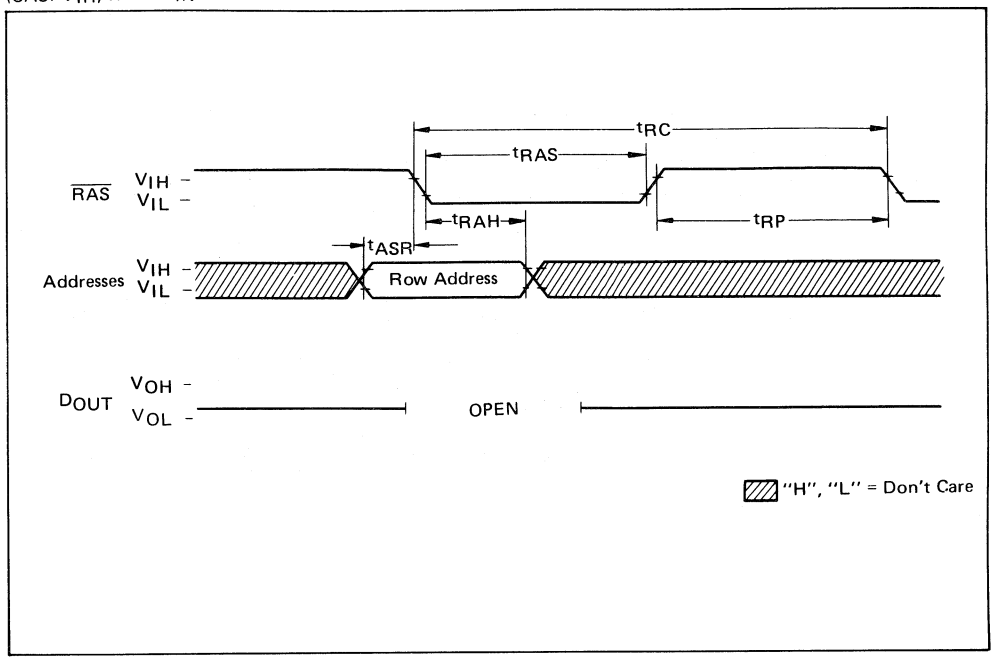


READ-WRITE/READ-MODIFY-WRITE CYCLE

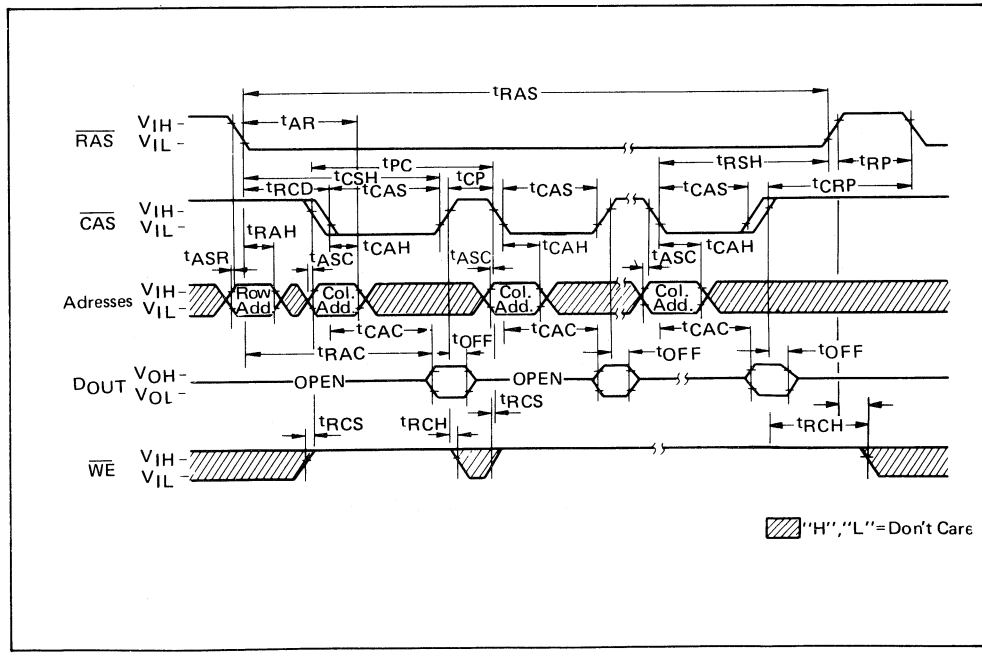


$\overline{RAS}$ ONLY REFRESH TIMING

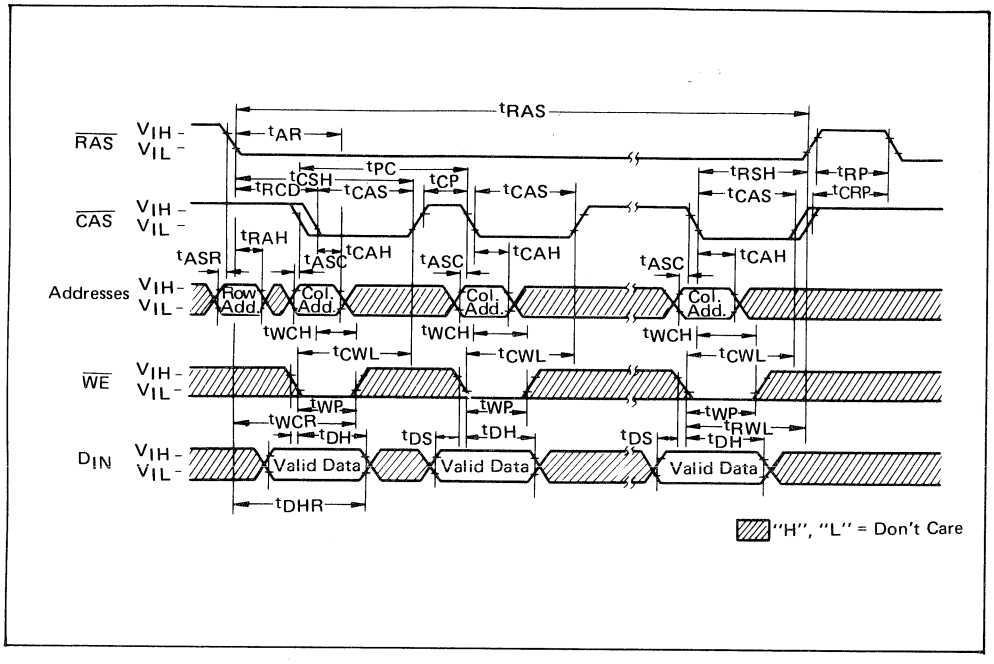
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



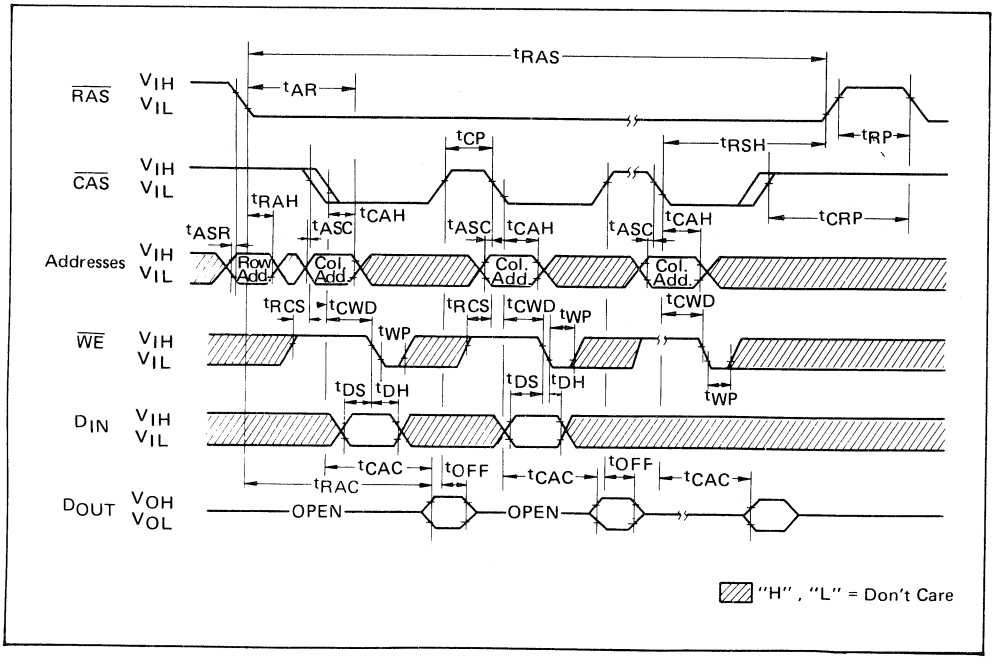
PAGE MODE READ CYCLE



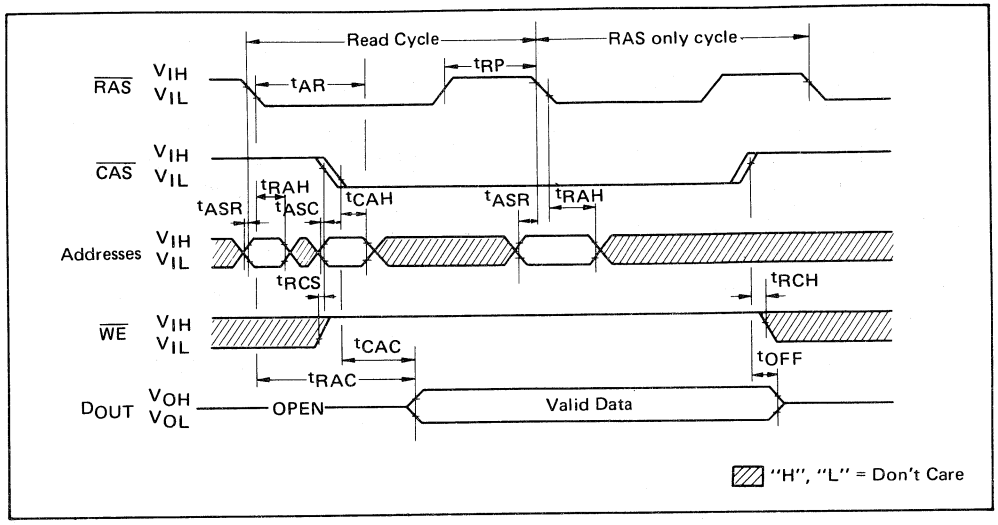
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

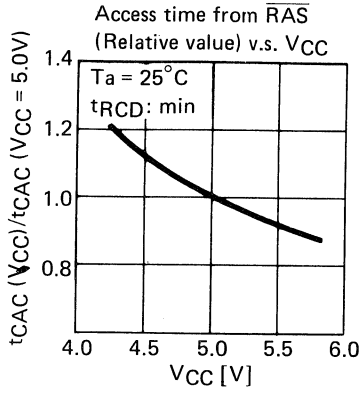
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

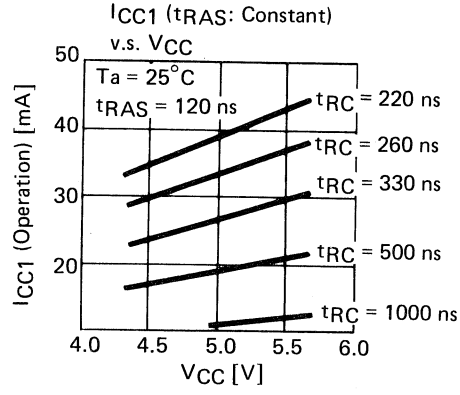
Hidden Refresh:

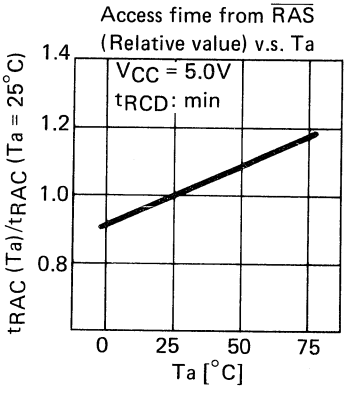
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

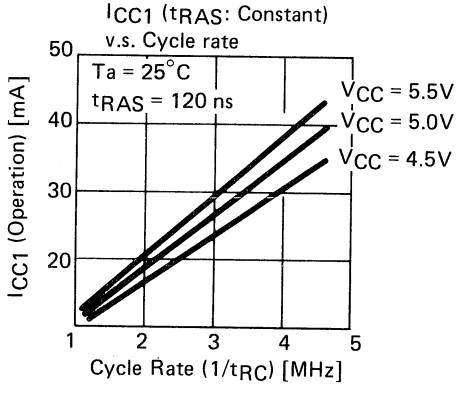
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

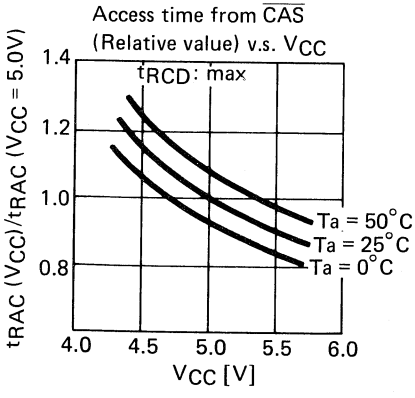
TYPICAL CHARACTERISTICS

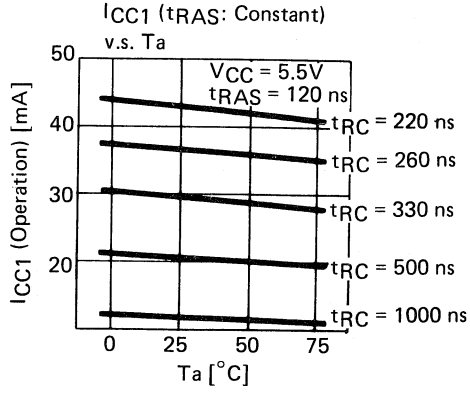


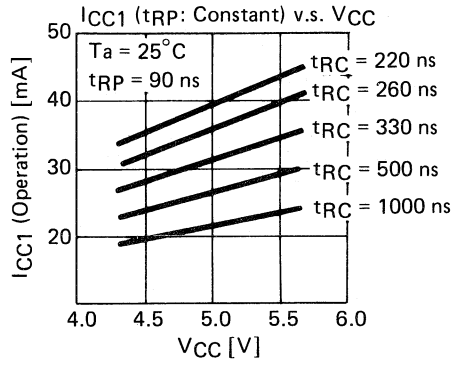


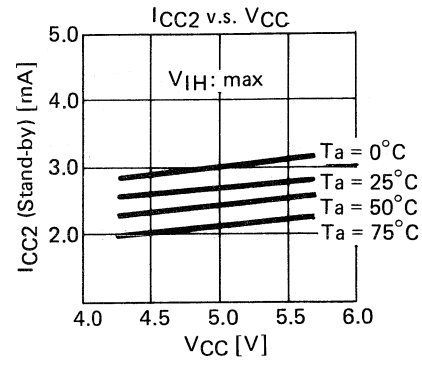


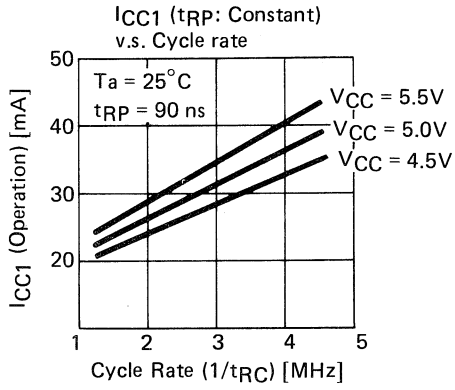


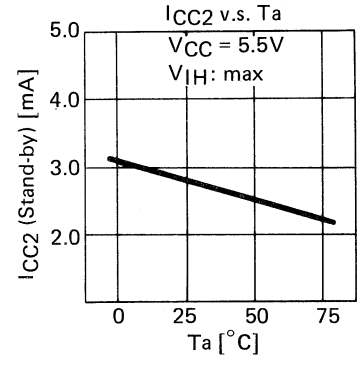


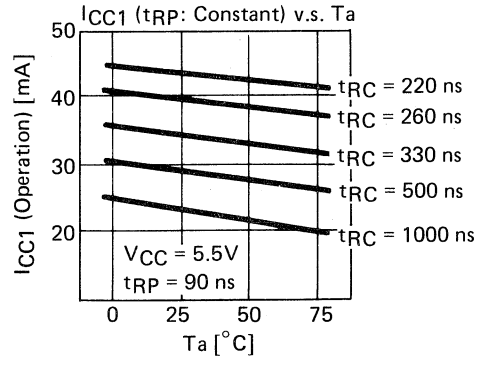


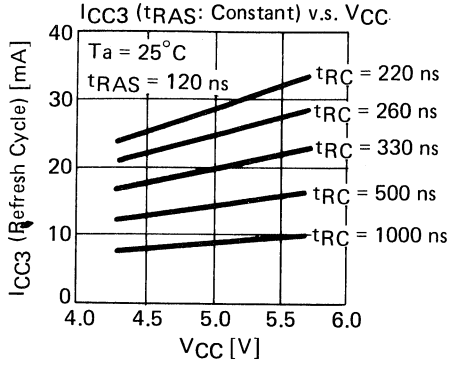

ICC1 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC1 (Operation) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]

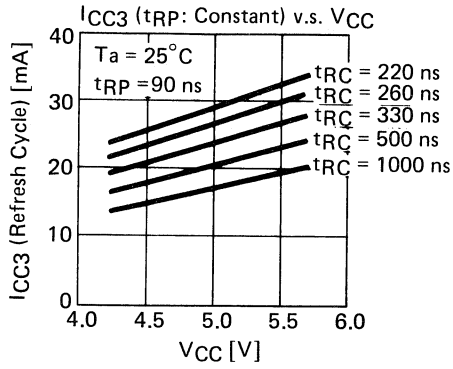

ICC2 v.s. VCC
VIH: max
Ta = 0°C
Ta = 25°C
Ta = 50°C
Ta = 75°C
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
4.0
4.5
5.0
5.5
6.0
VCC [V]

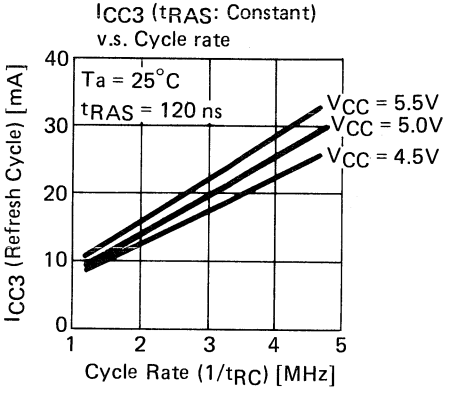

ICC1 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC1 (Operation) [mA]
50
40
30
20
1
2
3
4
5
Cycle Rate (1/tRC) [MHz]

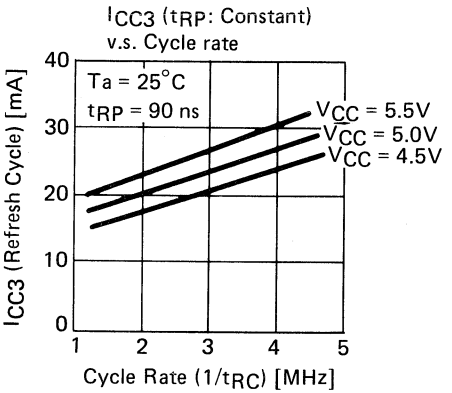

ICC2 v.s. Ta
VCC = 5.5V
VIH: max
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
0
25
50
75
Ta [°C]

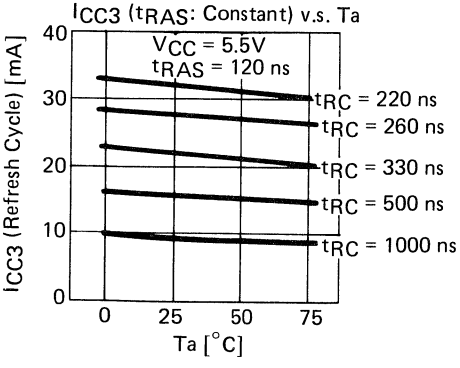

ICC1 (tRP: Constant) v.s. Ta
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
VCC = 5.5V
tRP = 90 ns
ICC1 (Operation) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

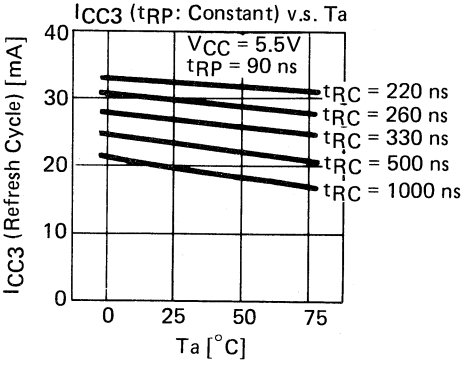

ICC3 (tRAS: Constant) v.s. VCC
Ta = 25°C
tRAS = 120 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
VCC [V]


ICC3 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
VCC [V]

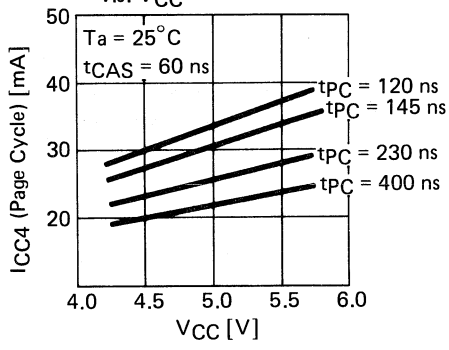

ICC3 (tRAS: Constant)
v.s. Cycle rate
Ta = 25°C
tRAS = 120 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC3 (Refresh Cycle) [mA]
Cycle Rate (1/tRC) [MHz]


ICC3 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC3 (Refresh Cycle) [mA]
Cycle Rate (1/tRC) [MHz]

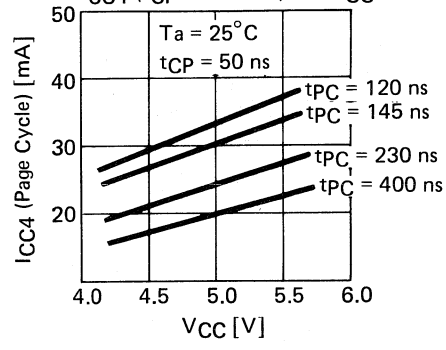

ICC3 (tRAS: Constant) v.s. Ta
VCC = 5.5V
tRAS = 120 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
Ta [°C]


ICC3 (tRP: Constant) v.s. Ta
VCC = 5.5V
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
Ta [°C]

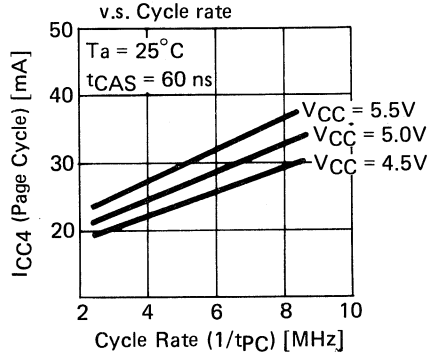
I_{CC4} (t_{CAS}: Constant) v.s. V_{CC}



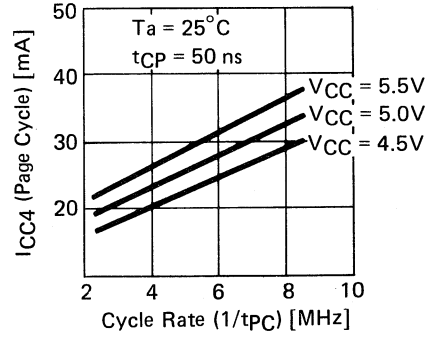
I_{CC4} (t_{CP}: Constant) v.s. V_{CC}



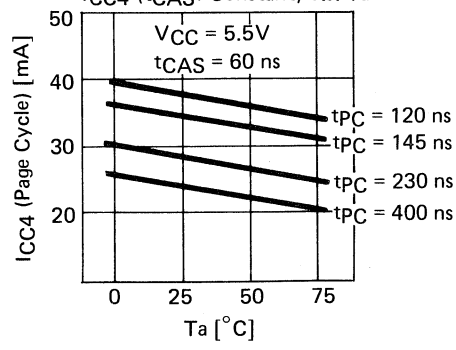
I_{CC4} (t_{CAS}: Constant) v.s. Cycle rate



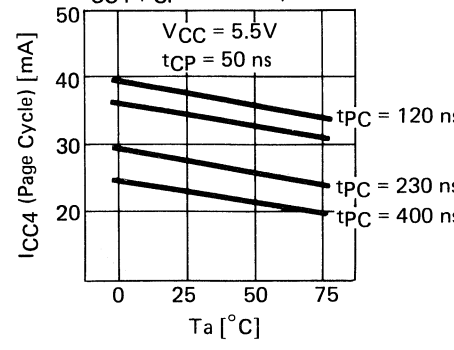
I_{CC4} (t_{CP}: Constant) v.s. Cycle rate



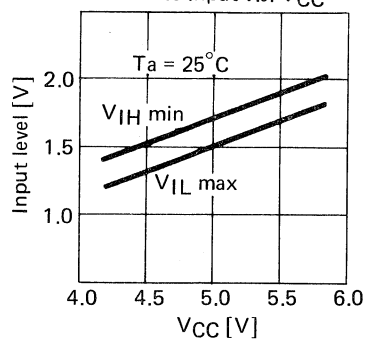
I_{CC4} (t_{CAS}: Constant) v.s. Ta



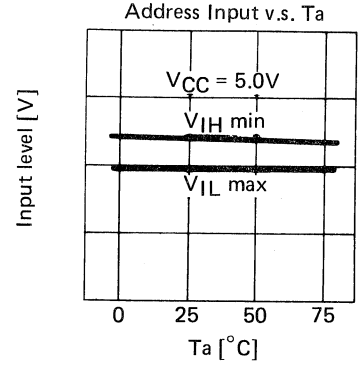
I_{CC4} (t_{CP}: Constant) v.s. Ta



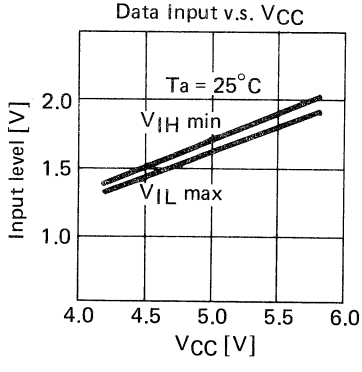
Address Input v.s. V_{CC}



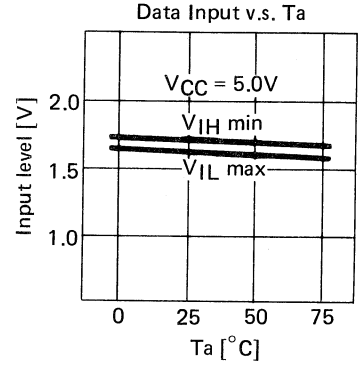
Address Input v.s. Ta



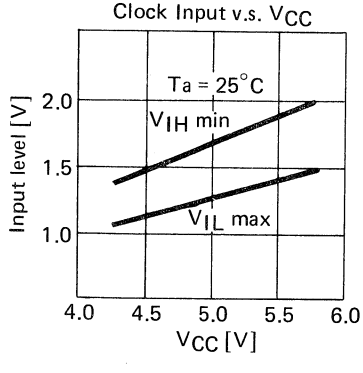
Data Input v.s. V_{CC}



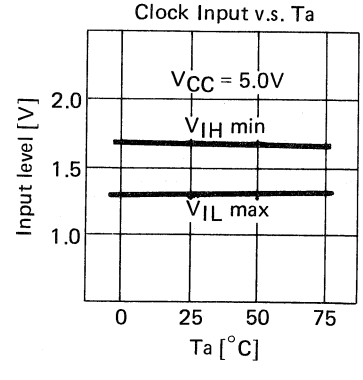
Data Input v.s. Ta



Clock Input v.s. V_{CC}

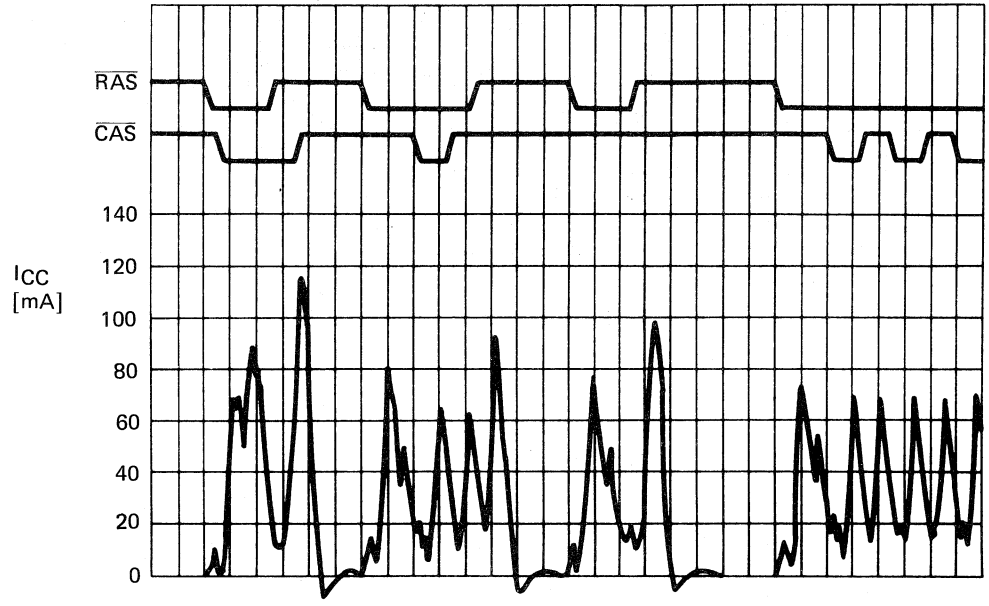


Clock Input v.s. Ta

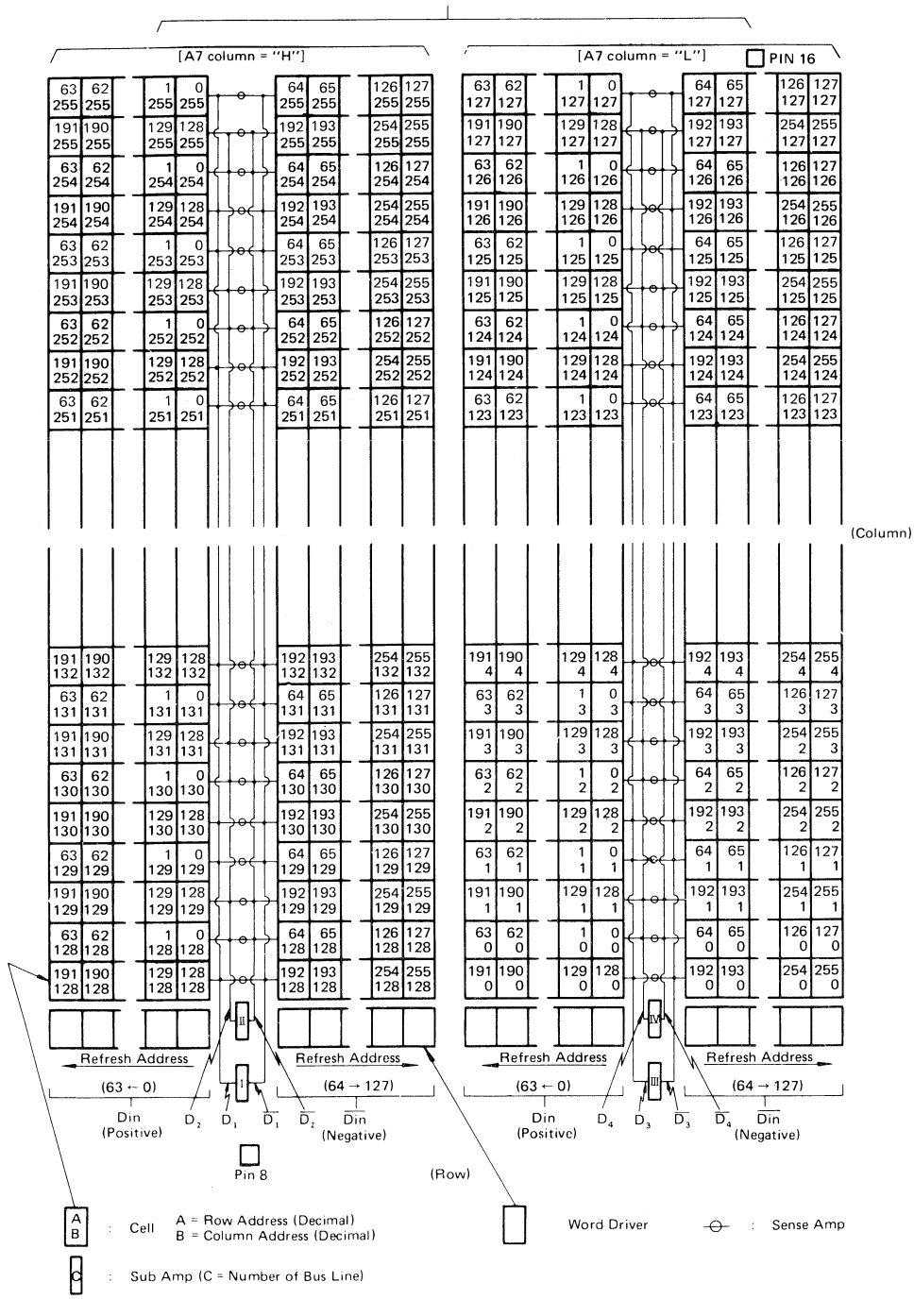


V_{CC} = 5.5V
Ta = 25°C
50 ns/div

RAS/CAS CYCLE, LONG RAS/CAS CYCLE, RASONLY CYCLE, PAGE MODE CYCLE



MSM3764A Bit MAP (Physical-Decimal)



OKI semiconductor

MSM41256RS/JS

262144-BIT DYNAMIC RANDOM ACCESS MEMORY < Page Mode Type >

GENERAL DESCRIPTION

The Oki MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 16-pin DIP or 18-pin PLCC. Pin-outs conform to the JEDEC approved pin out.

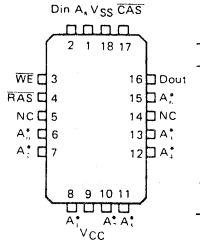
The MSM41256 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

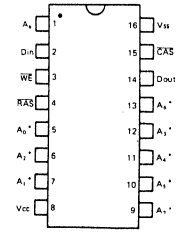
- 262144 x 1 RAM, 16-pin DIP or 18-pin PLCC package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max. (MSM41256-12)
  150 ns max. (MSM41256-15)
- Cycle time,
  230 ns min. (MSM41256-12)
  260 ns min. (MSM41256-15)
- Low power: 385 mW/360 mW active
  28 mW max. standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 4 ms/256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address



Pin Names	Function
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Din	Data Input
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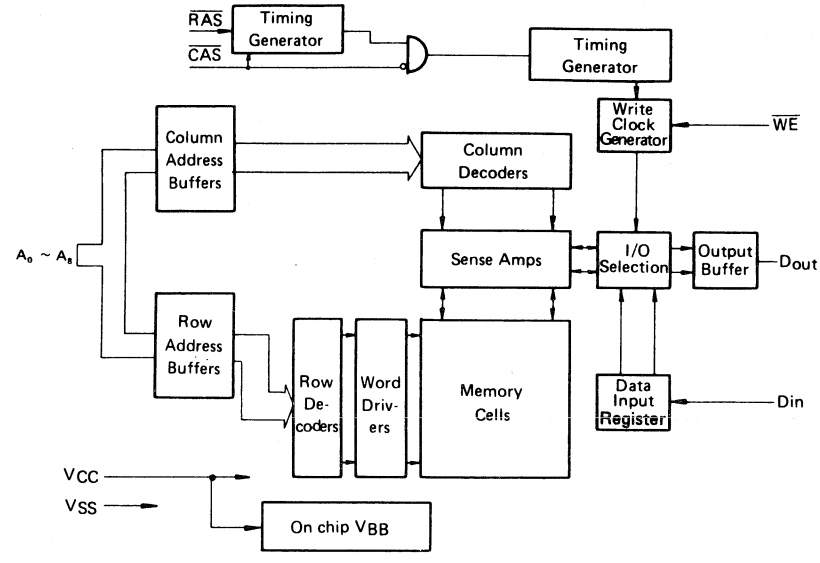
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Respect to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41256-12	I_{CC1}		70	mA
	MSM41256-15			65	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256-12	I_{CC3}		60	mA
	MSM41256-15			55	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256-12	I_{CC4}		60	mA
	MSM41256-15			55	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, (0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5 mA)		V_{OH}	2.4		V
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	7	pF

Note: Capacitance measured with Boonton Meter.

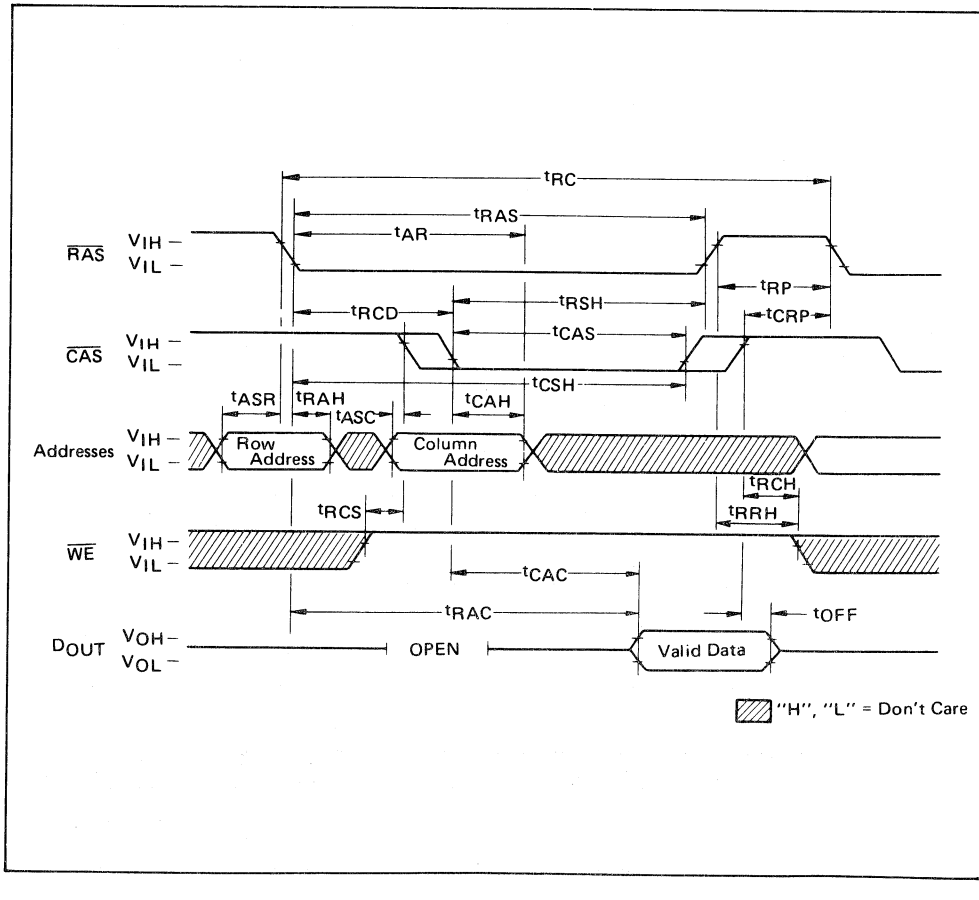
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM41256-12		MSM41256-15		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		
Read-write cycle time	t_{RWC}	ns	255		325		
Page mode cycle time	t_{PC}	ns	130		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	35		45		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		8
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		60		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		60		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		75		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		150		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		

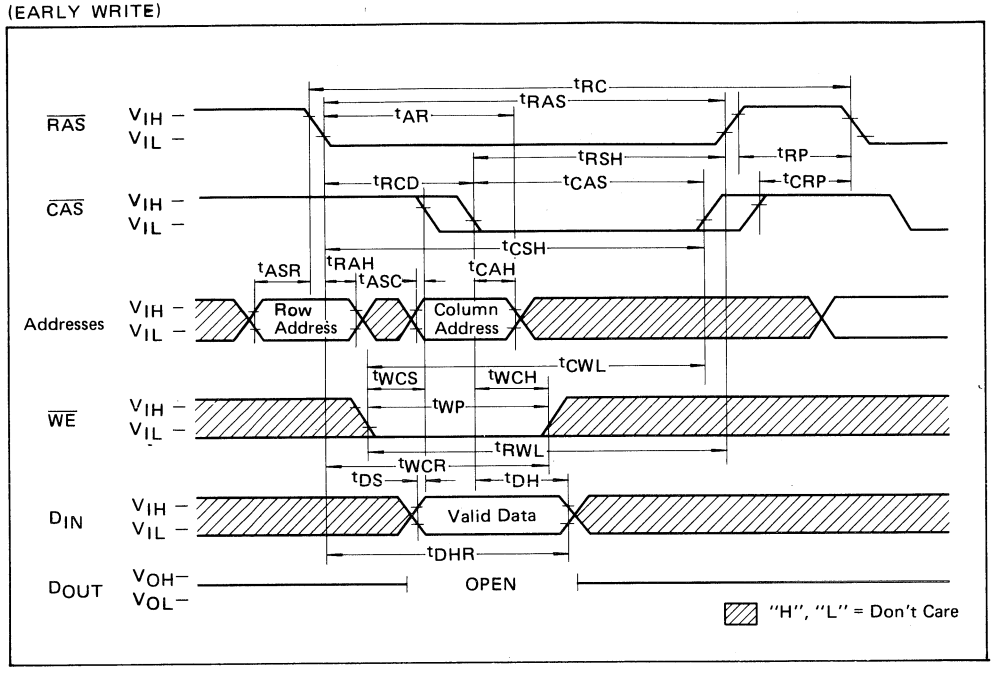
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

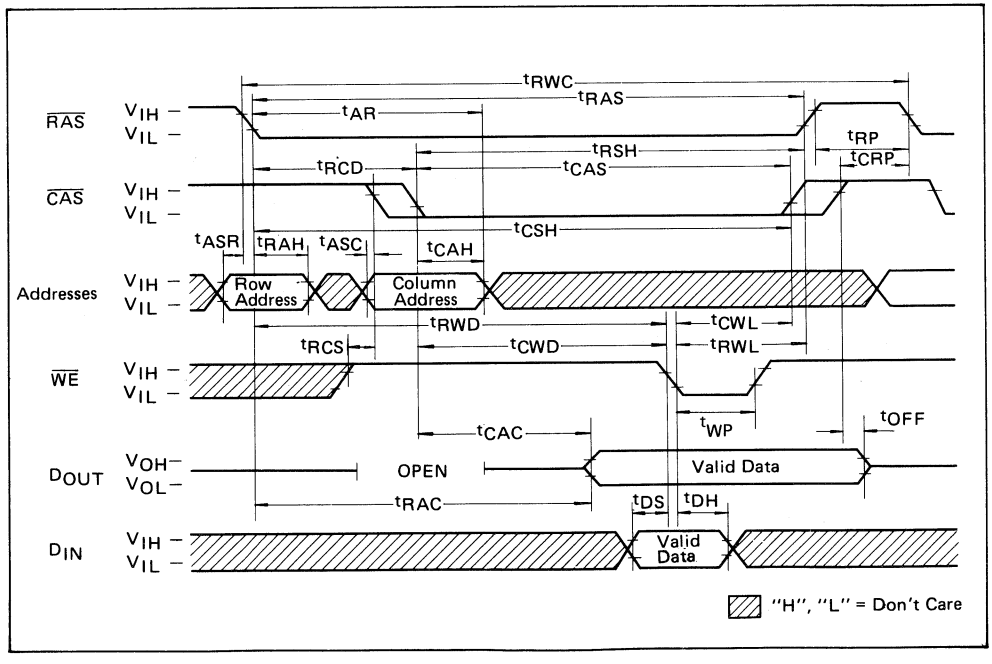


WRITE CYCLE TIMING

(EARLY WRITE)

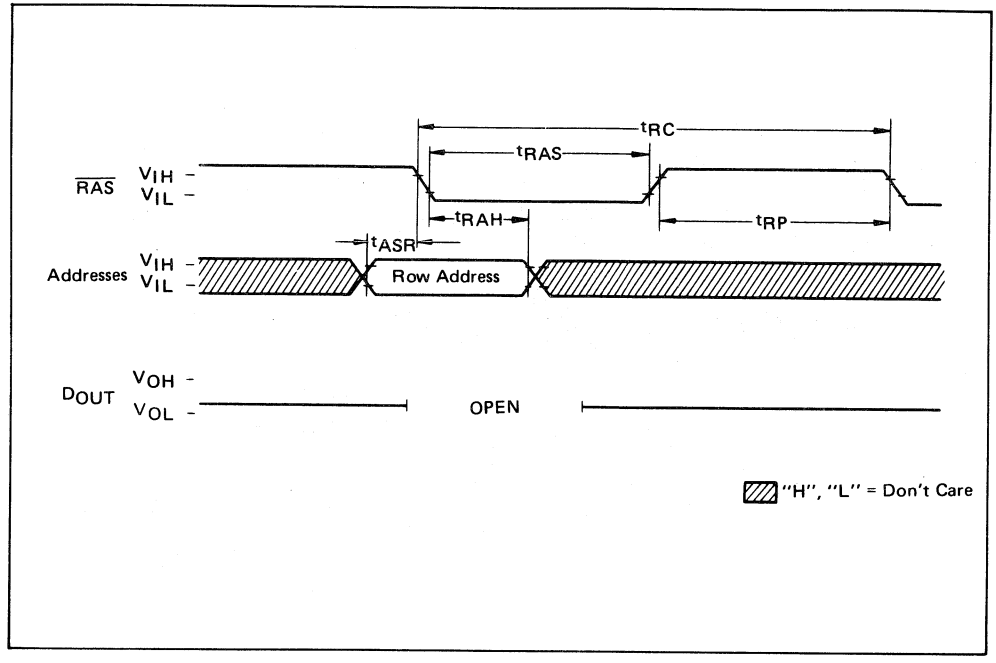


READ-WRITE/READ-MODIFY-WRITE CYCLE

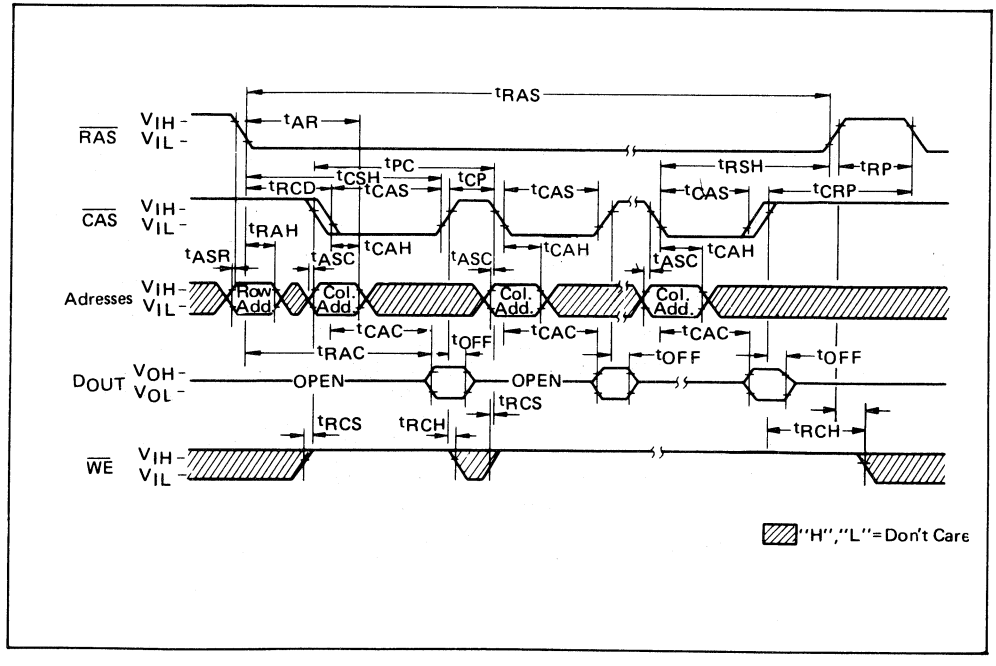


$\overline{RAS}$ ONLY REFRESH TIMING

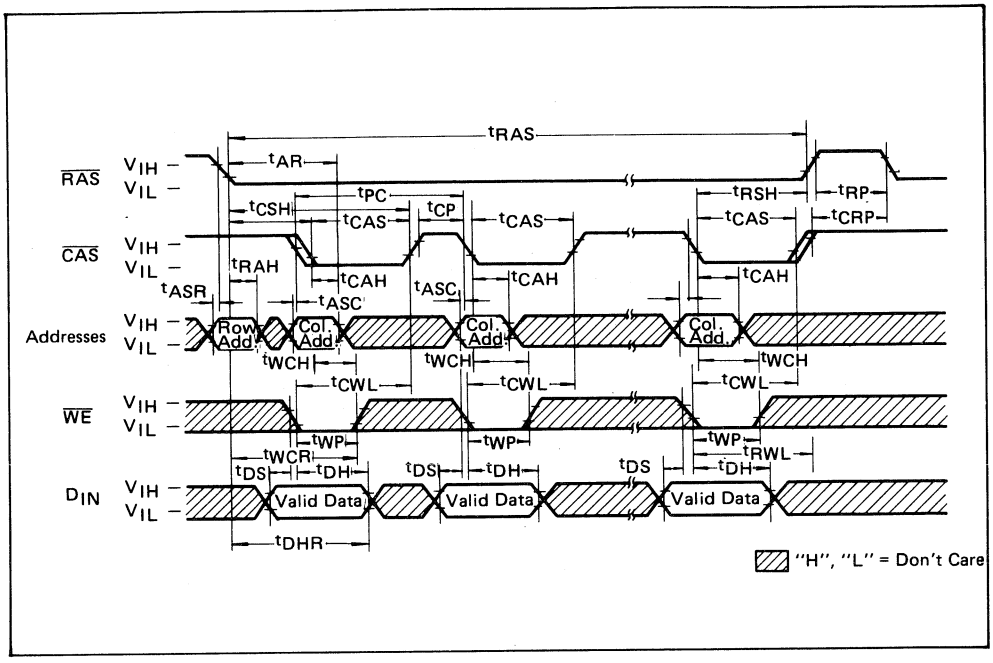
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



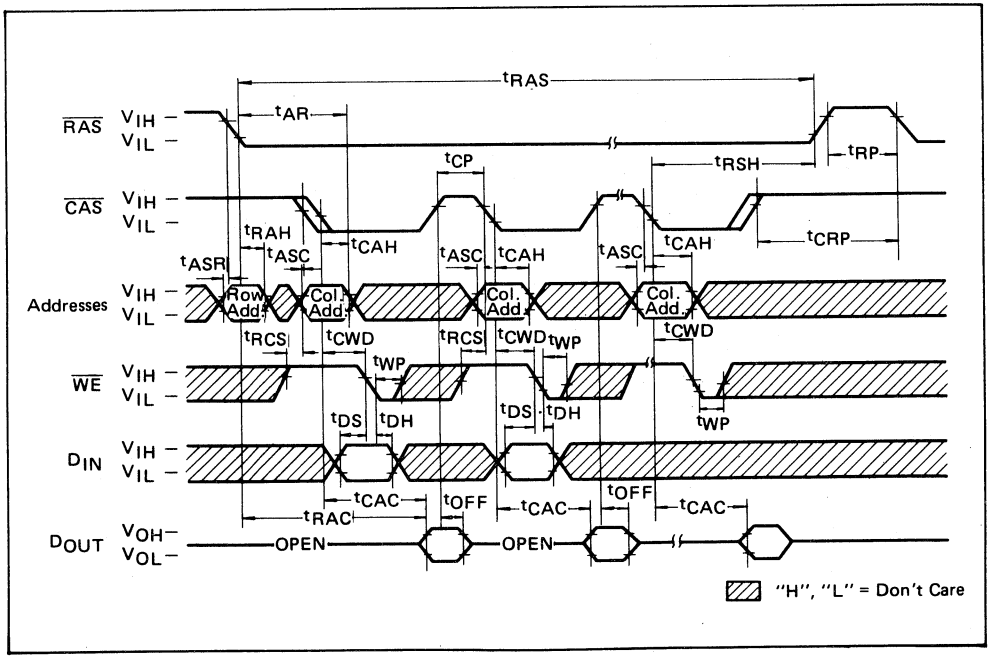
PAGE MODE READ CYCLE



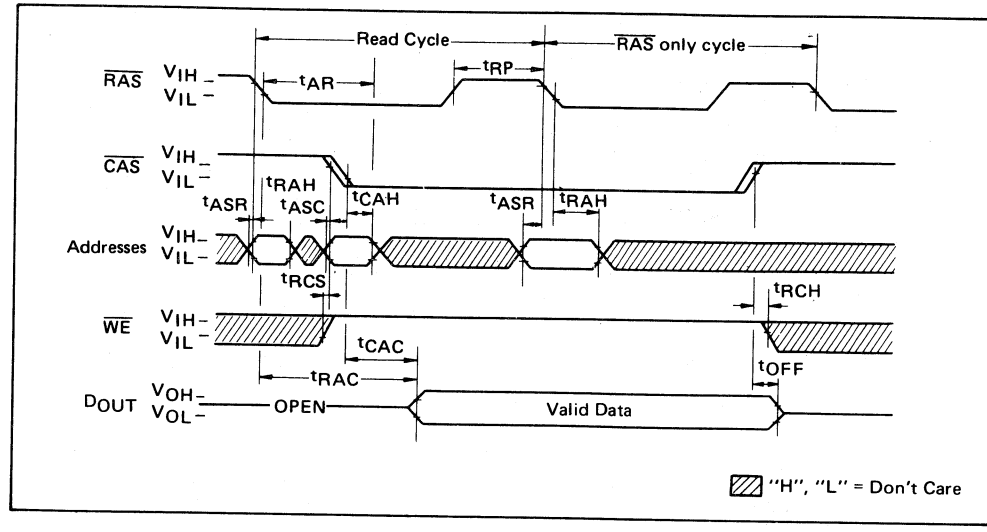
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSM41256 Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by RAS to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM41256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

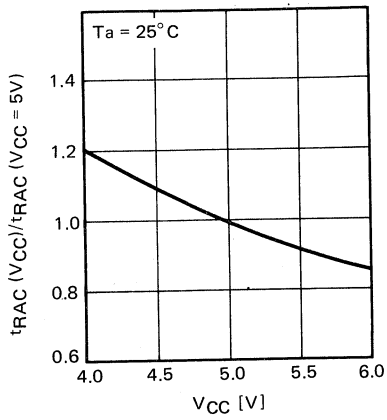
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

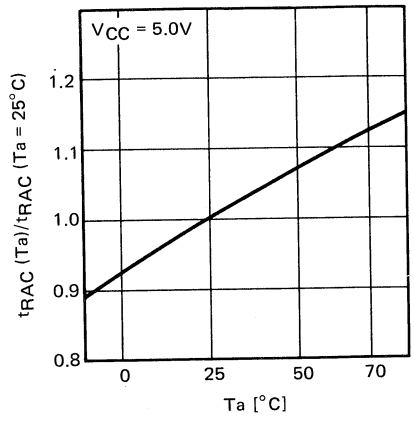
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

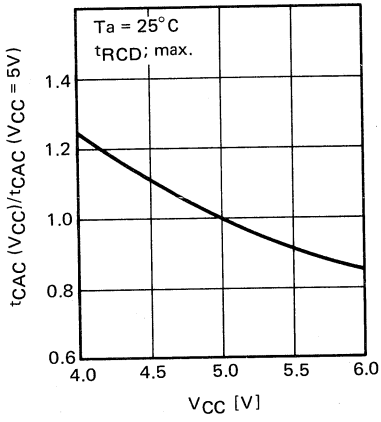
Access time from $\overline{RAS}$ (Relative value) vs. V_{CC}



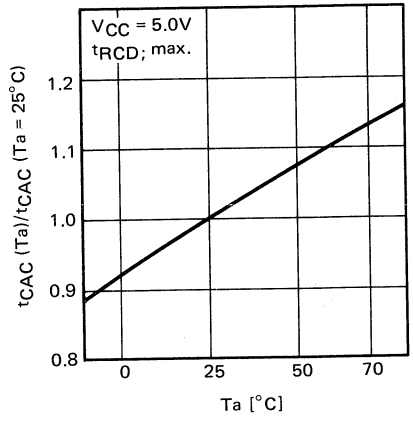
Access time from $\overline{RAS}$ (Relative value) vs. Ta



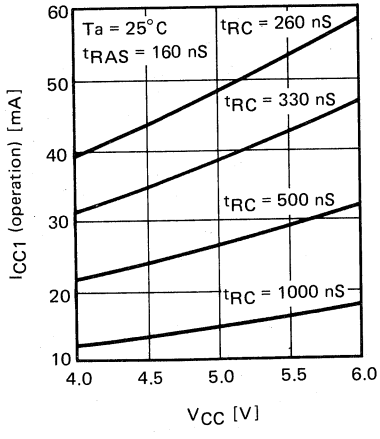
Access time from $\overline{CAS}$ (Relative value) vs. V_{CC}



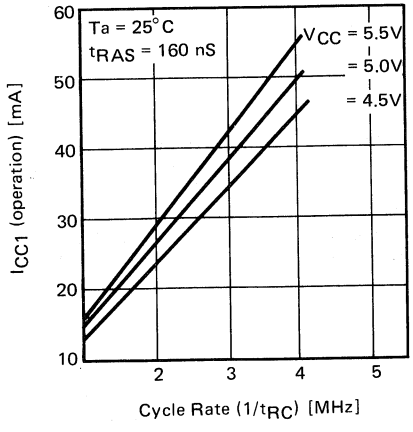
Access time from $\overline{CAS}$ (Relative value) vs. Ta

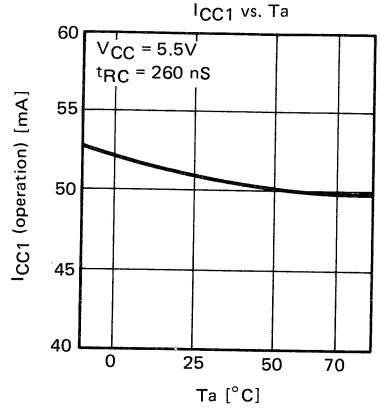


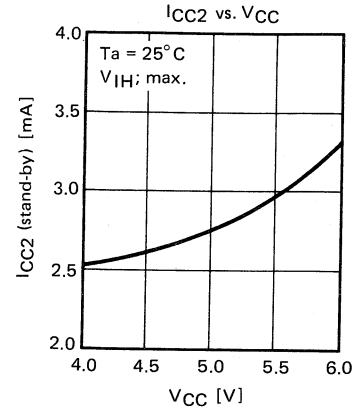
I_{CC1} vs. V_{CC}

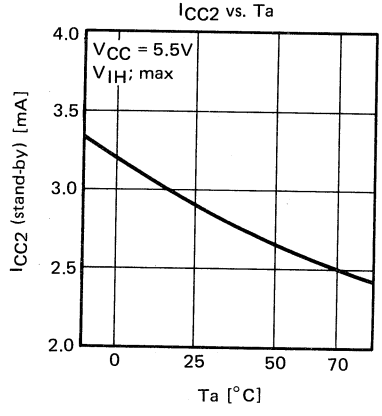


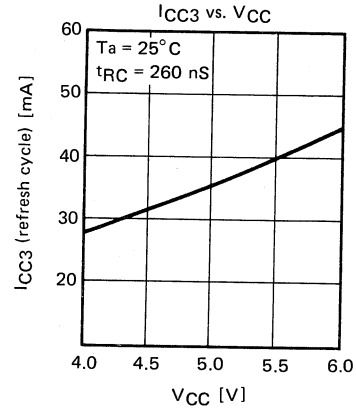
I_{CC1} vs. Cycle rate

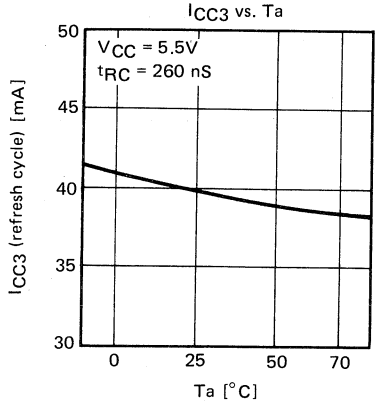


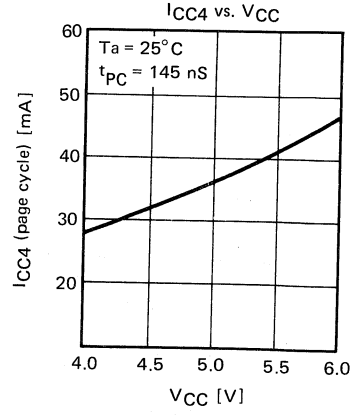

I_{CC1} vs. Ta
V_{CC} = 5.5V
t_{RC} = 260 nS
I_{CC1} (operation) [mA]
60
55
50
45
40
0
25
50
70
Ta [°C]

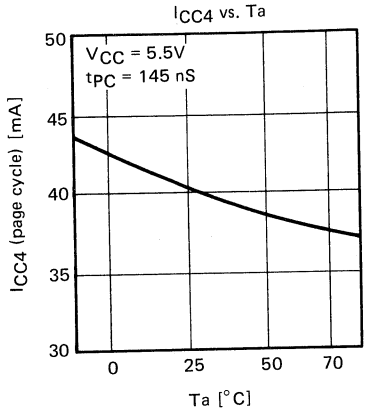

I_{CC2} vs. V_{CC}
Ta = 25°C
V_{IH}; max.
I_{CC2} (stand-by) [mA]
4.0
3.5
3.0
2.5
2.0
4.0
4.5
5.0
5.5
6.0
V_{CC} [V]

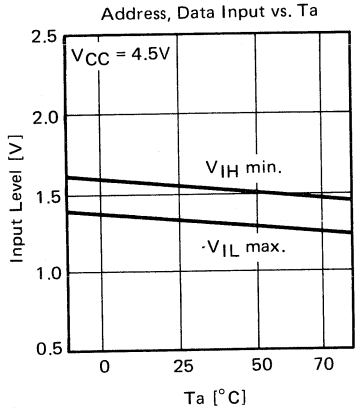

I_{CC2} vs. Ta
V_{CC} = 5.5V
V_{IH}; max
I_{CC2} (stand-by) [mA]
4.0
3.5
3.0
2.5
2.0
0
25
50
70
Ta [°C]

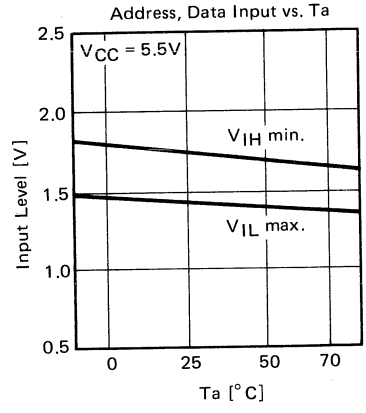

I_{CC3} vs. V_{CC}
Ta = 25°C
t_{RC} = 260 nS
I_{CC3} (refresh cycle) [mA]
60
50
40
30
20
4.0
4.5
5.0
5.5
6.0
V_{CC} [V]

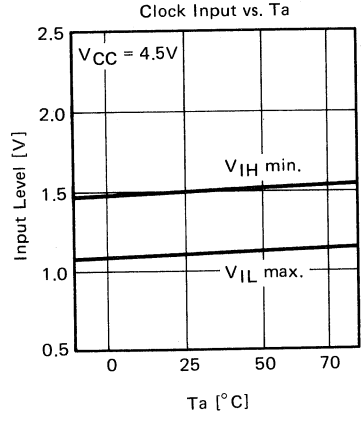

I_{CC3} vs. Ta
V_{CC} = 5.5V
t_{RC} = 260 nS
I_{CC3} (refresh cycle) [mA]
50
45
40
35
30
0
25
50
70
Ta [°C]

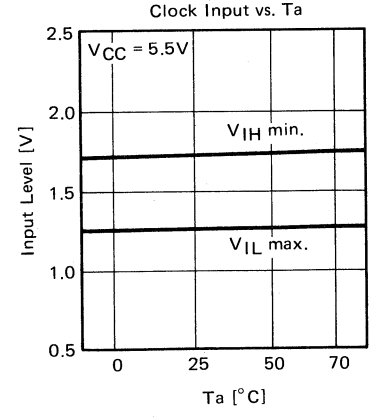

I_{CC4} vs. V_{CC}
Ta = 25°C
t_{PC} = 145 nS
I_{CC4} (page cycle) [mA]
60
50
40
30
20
4.0
4.5
5.0
5.5
6.0
V_{CC} [V]

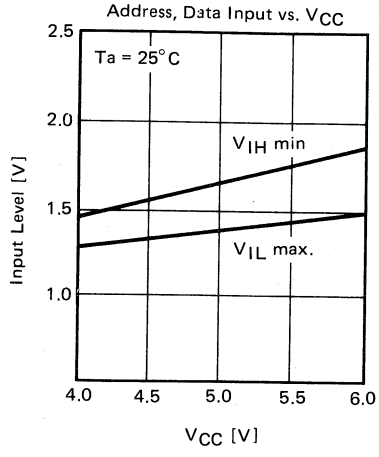

ICC4 vs. Ta
VCC = 5.5V
tPC = 145 nS
ICC4 (page cycle) [mA]
50
45
40
35
30
0
25
50
70
Ta [°C]

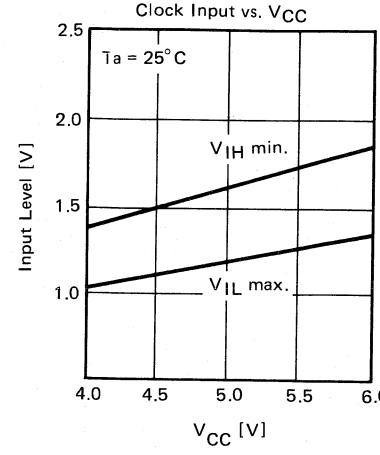

Address, Data Input vs. Ta
VCC = 4.5V
VIH min.
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
0.5
0
25
50
70
Ta [°C]

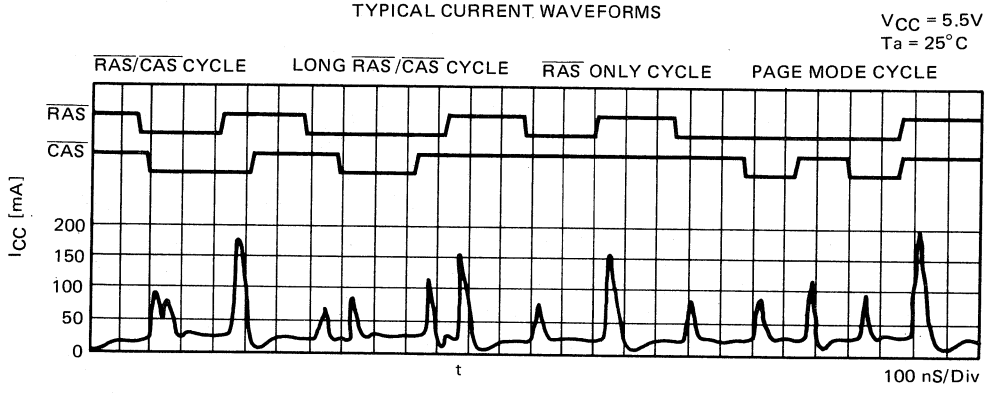

Address, Data Input vs. Ta
VCC = 5.5V
VIH min.
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
0.5
0
25
50
70
Ta [°C]


Clock Input vs. Ta
VCC = 4.5V
VIH min.
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
0.5
0
25
50
70
Ta [°C]

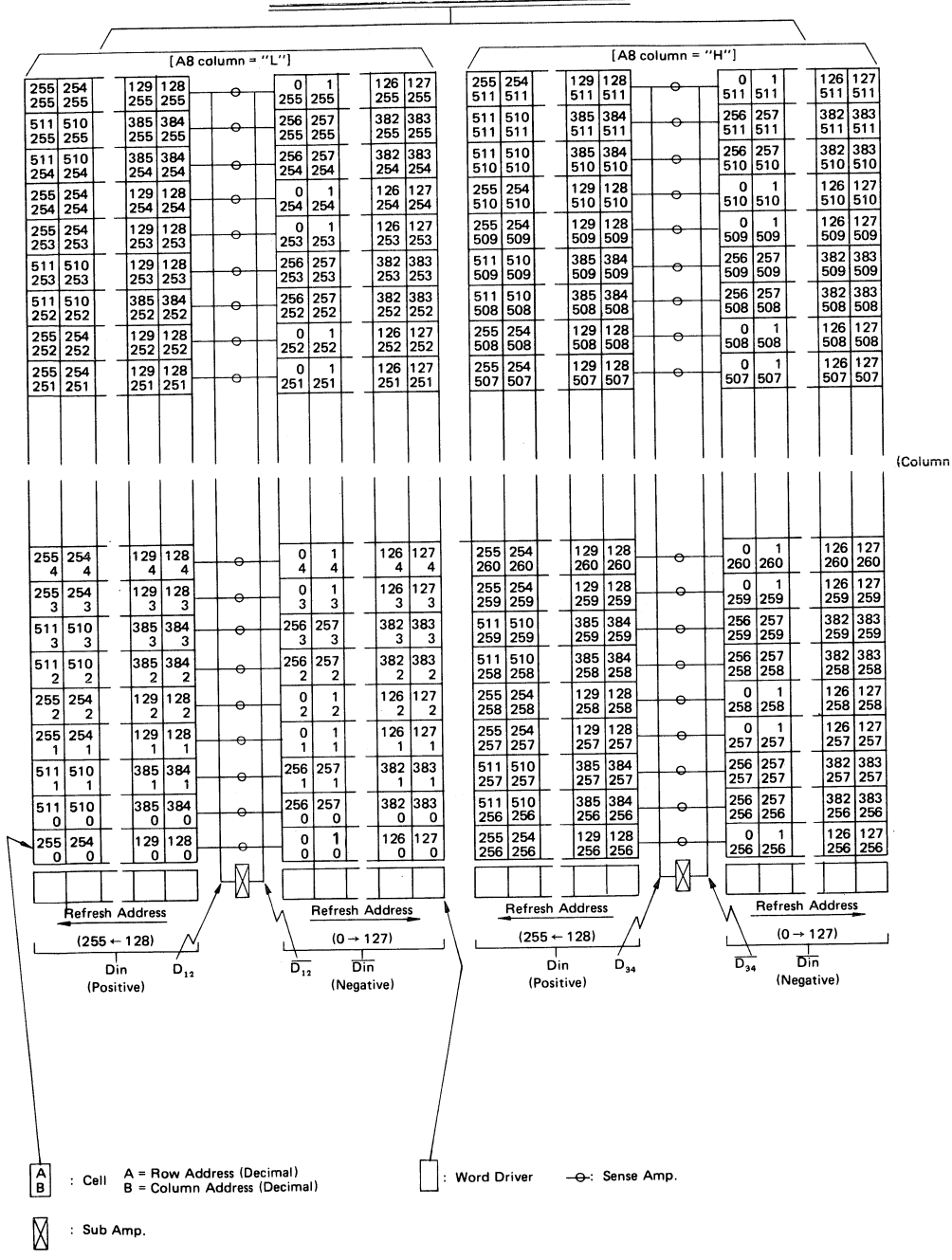

Clock Input vs. Ta
VCC = 5.5V
VIH min.
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
0.5
0
25
50
70
Ta [°C]


Address, Data Input vs. VCC
Ta = 25°C
VIH min
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
4.0
4.5
5.0
5.5
6.0
VCC [V]


Clock Input vs. VCC
Ta = 25°C
VIH min.
VIL max.
Input Level [V]
2.5
2.0
1.5
1.0
4.0
4.5
5.0
5.5
6.0
VCC [V]


TYPICAL CURRENT WAVEFORMS
VCC = 5.5V
Ta = 25°C
RAS/CAS CYCLE
LONG RAS/CAS CYCLE
RAS ONLY CYCLE
PAGE MODE CYCLE
RAS
CAS
ICC [mA]
200
150
100
50
0
t
100 nS/Div

MSM41256 Bit Map (Physical-Decimal)



OKI semiconductor

MSM41256ARS/JS

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Page Mode Type>

GENERAL DESCRIPTION

The Oki MSM41256A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM 41256A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.

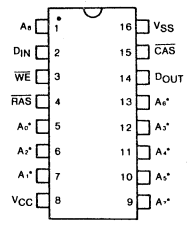
The MSM41256A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

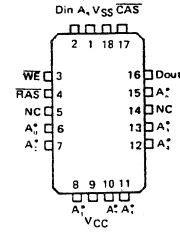
- 262,144 × 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41256A-10)
  - 120 ns max (MSM41256A-12)
  - 150 ns max (MSM41256A-15)
- Cycle time:
  - 200 ns min (MSM41256A-10)
  - 220 ns min (MSM41256A-12)
  - 260 ns min (MSM41256A-15)
- Low power:
  - 330 mW active (MSM41256A-10)
  - 303 mW active (MSM41256A-12)
  - 275 mW active (MSM41256A-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

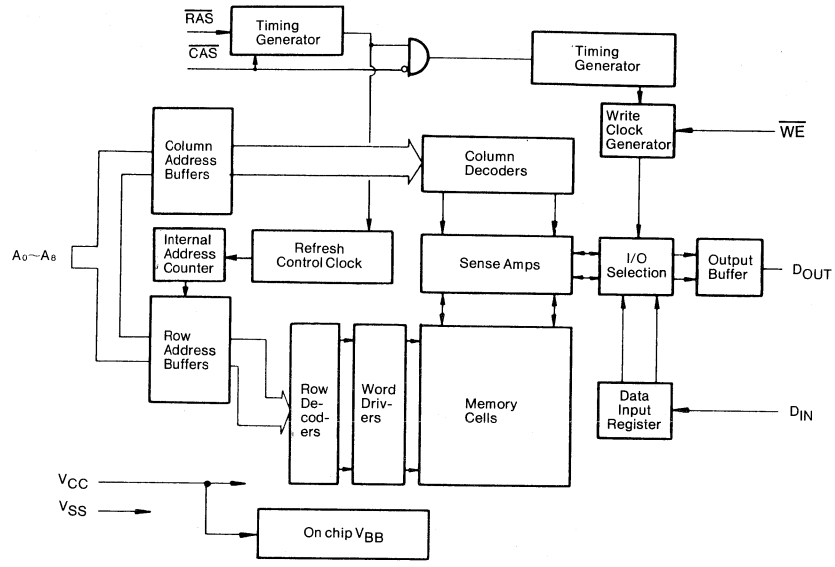
*Refresh Address



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41256A-10	I_{CC1}		60	mA	
	MSM41256A-12			55		
	MSM41256A-15			50		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256A-10	I_{CC3}		55	mA	
	MSM41256A-12			50		
	MSM41256A-15			45		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256A-10	I_{CC4}		40	mA	
	MSM41256A-12			35		
	MSM41256A-15			30		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41256A-10	I_{CC5}		55	mA	
	MSM41256A-12			50		
	MSM41256A-15			45		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	205		225		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

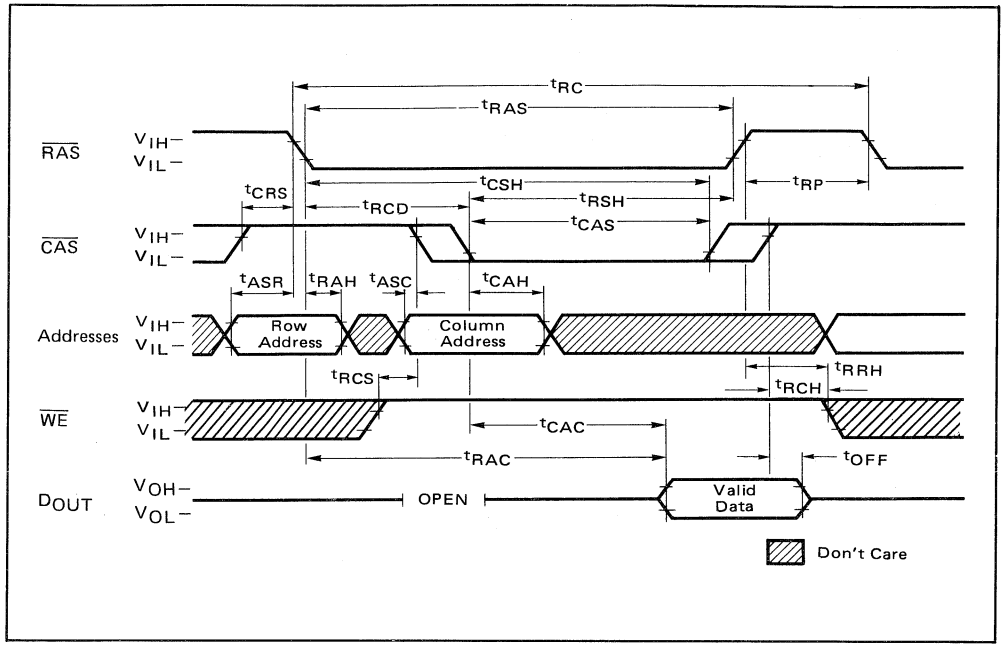
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		9
Page mode read write cycle time	t_{PRWC}	ns	105		125		145		9
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		9
Refresh counter test cycle time	t_{RTC}	ns	315		355		415		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	215	10μs	255	10μs	305	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

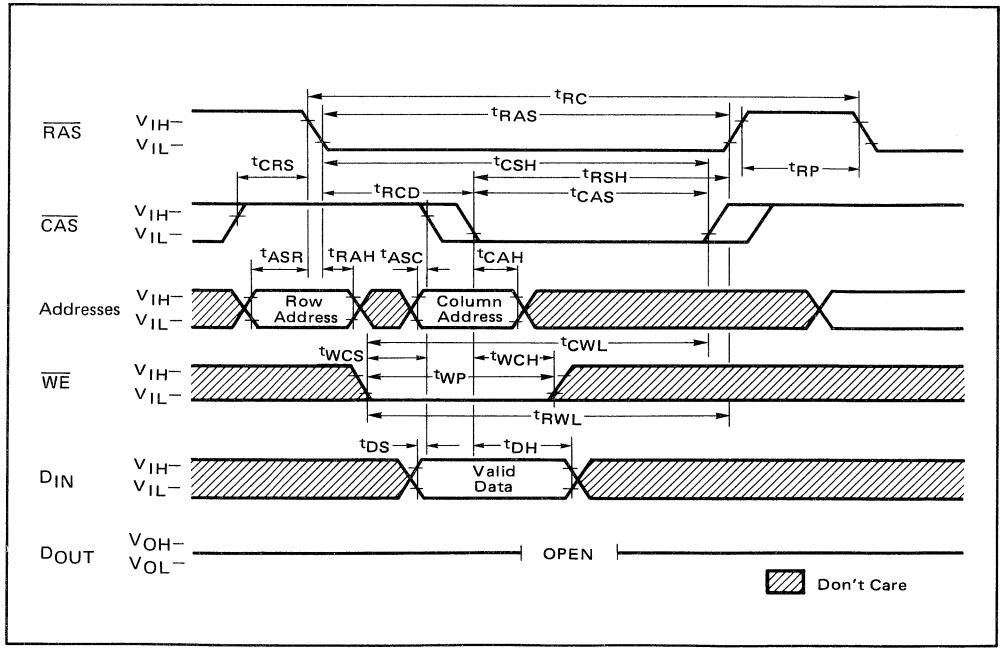
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Page mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

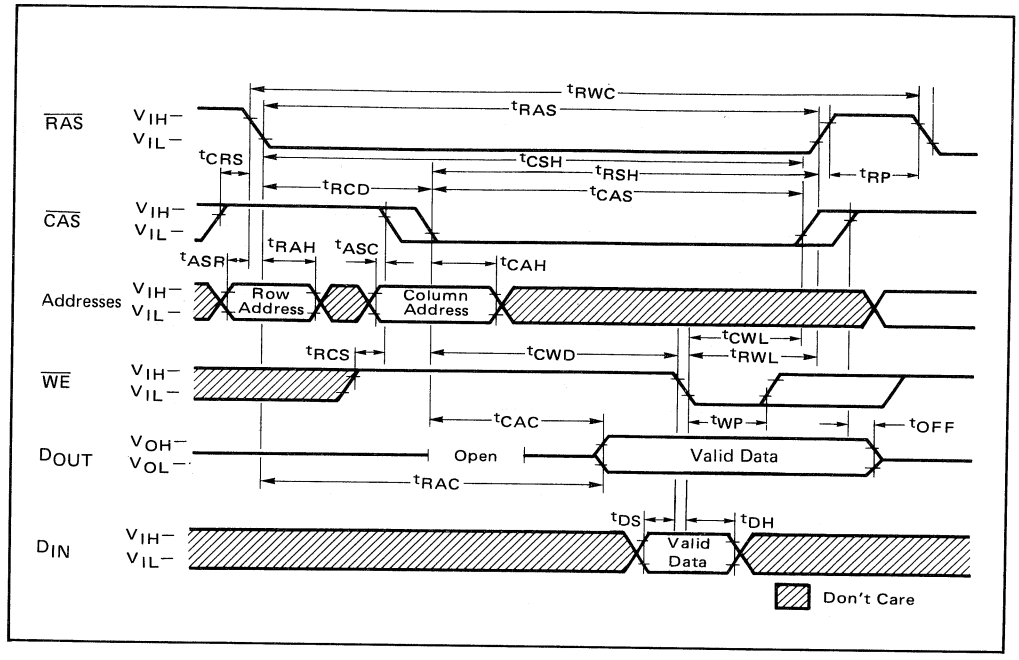
READ CYCLE



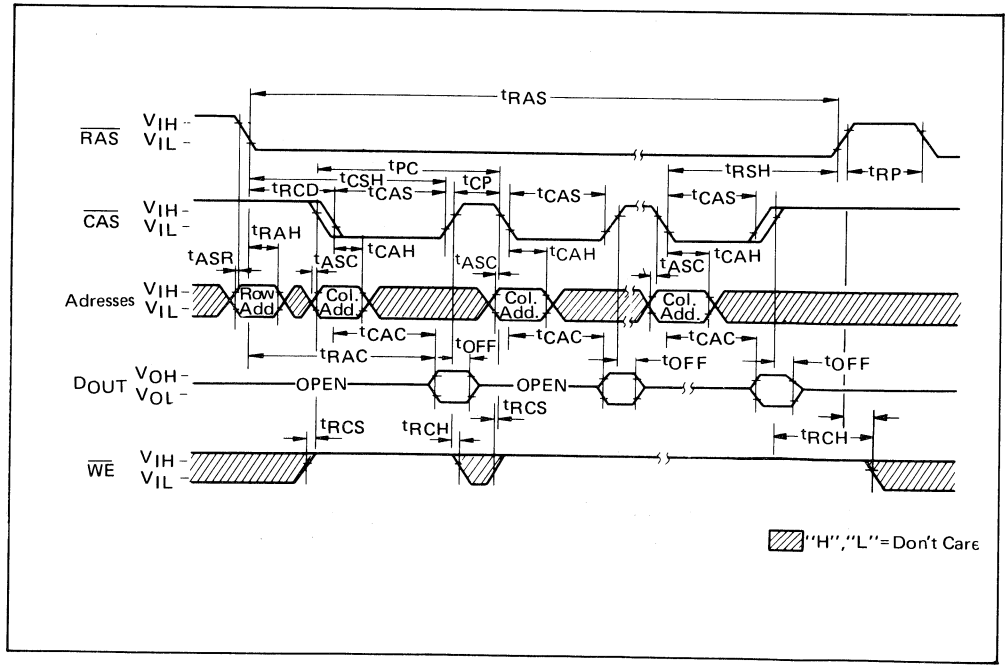
WRITE CYCLE (EARLY WRITE)



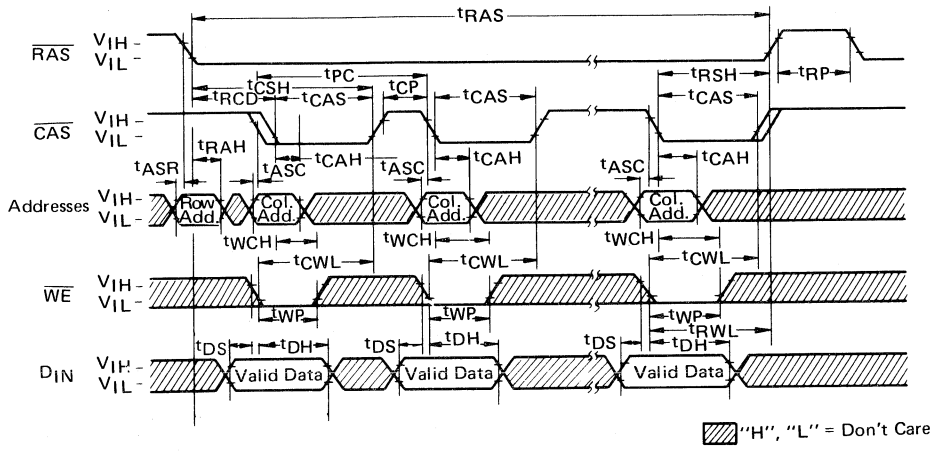
READ-WRITE/READ-MODIFY-WRITE CYCLE



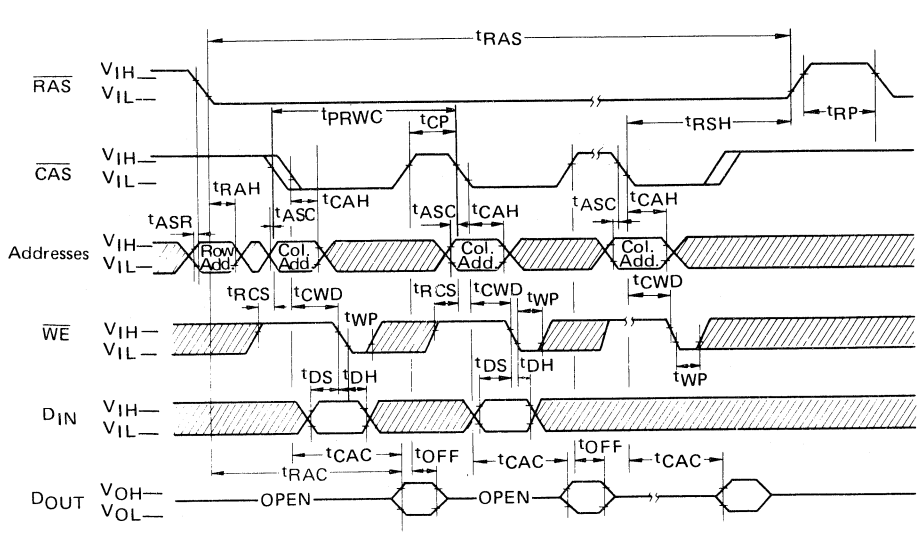
PAGE MODE READ CYCLE



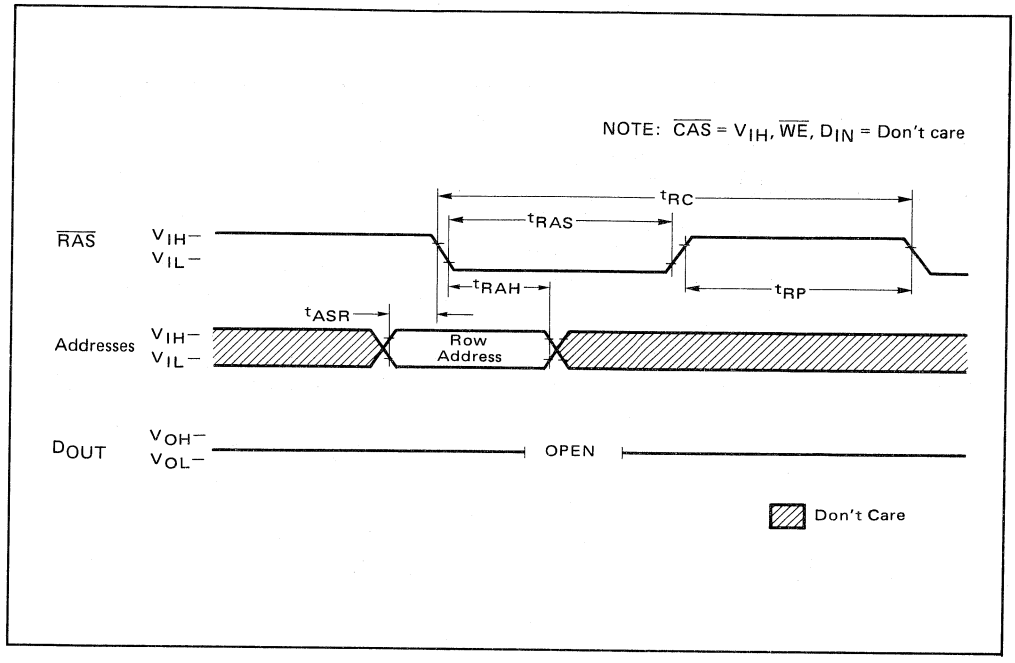
PAGE MODE WRITE CYCLE



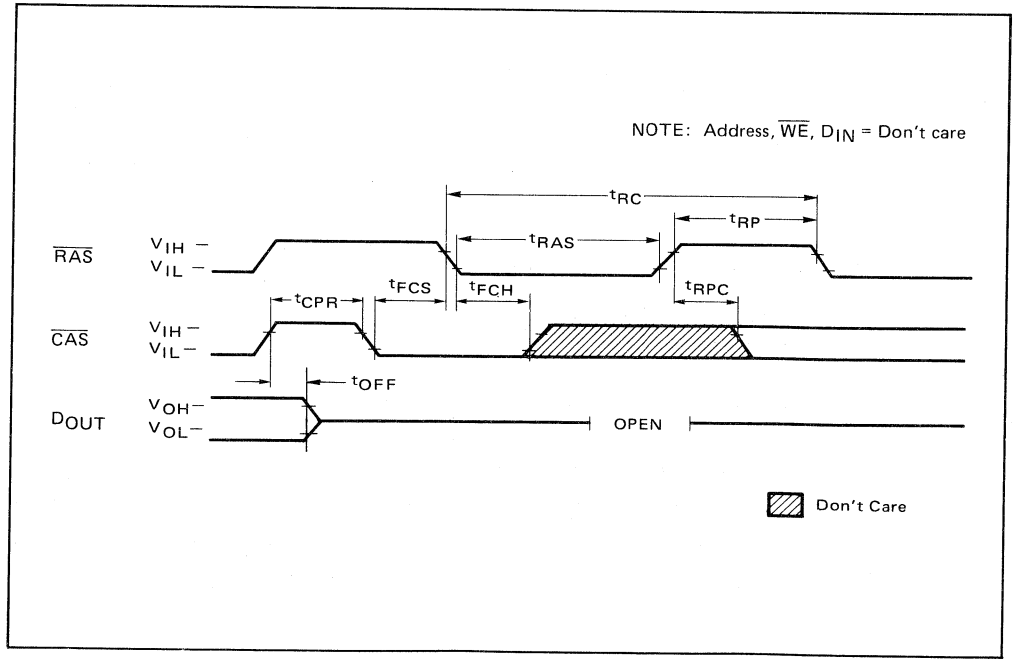
PAGE MODE, READ-MODIFY-WRITE CYCLE



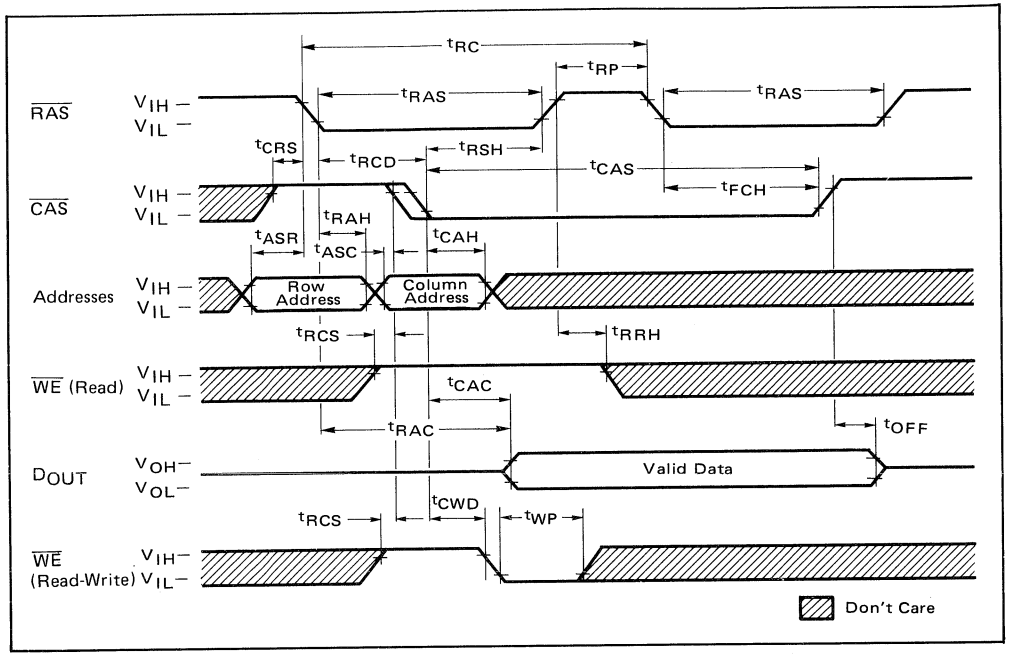
$\overline{RAS}$ ONLY REFRESH CYCLE



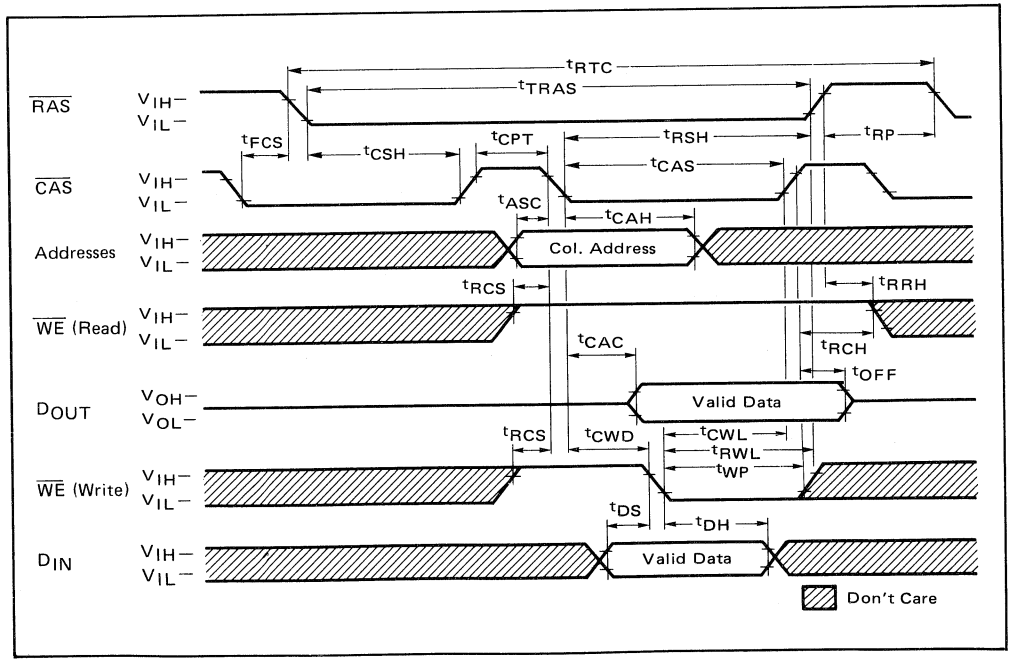
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41256A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41256A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41256A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41256A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41256A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41256A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41256A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41256A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41256A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS
(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS
(0 – 255)

□ Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

ROW ADDRESS
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
N=0, 1, 2, ·····63

COLUMN ADDRESS
2N : POSITIVE
2N : NEGATIVE
2N+1 : NEGATIVE
2N+1 : POSITIVE
N=0, 1, 2, ·····255

MSM41257ARS/JS

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Nibble Mode Type>

GENERAL DESCRIPTION

The Oki MSM41257A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41257A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41257A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.
high speed serial access to up to 4 bits of data.

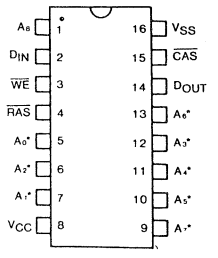
The MSM41257A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

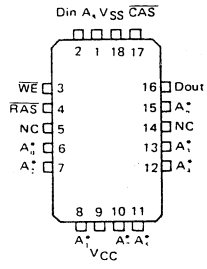
- 262,144 × 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41257A-10)
  - 120 ns max (MSM41257A-12)
  - 150 ns max (MSM41257A-15)
- Cycle time:
  - 200 ns min (MSM41257A-10)
  - 220 ns min (MSM41257A-12)
  - 260 ns min (MSM41257A-15)
- Low power:
  - 330 mW active (MSM41257A-10)
  - 303 mW active (MSM41257A-12)
  - 275 mW active (MSM41257A-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

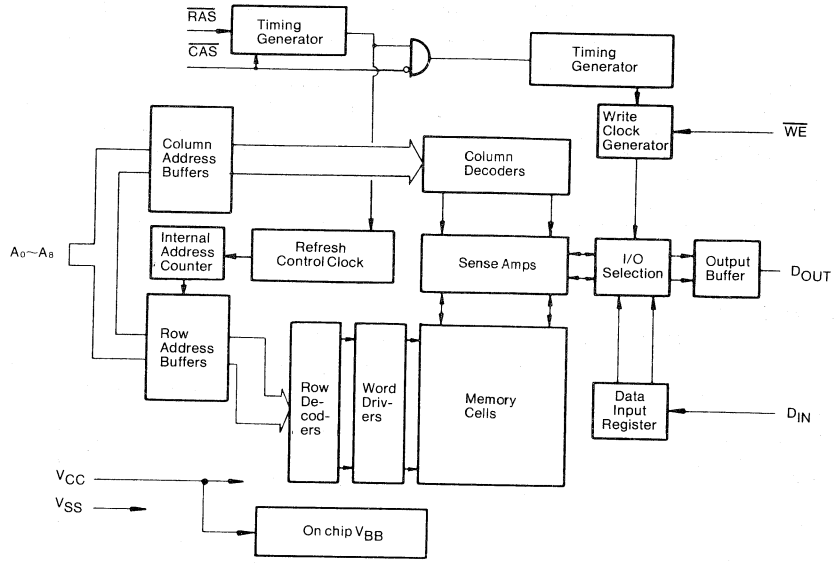
*Refresh Address



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41257A-10	I_{CC1}		60	mA	
	MSM41257A-12			55		
	MSM41257A-15			50		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41257A-10	I_{CC3}		55	mA	
	MSM41257A-12			50		
	MSM41257A-15			45		
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	MSM41257A-10	I_{CC4}		30	mA	
	MSM41257A-12			27		
	MSM41257A-15			25		
REFRESH CURRENT 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41257A-10	I_{CC5}		55	mA	
	MSM41257A-12			50		
	MSM41257A-15			45		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	205		225		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Nibble mode read/write cycle time	t_{NC}	ns	60		70		80		9
Nibble mode read-write cycle time	t_{NRWC}	ns	60		70		80		9
Nibble mode access time	t_{NCAC}	ns		25		30		35	9
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	25		30		35		9
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	ns	25		30		35		9
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	ns	25		30		35		9
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	ns	45		50		60		9
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	25		30		35		9

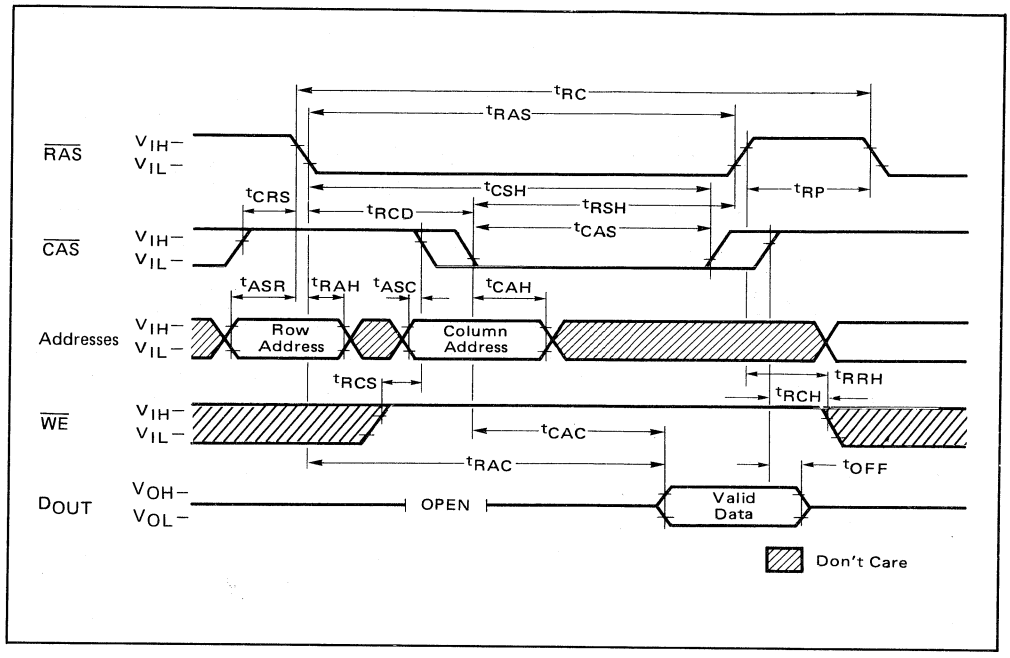
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh counter test cycle time	t_{RTC}	ns	315		355		415		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	215	10μs	255	10μs	305	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

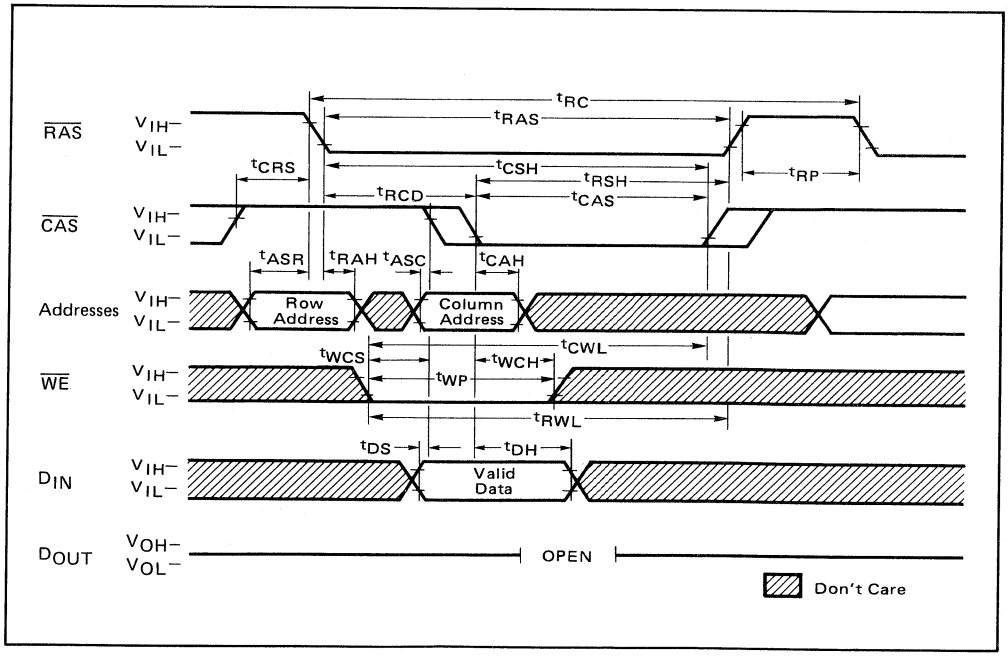
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Nibble mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

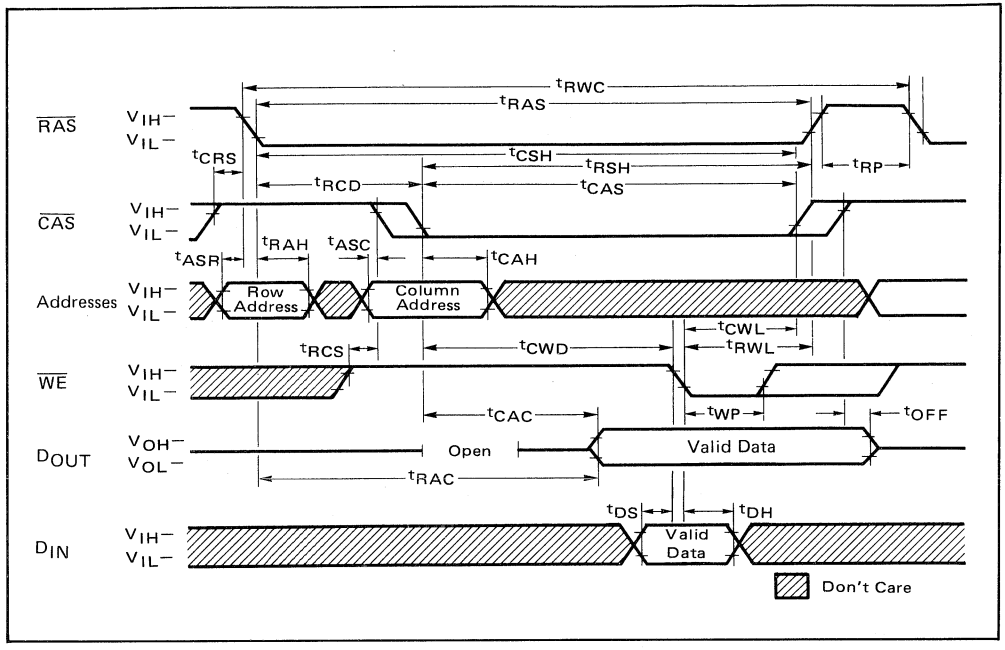
READ CYCLE



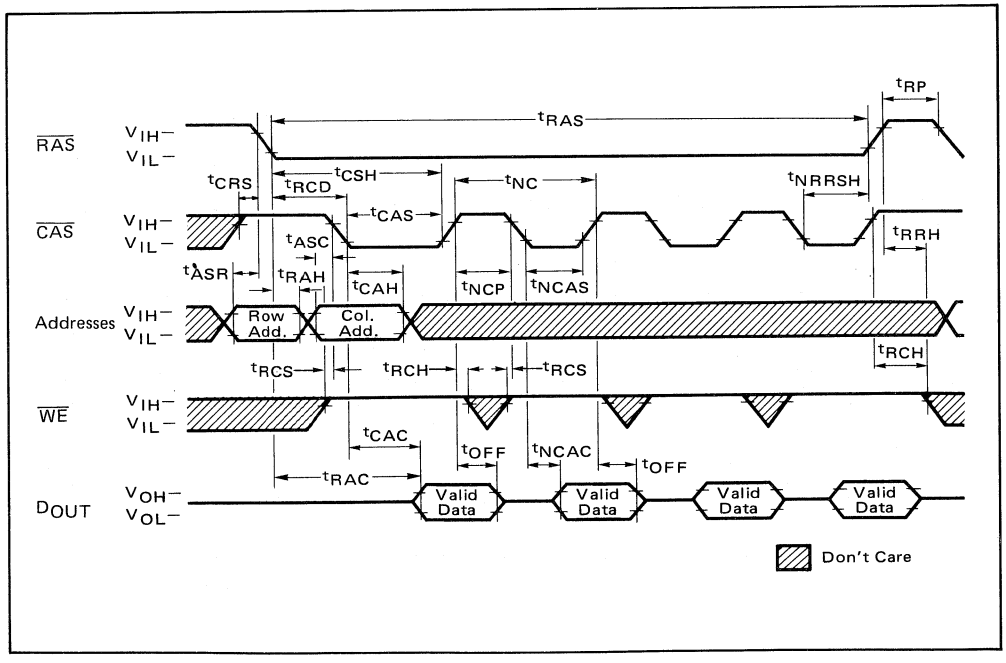
WRITE CYCLE (EARLY WRITE)



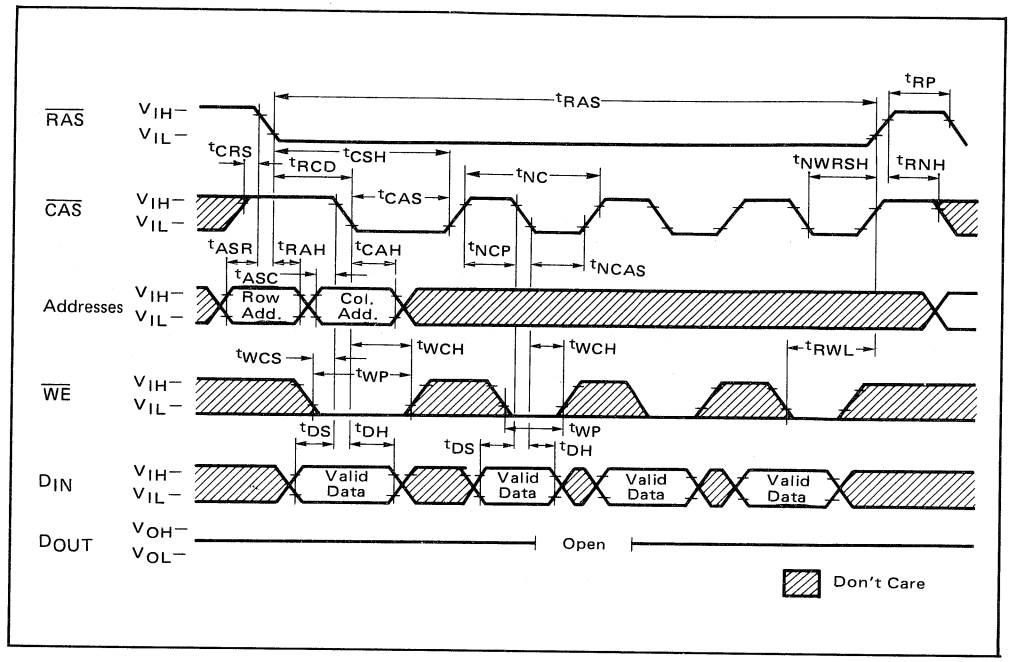
READ-WRITE/READ-MODIFY-WRITE CYCLE



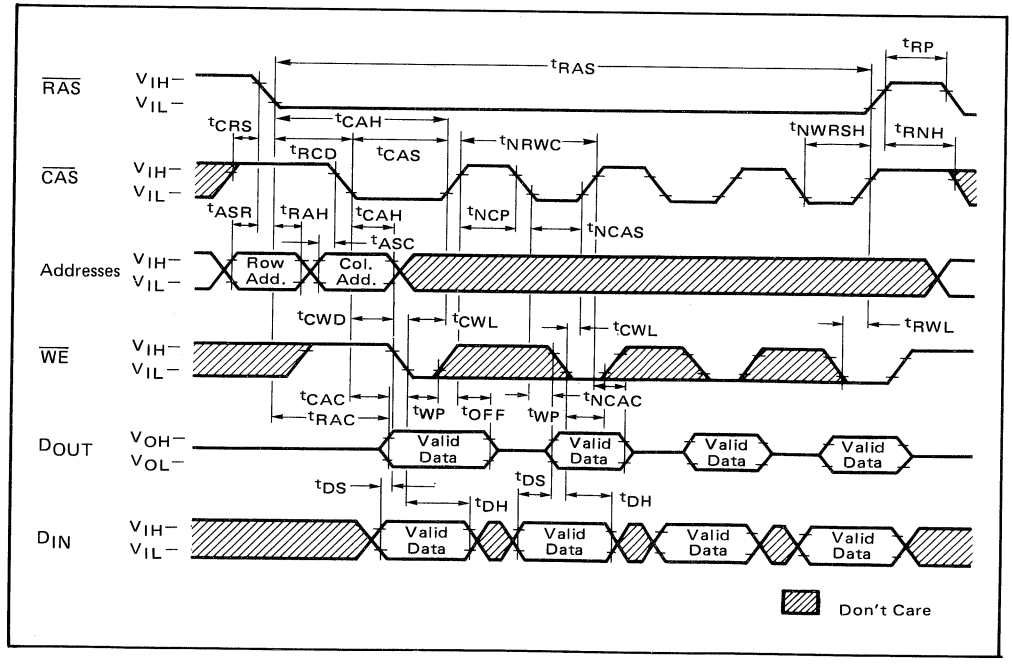
NIBBLE MODE READ CYCLE



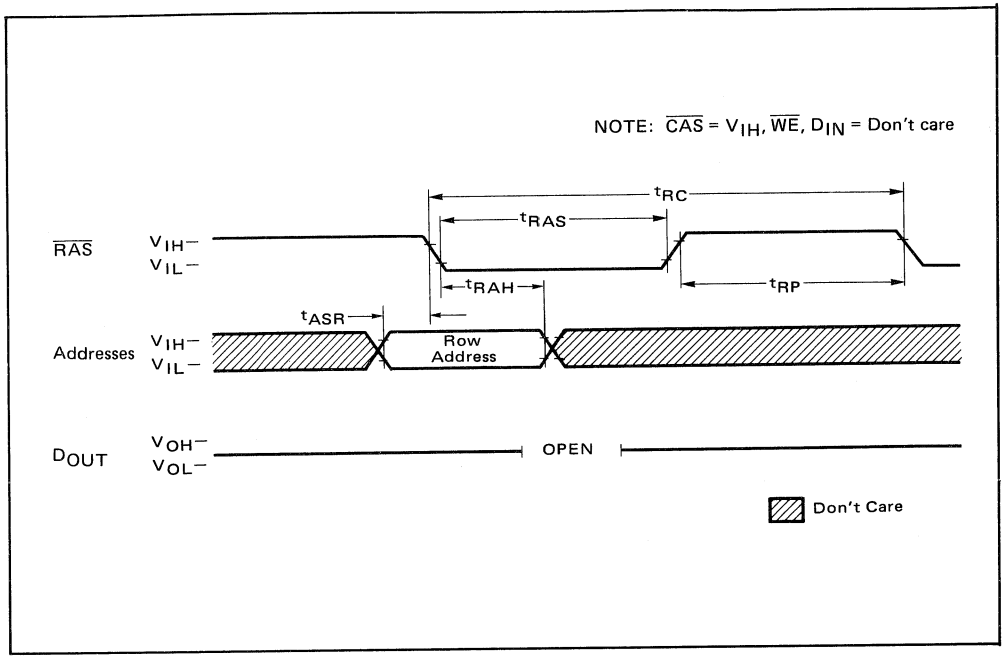
NIBBLE MODE WRITE CYCLE



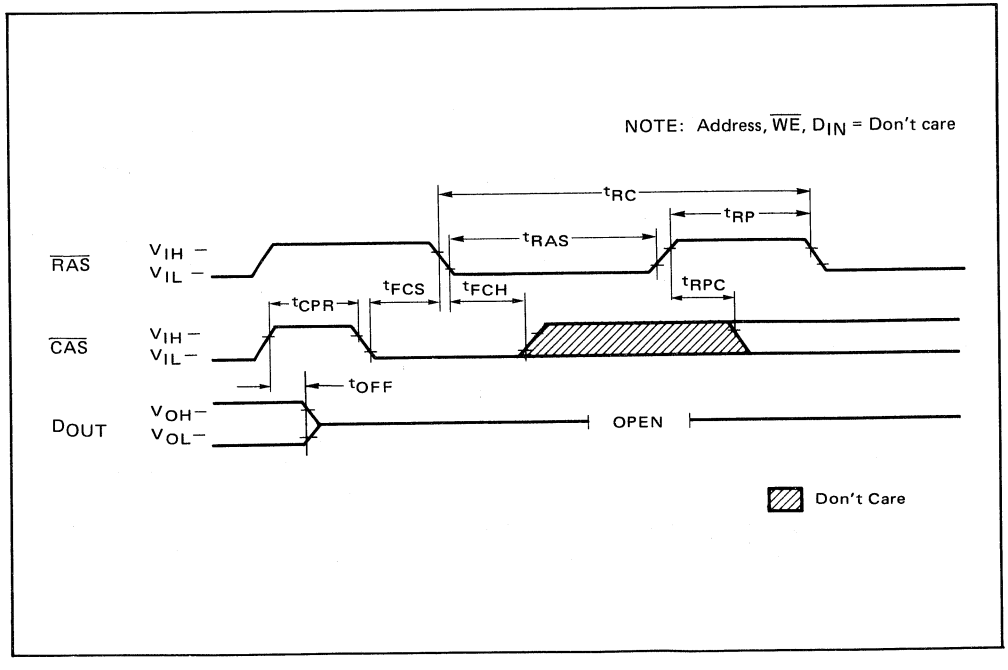
NIBBLE MODE READ-WRITE CYCLE



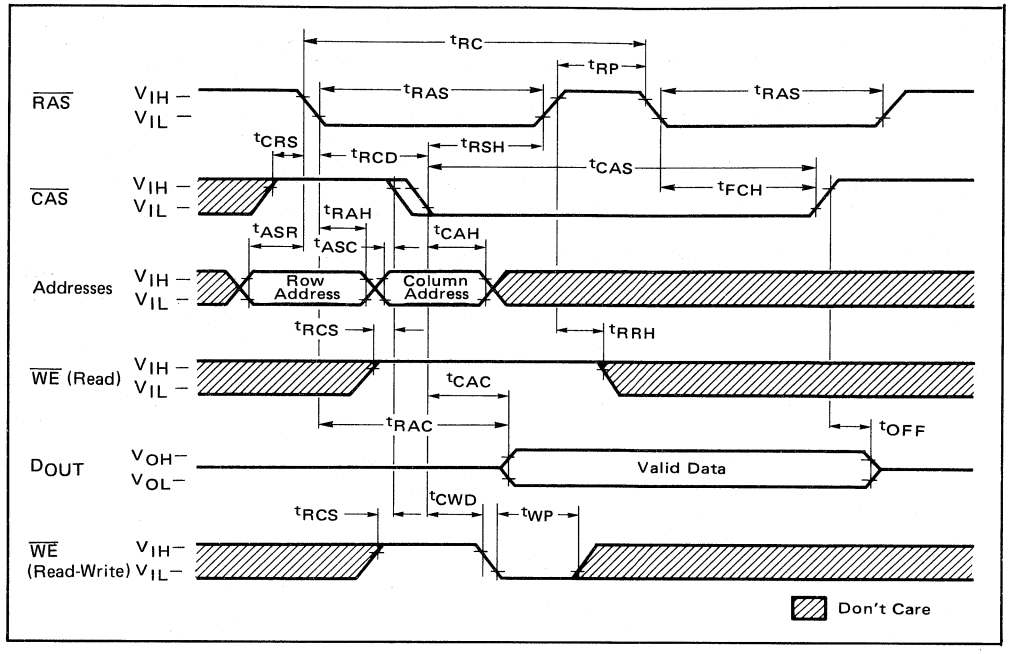
$\overline{RAS}$ ONLY REFRESH CYCLE



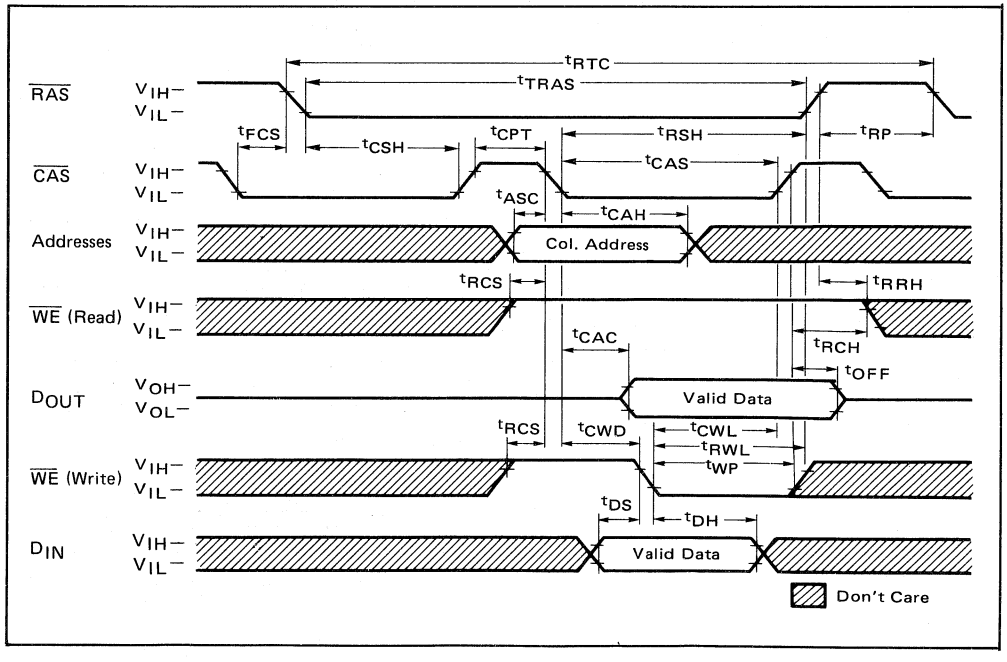
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41257A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41257A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41257A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41257A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41257A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41257A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41257A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41257A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41257A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8 RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	... input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	generated internally sequence repeats
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41257A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41257A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

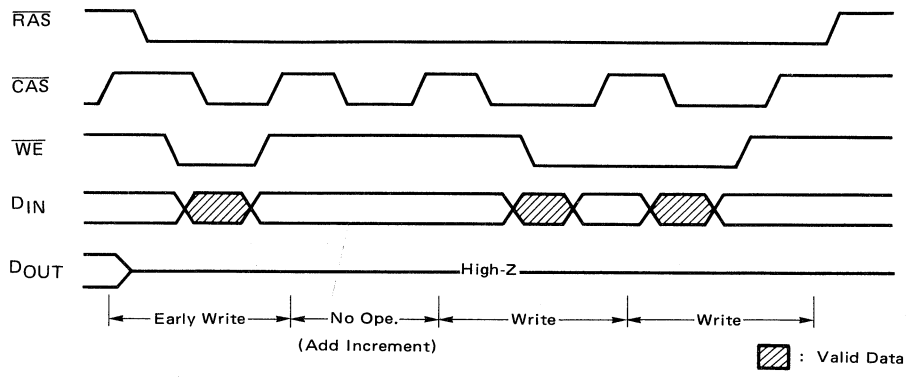
Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

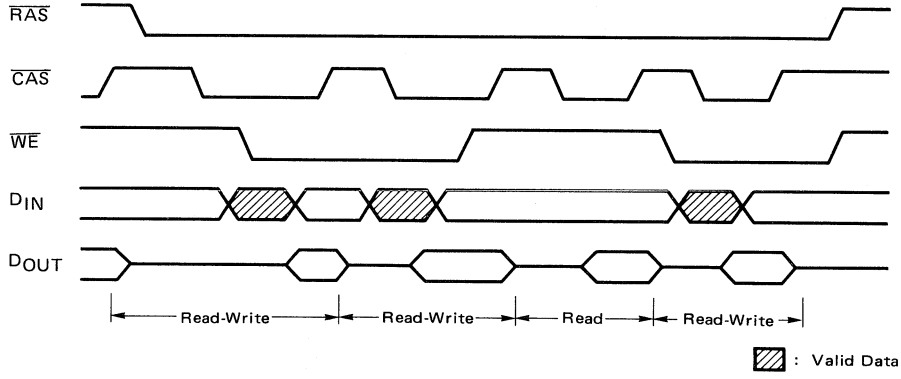
(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

NIBBLE MODE

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)



MSM41257A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS
(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS
(0 – 255)

□ Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

ROW ADDRESS	COLUMN ADDRESS	
8N+6, 8N+7, 8N, 8N+1	2N	: POSITIVE
8N+2, 8N+3, 8N+4, 8N+5	2N	: NEGATIVE
8N+6, 8N+7, 8N, 8N+1	2N+1	: NEGATIVE
8N+2, 8N+3, 8N+4, 8N+5	2N+1	: POSITIVE
N=0, 1, 2, ·····63	N=0, 1, 2, ·····255	

OKI semiconductor

MSM41464RS/JS

65,536-WORD × 4-BITS DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM41464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41464 to be housed in a standard 18 pin DIP or PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh provides an on-chip refresh capability.

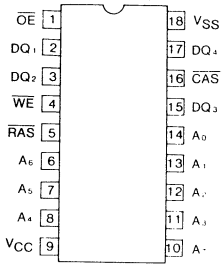
The MSM41464 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

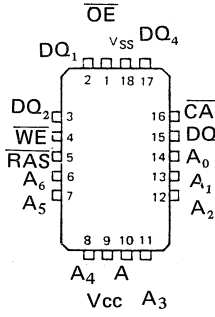
FEATURES

- 65,536 × 4 RAM, 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41464-10)
  - 120 ns max (MSM41464-12)
  - 150 ns max (MSM41464-15)
- Cycle time:
  - 200 ns min (MSM41464-10)
  - 220 ns min (MSM41464-12)
  - 260 ns min (MSM41464-15)
- Low power:
  - 385 mW active (MSM41464-10)
  - 360 mW active (MSM41464-12)
  - 330 mW active (MSM41464-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{\text{CAS}}$
- 256 refresh cycles/4 ms
- Output impedance controllable through early write and $\overline{\text{OE}}$ operations
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- "Page Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$DQ_1 \sim DQ_4$	Data In/Data Out
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)



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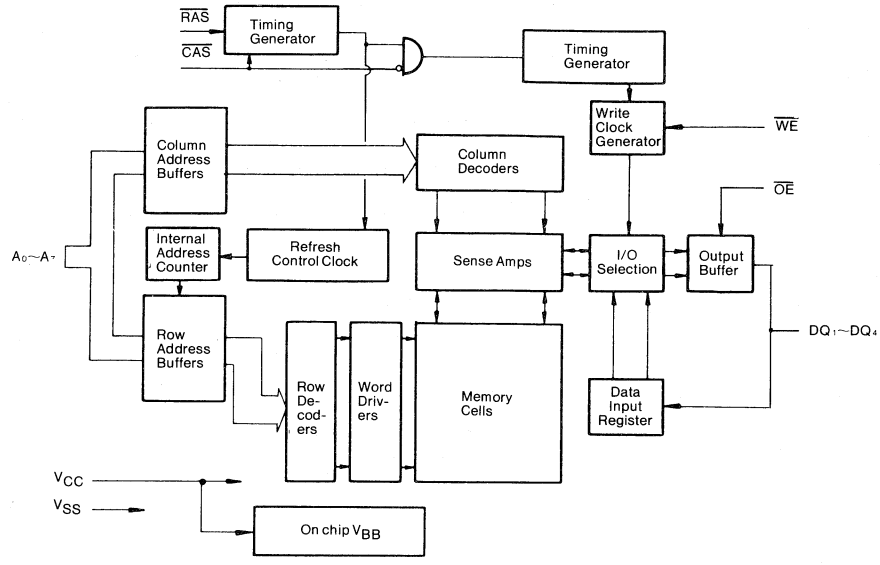
FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41464-10	I_{CC1}		70	mA	
	MSM41464-12			65		
	MSM41464-15			60		
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41464-10	I_{CC3}		60	mA	
	MSM41464-12			55		
	MSM41464-15			50		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41464-10	I_{CC4}		45	mA	
	MSM41464-12			40		
	MSM41464-15			35		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41464-10	I_{CC5}		65	mA	
	MSM41464-12			60		
	MSM41464-15			55		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_7$)	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	7	pF
Data I/O capacitance ($DQ_1 \sim DQ_4$)	C_D	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Note 1, 2, 3

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	270		300		355		
Page mode cycle time	t_{PC}	ns	100		120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	25	0	30	0	40	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	ns	40		50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7, 8
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		10
Write command set-up time	t_{WCS}	ns	0		0		0		9

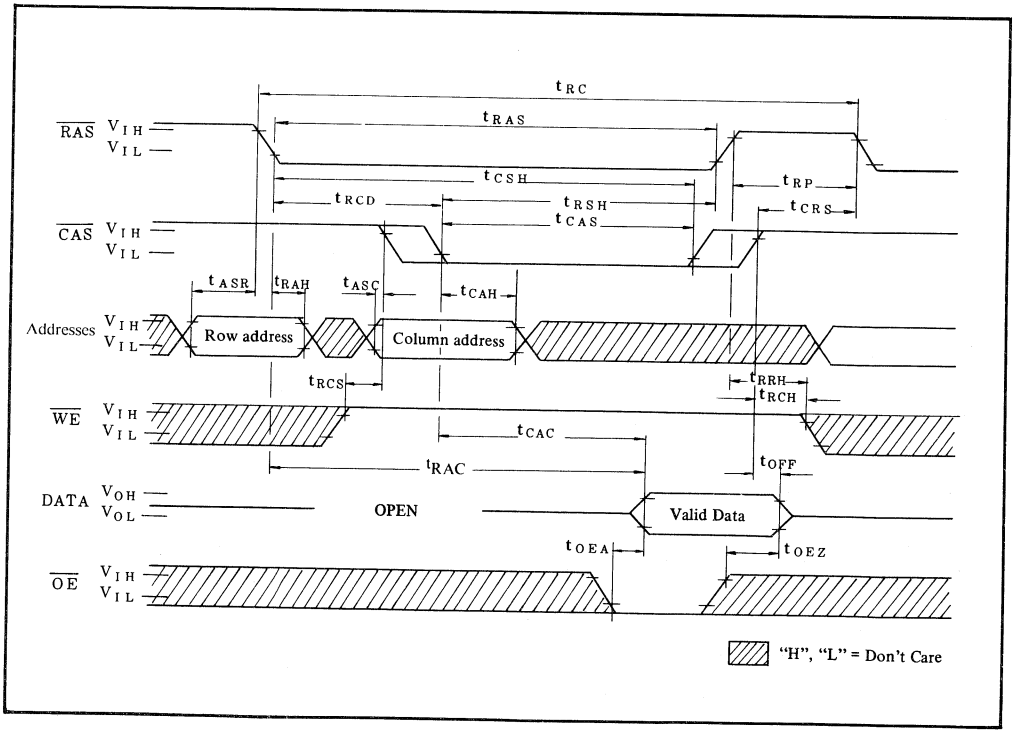
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	25		30		35		
Write command hold time	t_{WCH}	ns	25		30		35		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	25		30		35		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	80		95		120		9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	130		155		195		9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		20		20		10
Access time from $\overline{OE}$	t_{OEA}	ns		25		30		40	
$\overline{OE}$ data delay time	t_{OED}	ns	25		30		40		
$\overline{OE}$ hold time	t_{OEH}	ns	0		0		0		
Turn-off delay time from $\overline{OE}$	t_{OEZ}	ns	0	25	0	30	0	40	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	ns	20		25		30		
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	ns	20		20		20		
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	ns	20		25		30		
Read/write cycle (Refresh counter test)	t_{RTC}	ns	380		430		510		11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	ns	280	10μs	330	10μs	400	10μs	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	ns	50		60		70		11
Read/write cycle time (Page mode)	t_{PRWC}	ns	170		200		240		

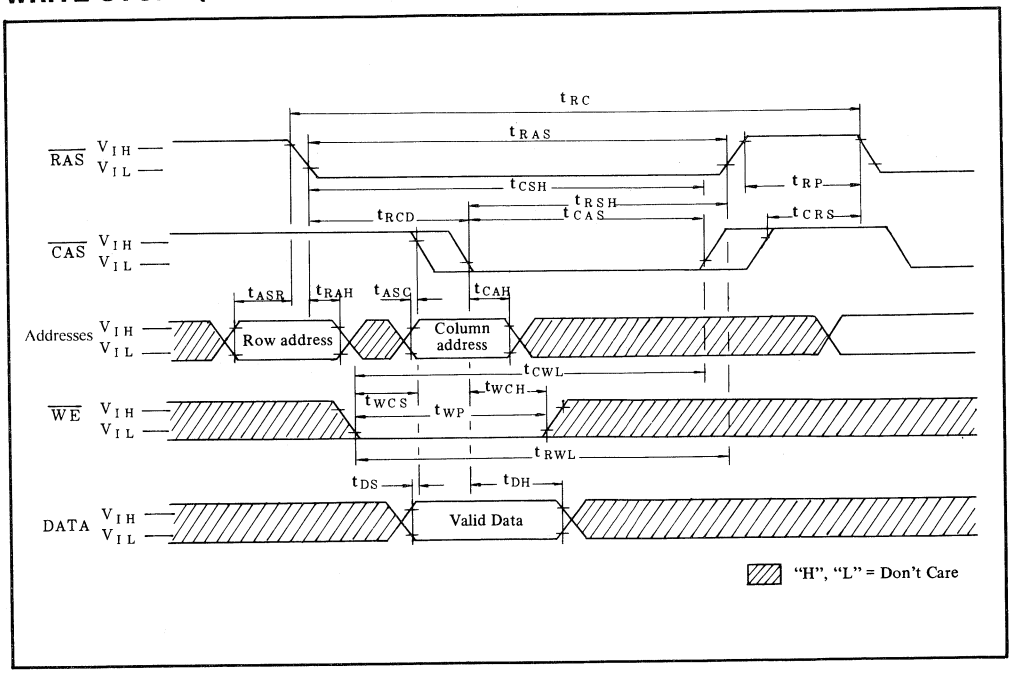
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.) If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) $= t_{RAH}$ (Min.) $+ 2t_T + t_{ASC}$ (Min.)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle and the data in/data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data in/data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

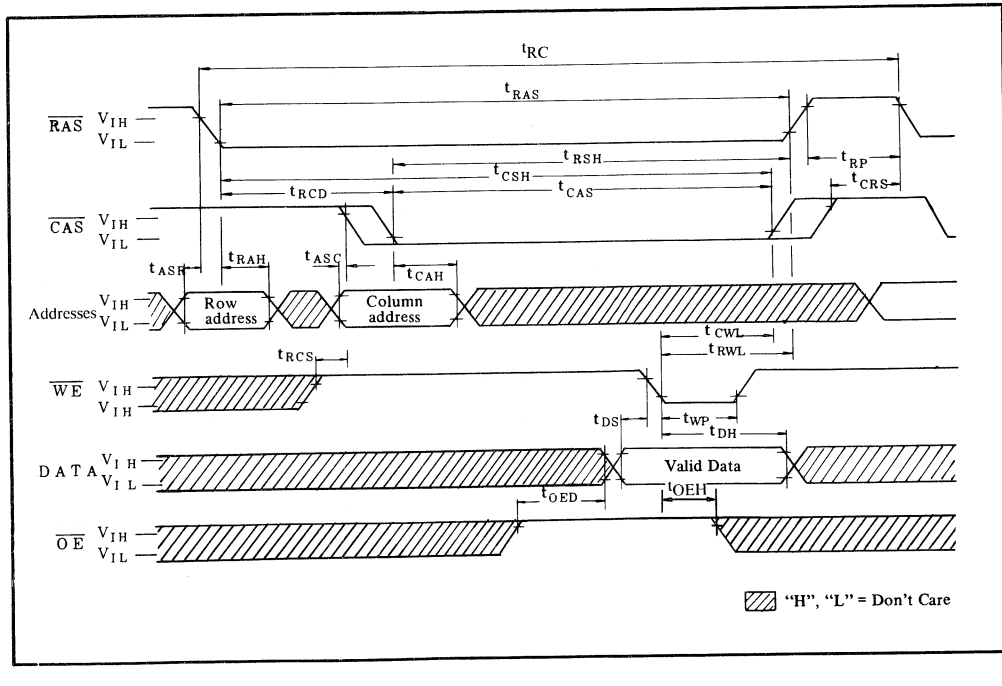
READ CYCLE



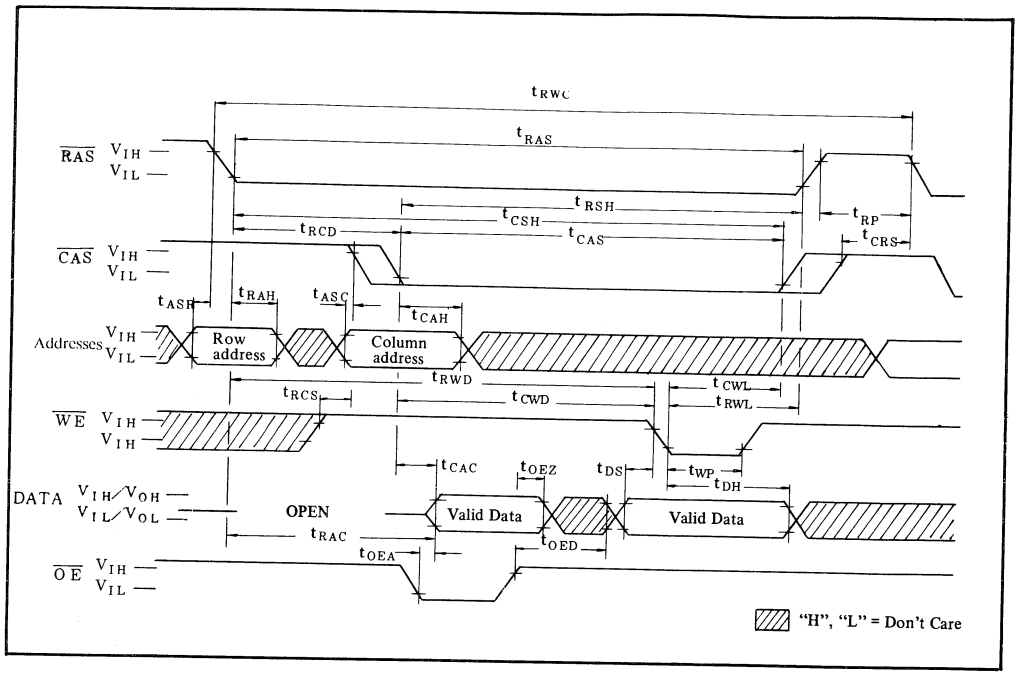
WRITE CYCLE (EARLY WRITE)



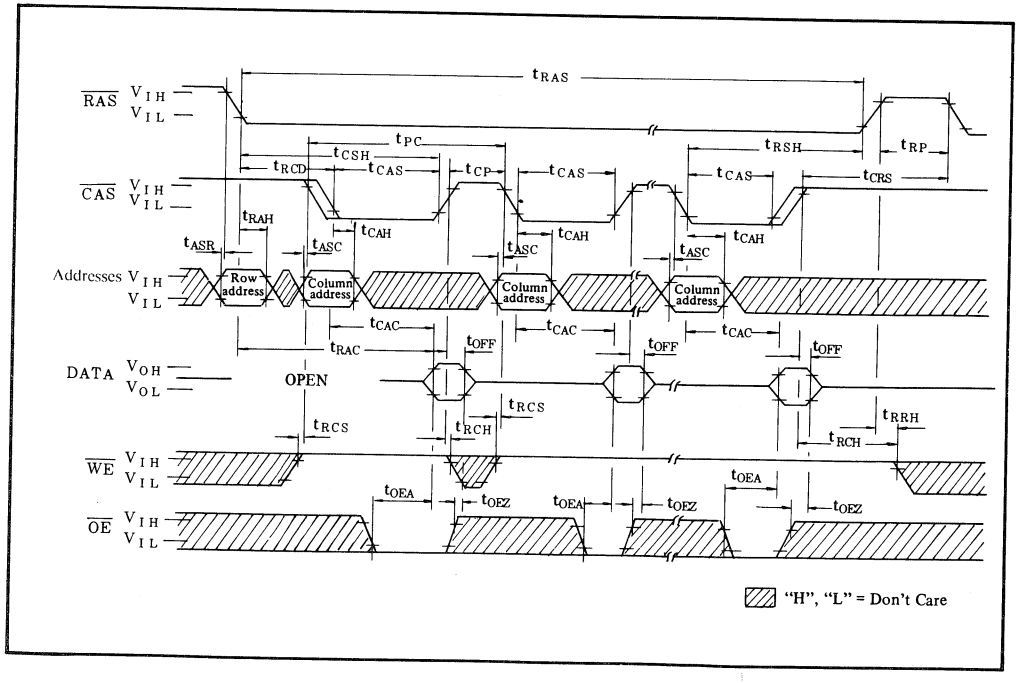
OE WRITE CYCLE



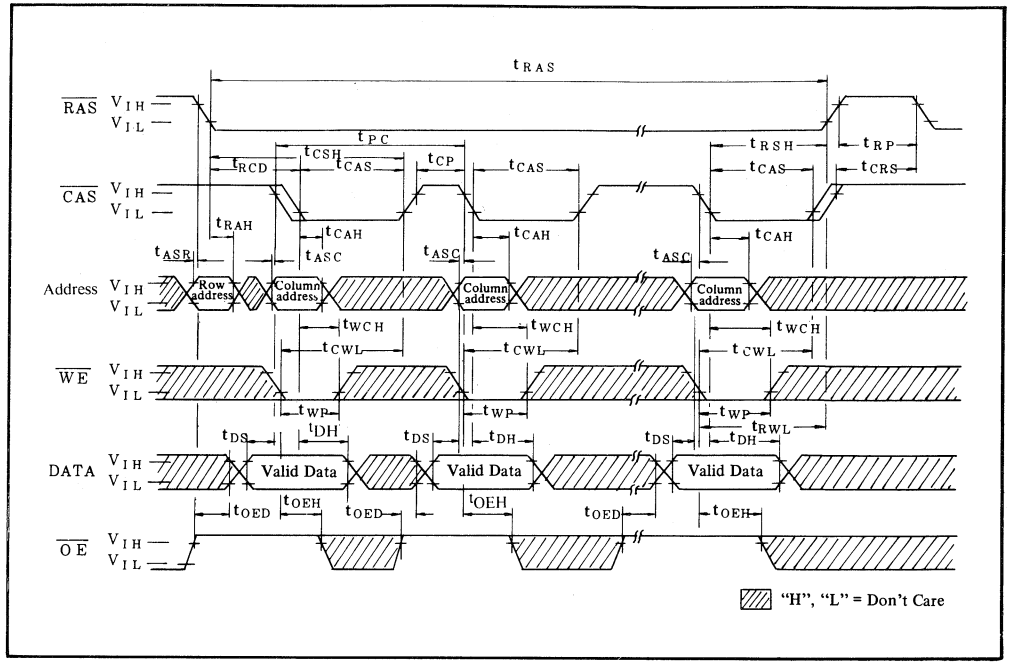
READ/WRITE AND READ MODIFY WRITE CYCLE



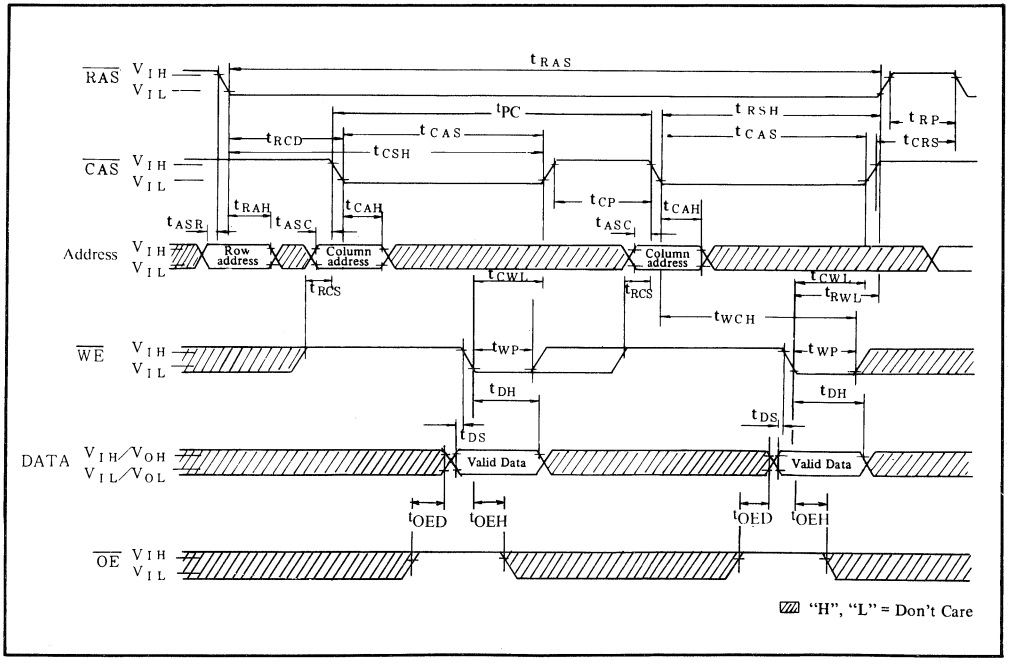
PAGE MODE READ CYCLE



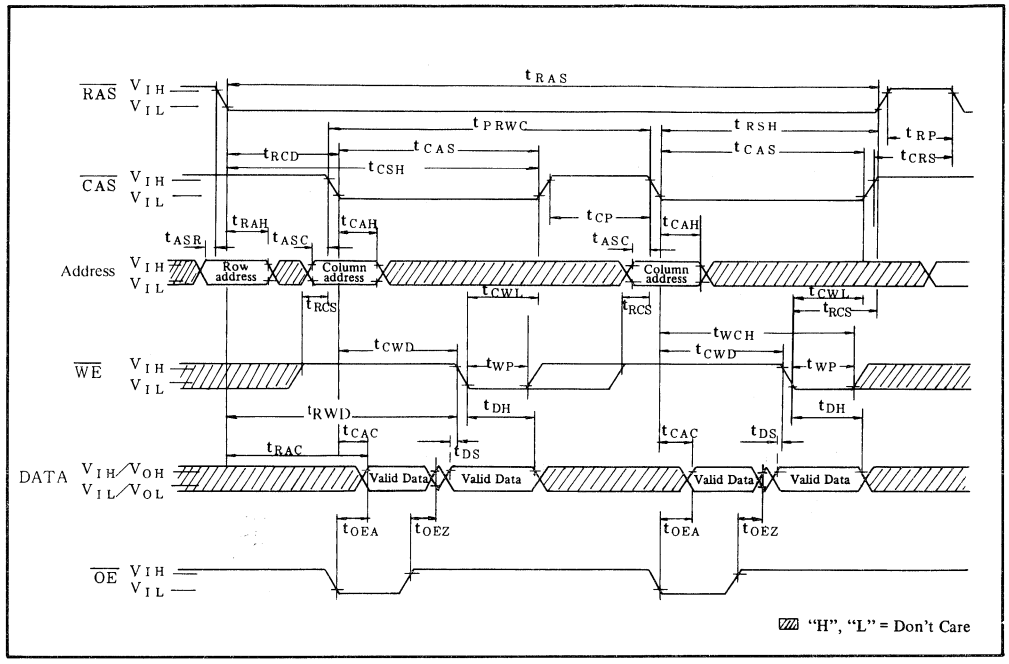
PAGE MODE WRITE CYCLE



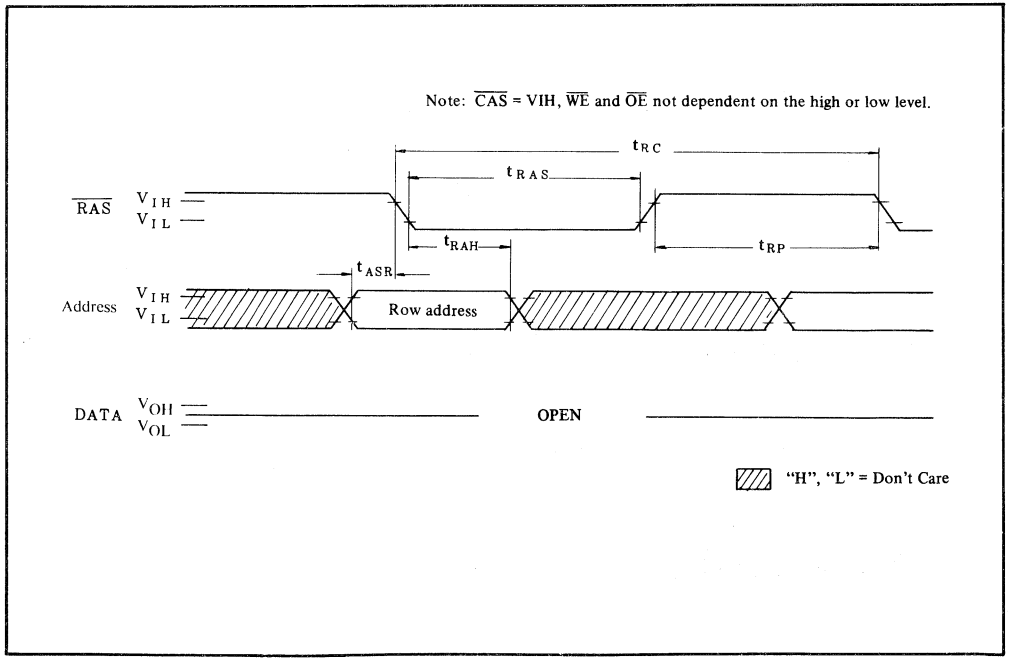
PAGE MODE $\overline{OE}$ WRITE CYCLE



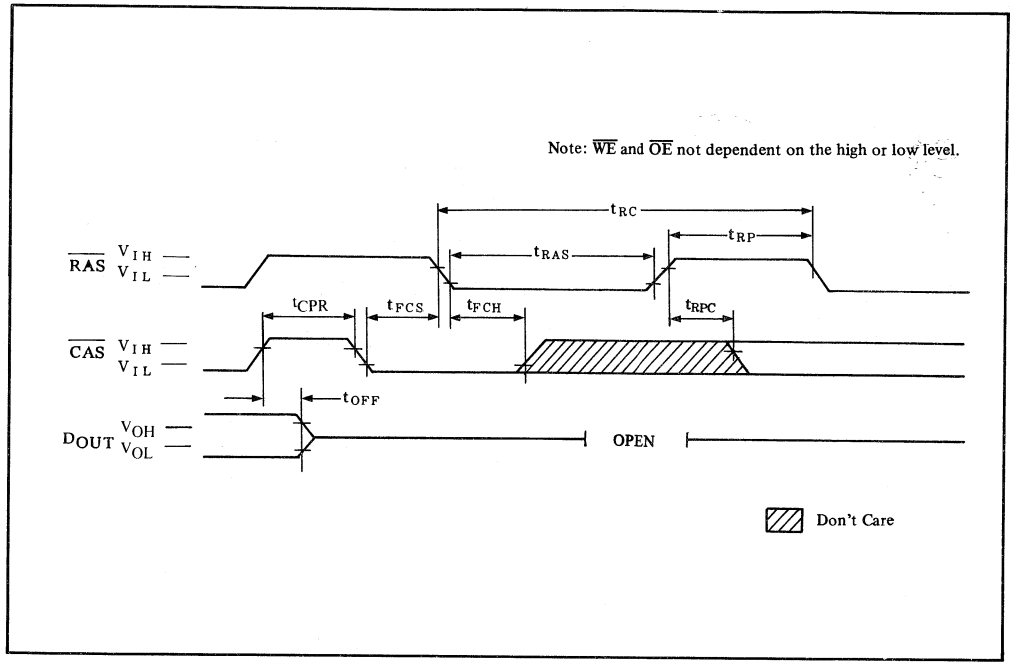
PAGE MODE READ/WRITE CYCLE



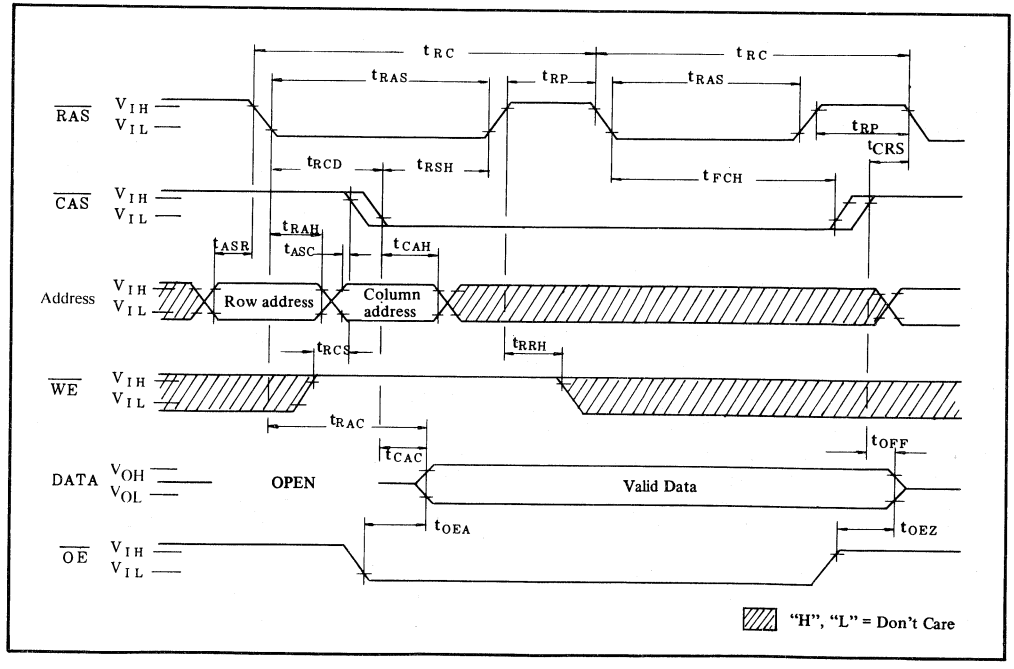
RAS ONLY REFRESH CYCLE



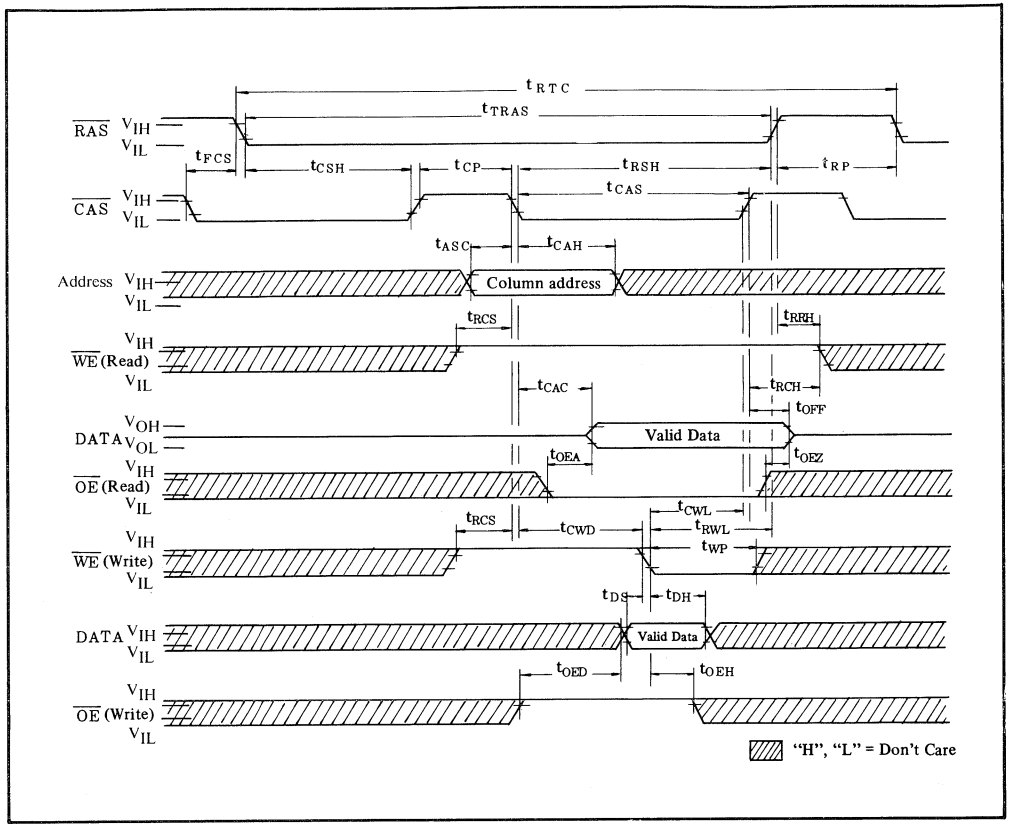
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

16 bits of binary address input are required to decode any one of the 65,536 words by 4 bit storage cell locations.

8 row-address bits are set up on address input pins A_0 through A_7 and latched onto the chip by the row address strobe (RAS). Then 8 column-address bits are set up on pins A_0 through A_7 and latched onto the chip by the column address strobe (CAS).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ or $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every four milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 (A_0 to A_7) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41464 Bit Map (Physical-Decimal)

DQ1 DQ2 DQ4 DQ3

□ Pin 18

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253	253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253	253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COLUMN DECODER

REFRESH ADDRESS

(0 – 255)

REFRESH ADDRESS

(0 – 255)

□
Pin 9

A
B

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)

OKI semiconductor

MSM414256RS

262,144-WORD × 4-BIT DYNAMIC RAM

GENERAL DESCRIPTION

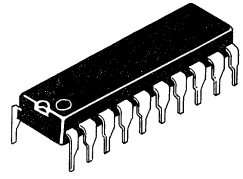
The MSM414256RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM414256RS is OKI's N channel silicon gate MOS process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

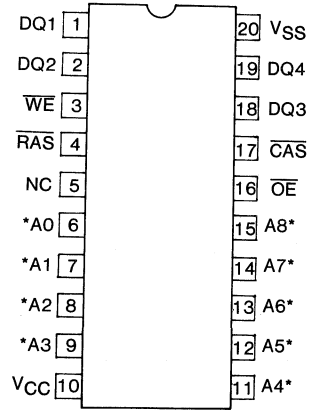
- Silicon gate, tripple polysilicon NMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Stand By (MAX)
MSM414256-10RS	100 ns	200 ns	413 mW	28 mW
MSM414256-12RS	120 ns	230 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and OE operations
- Page mode, read modify write capability
- CAS before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



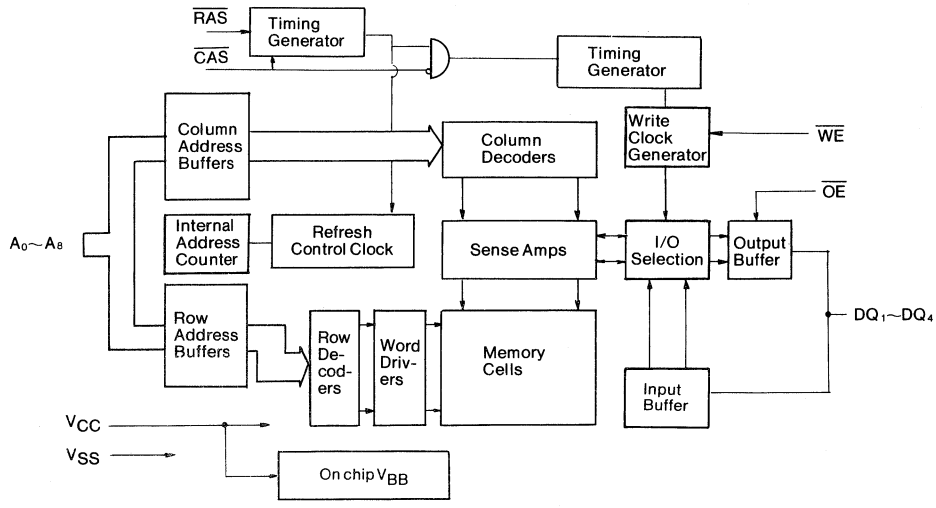
PIN CONFIGURATION (TOP VIEW)



*Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 414256-10		MSM 414256-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	–	2.4	–	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	–	0.4	–	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	–	5	–	5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min	–	65	–	60	mA	
Average power supply current* (Page mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	–	55	–	50	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	65	–	60	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	10	pF
I/O capacitance (DQ1 to DQ4)	C_D	–	–	7	pF

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Read/write cycle time	t_{RWC}	275	–	305	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	10
Write command hold time from $\overline{RAS}$	t_{WCR}	70	–	85	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	9
Write command hold time	t_{WCH}	20	–	25	–	ns	

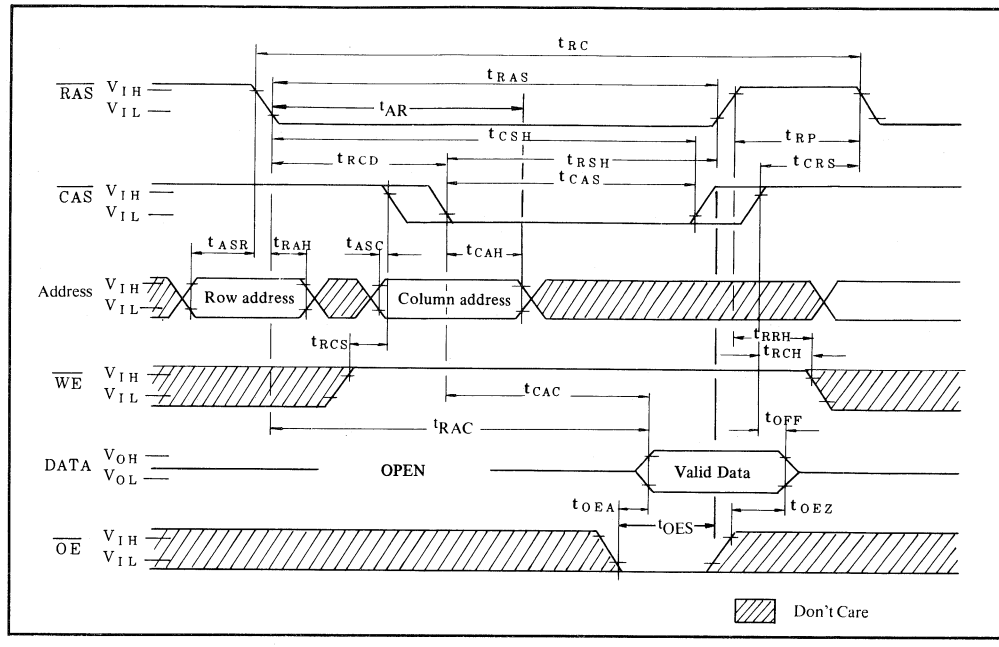
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	70	–	85	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80	–	90	–	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130	–	150	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	10
Access time from $\overline{OE}$	t_{OEA}	–	30	–	30	ns	
$\overline{OE}$ data delay time	t_{OED}	25	–	25	–	ns	
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Turn-off delay time from $\overline{OE}$	t_{OEZ}	0	25	0	25	ns	
$\overline{OE}$ set-up time	t_{OES}	30	–	30	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
Read/write cycle (Refresh counter test)	t_{RTC}	385	–	435	–	ns	11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	285	10000	325	10000	ns	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	11
Read/write cycle time (Page mode)	t_{PRWC}	175	–	195	–	ns	

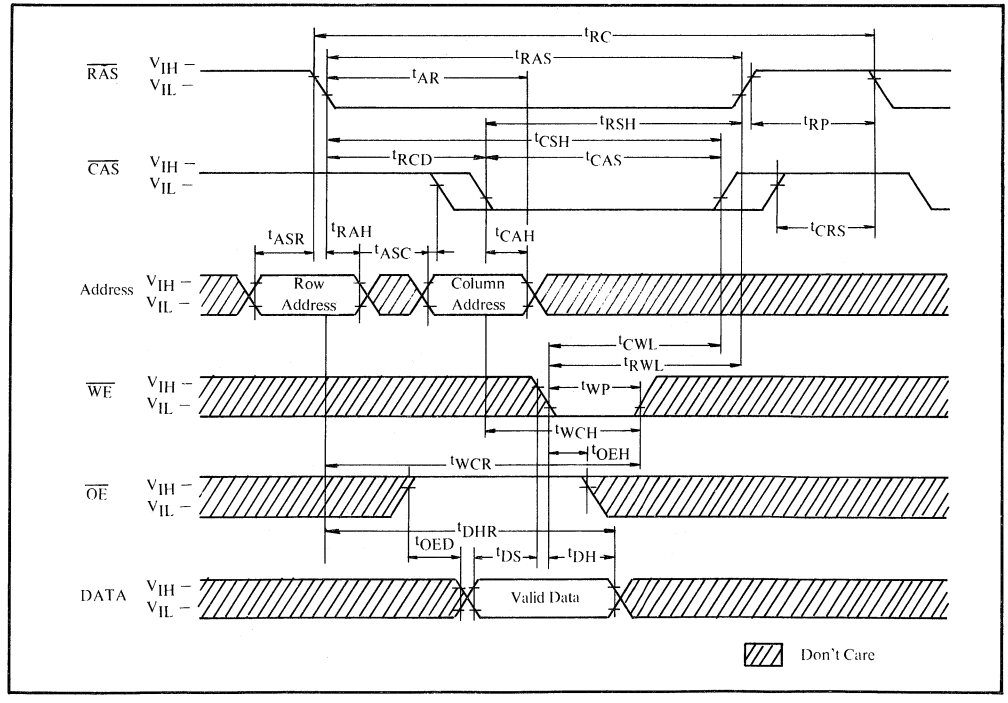
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

READ CYCLE

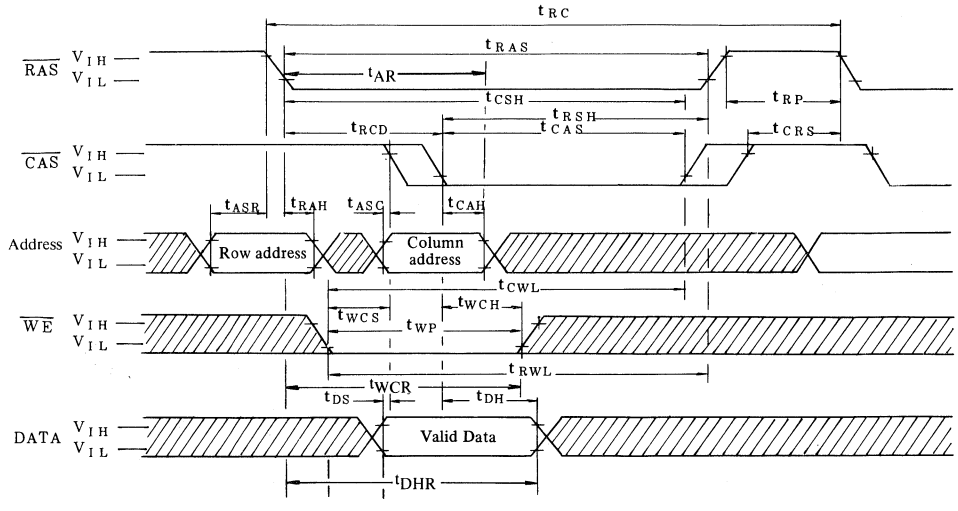


OE WRITE CYCLE

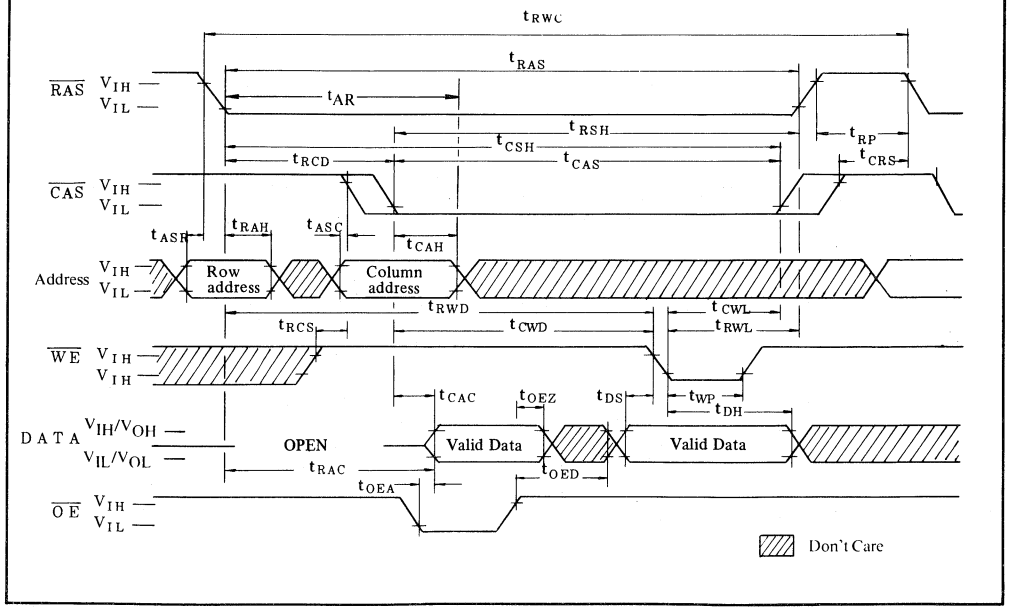


WRITE CYCLE (EARLY WRITE)

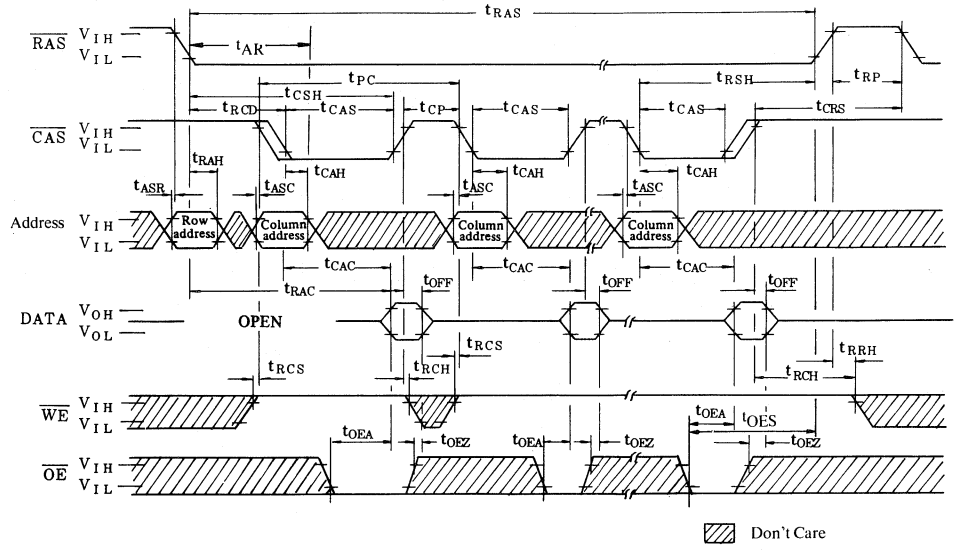
Note: $\overline{OE}$ not dependent on the high or low level.



READ/WRITE AND READ MODIFY WRITE CYCLE

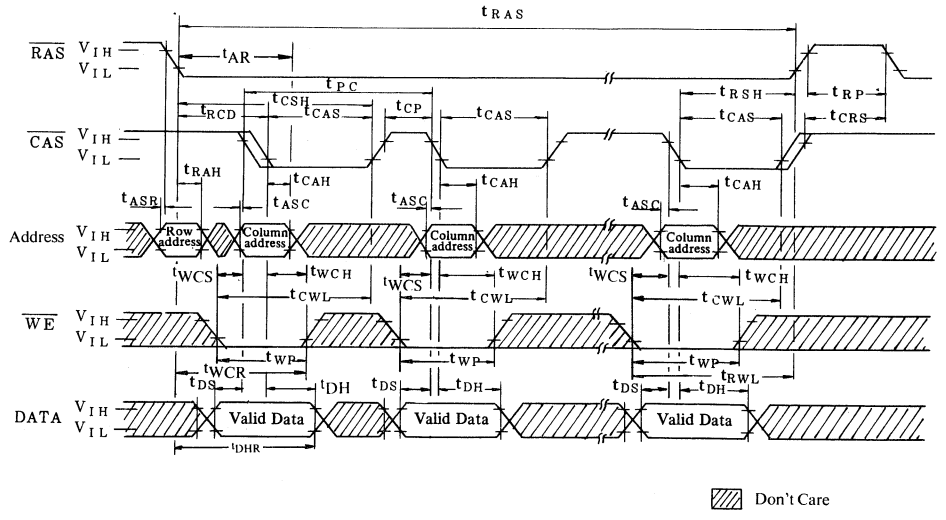


PAGE MODE READ CYCLE

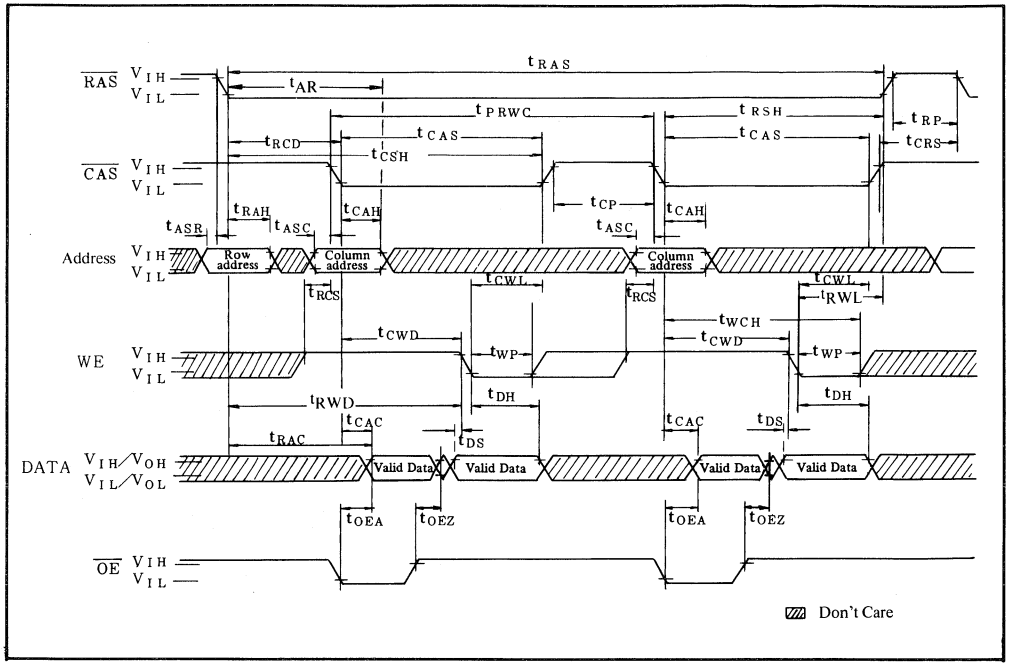


PAGE MODE WRITE CYCLE (EARLY WRITE)

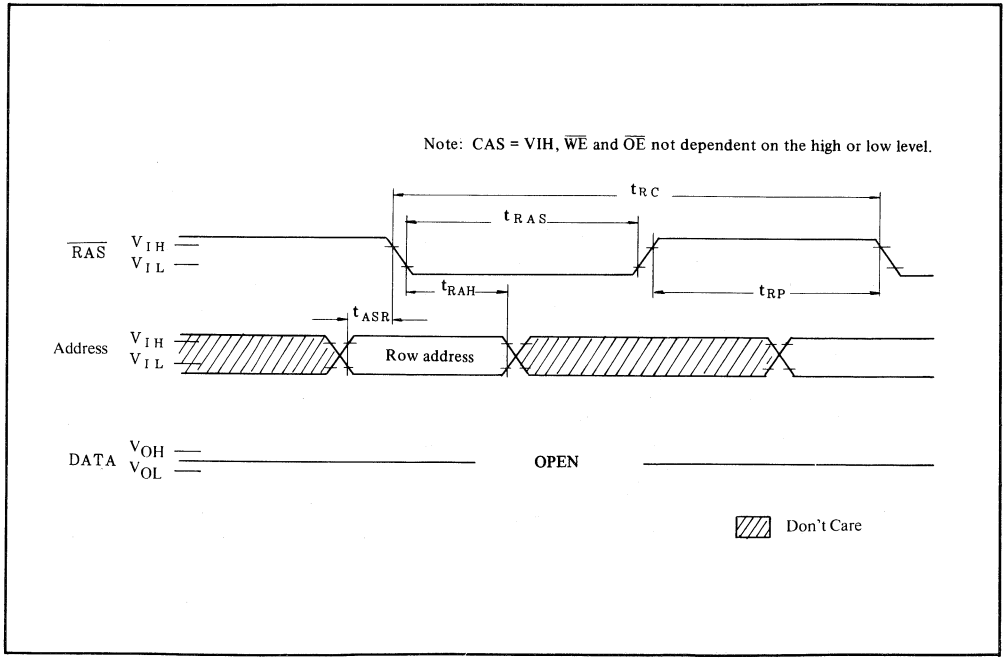
Note: $\overline{OE}$ not dependent on the high or low level.



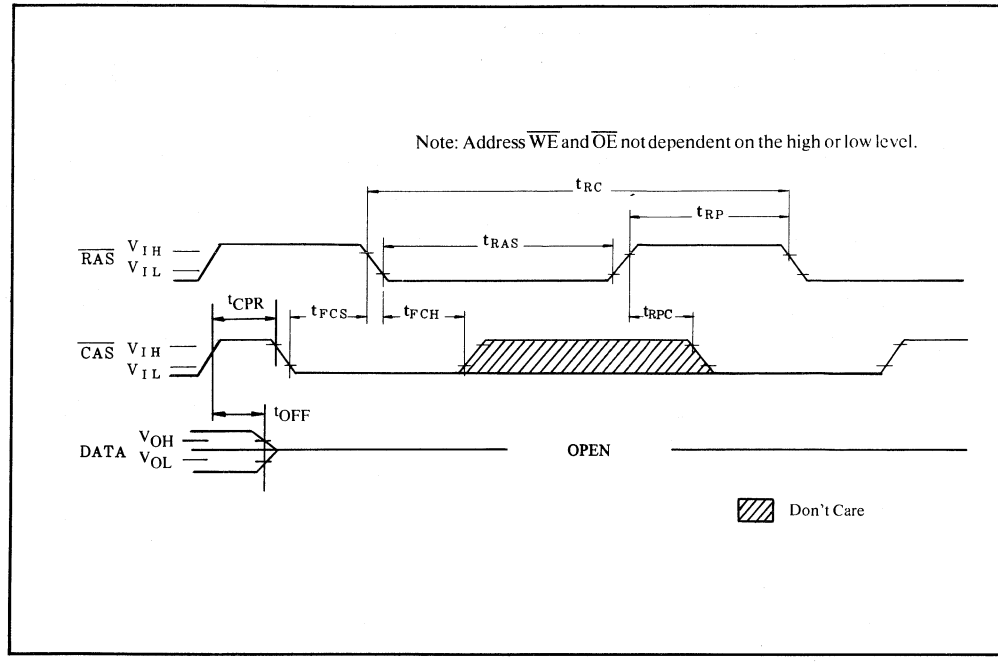
PAGE MODE READ/WRITE CYCLE



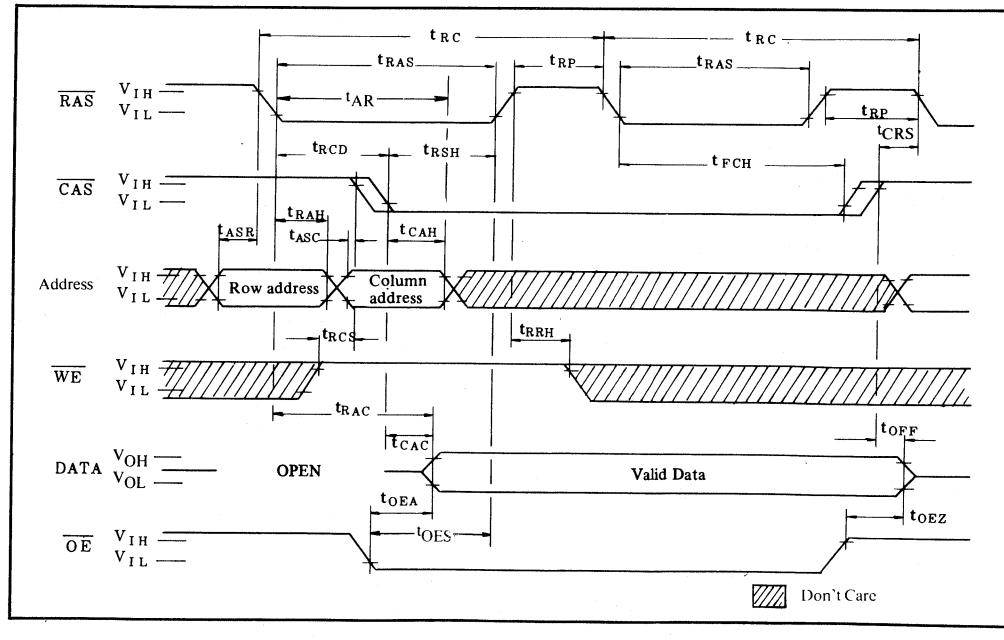
RAS ONLY REFRESH CYCLE



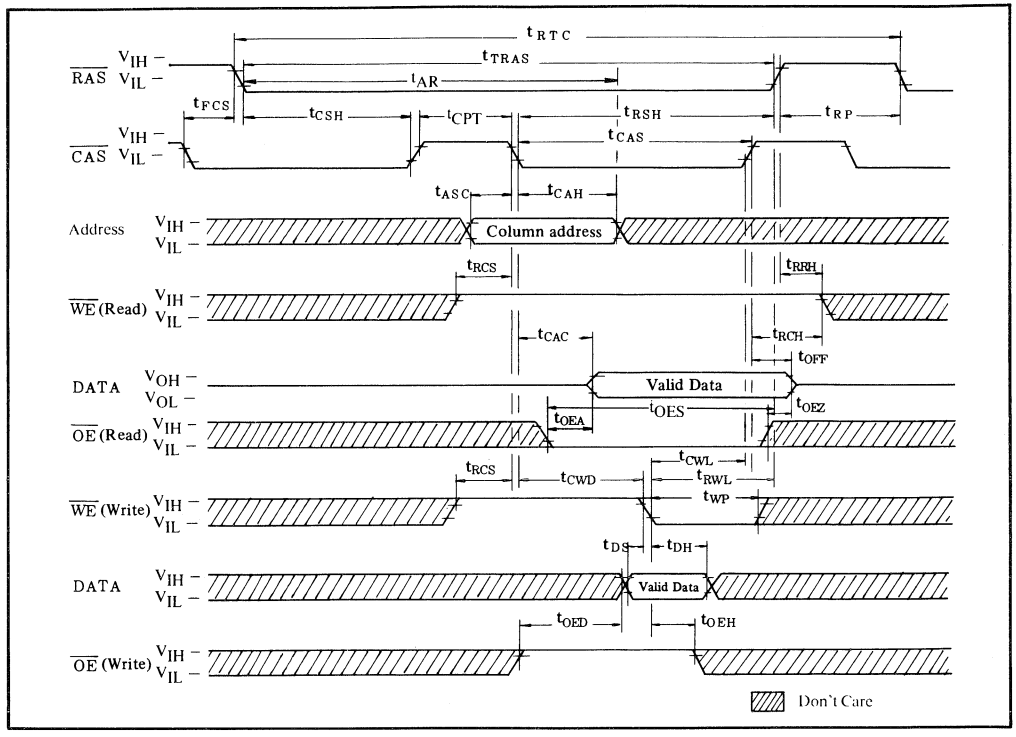
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

18 bits of binary address input are required to decode any one of the 262,144 words by 4 bits storage cell locations.

9 row-address bits are set up on address input pins A0 through A8 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 9 column-address bits are set up on pins A0 through A8 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval

t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ is low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{CAS}$ or $\overline{OE}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every eight milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_8 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 512 row addresses.
(3) By using $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 512 times, and highs are written into the 512 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

OKI semiconductor

MSM411000RS

1,048,576-WORD × 1-BIT DYNAMIC RAM

GENERAL DESCRIPTION

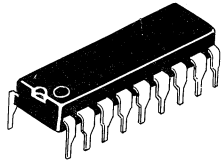
The MSM411000RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM411000RS is OKI's N channel silicon gate MOS process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

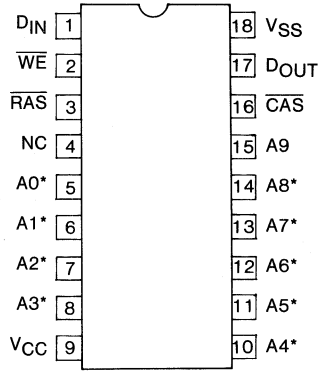
- Silicon gate, tripple polysilicon NMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Stand By (MAX)
MSM411000-10RS	100 ns	200 ns	413 mW	28 mW
MSM411000-12RS	120 ns	230 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



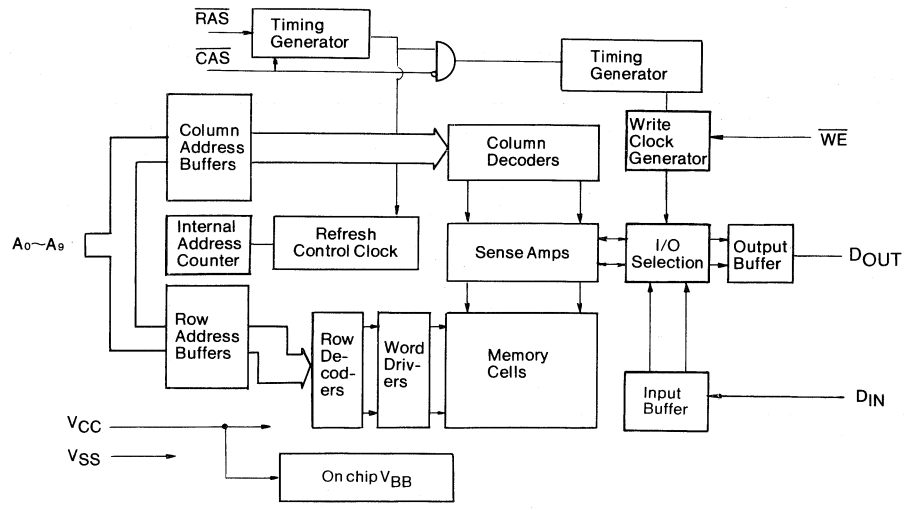
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 411000-10		MSM 411000-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	–	2.4	–	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	–	0.4	–	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	–	5	–	5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min	–	65	–	60	mA	
Average power supply current* (Page mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	–	55	–	50	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	65	–	60	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	10	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSM411000-10		MSM411000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Read/write cycle time	t_{RWC}	235	–	255	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	10
Write command hold time from $\overline{RAS}$	t_{WCR}	70	–	85	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	9
Write command hold time	t_{WCH}	20	–	25	–	ns	

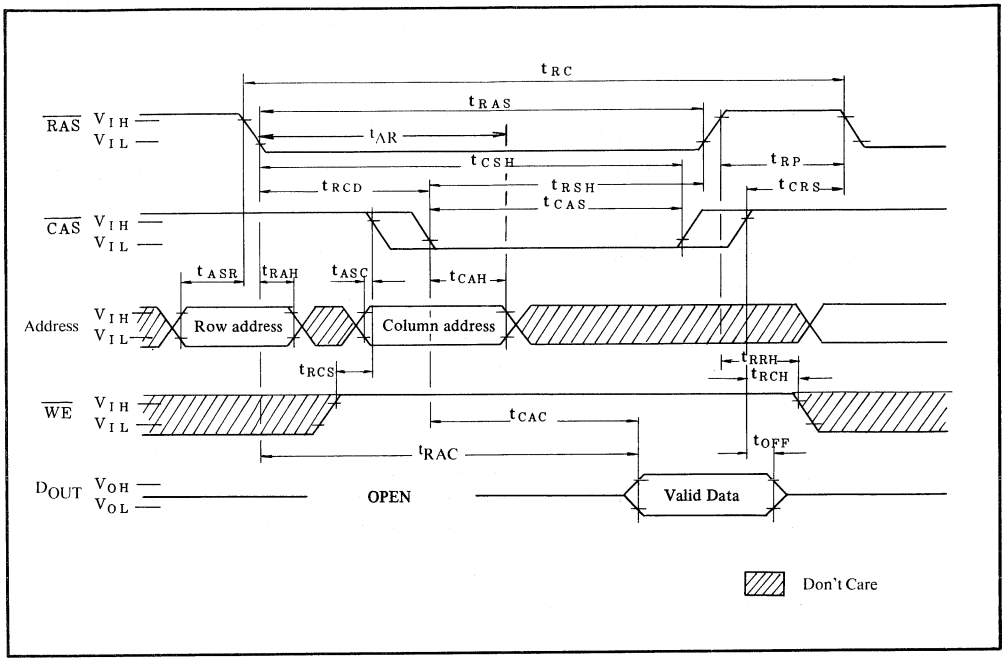
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM411000-10		MSM411000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	70	–	85	–	ns	
CAS to $\overline{WE}$ delay	t_{CWD}	40	–	40	–	ns	9
RAS to $\overline{WE}$ delay	t_{RWD}	90	–	100	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	10
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
Read/write cycle (Refresh counter test)	t_{RTC}	355	–	385	–	ns	11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	255	10000	275	10000	ns	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	11
Read/write cycle time (Page mode)	t_{PRWC}	135	–	145	–	ns	

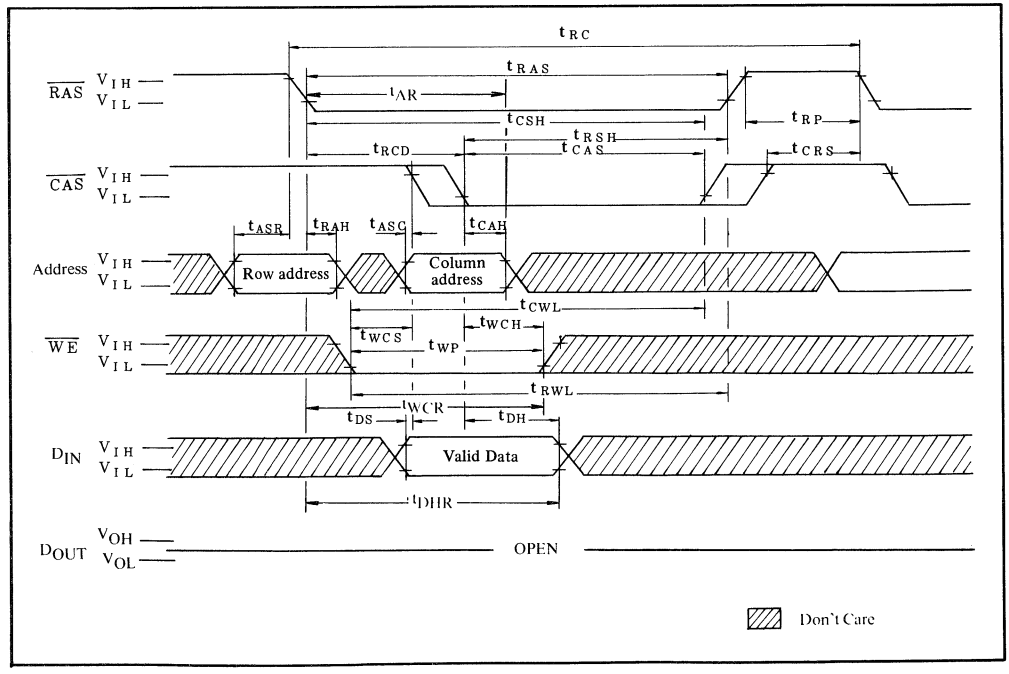
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{ t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) $= t_{RAH}$ (Min.) $+ 2t_T + t_{ASC}$ (Min.).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

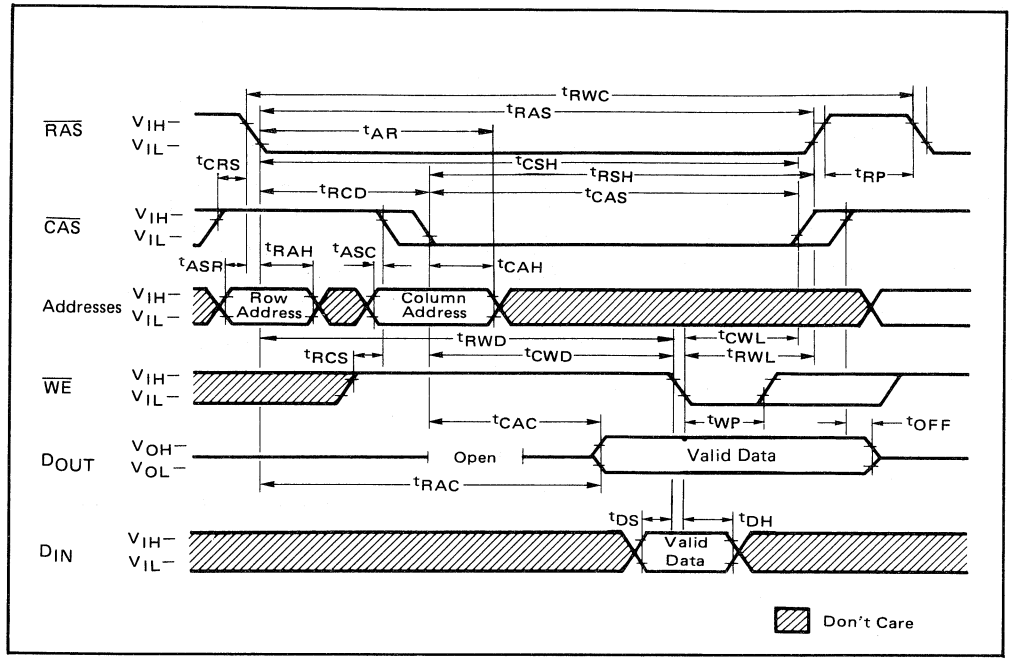
READ CYCLE



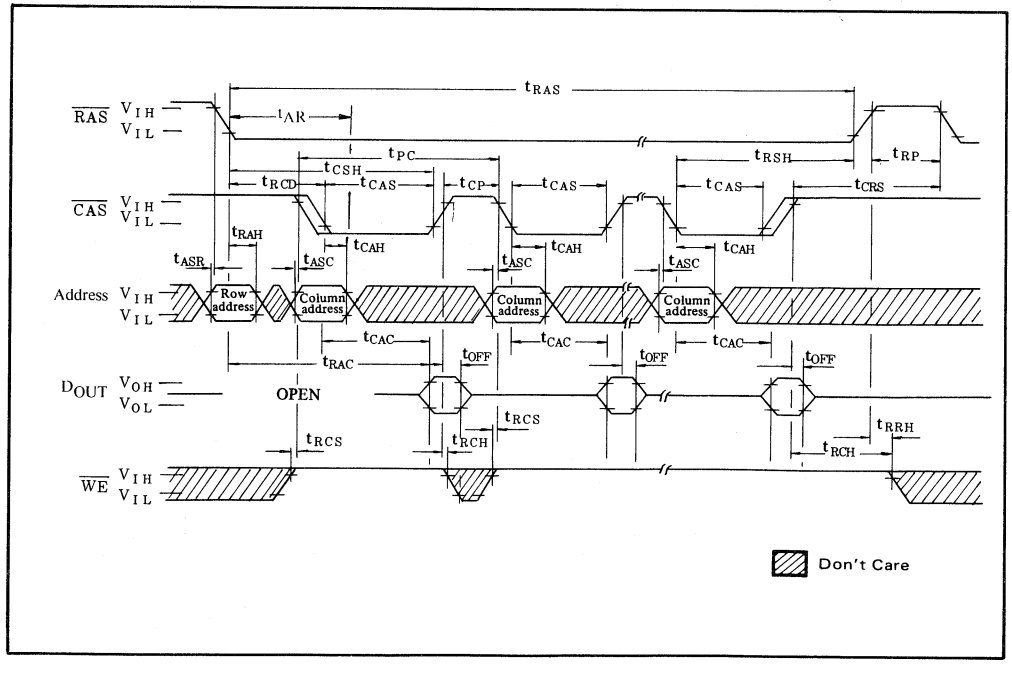
WRITE CYCLE (EARLY WRITE)



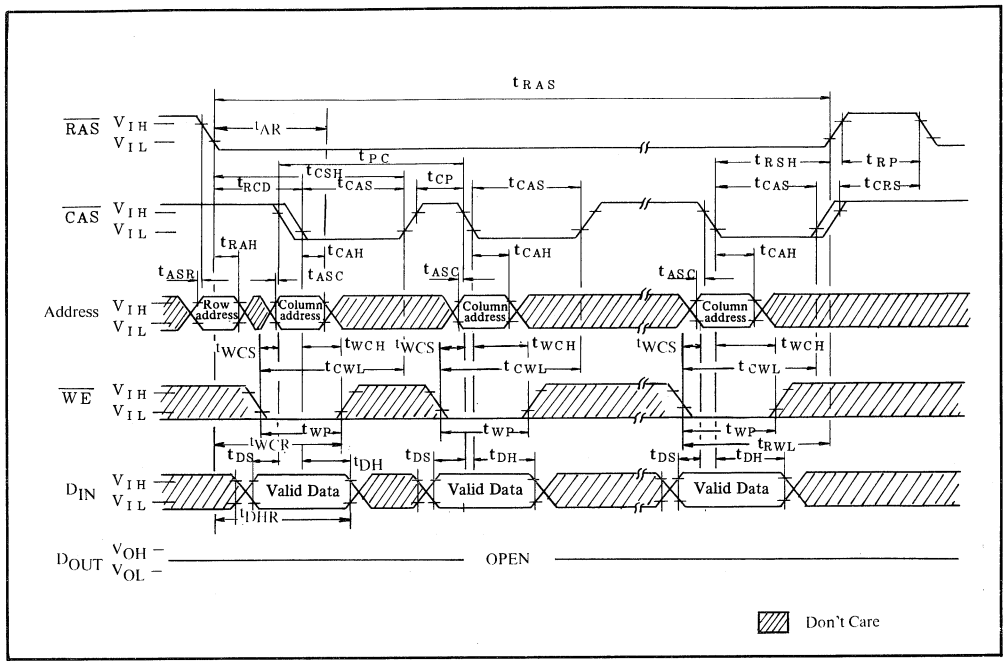
READ/WRITE AND READ MODIFY WRITE CYCLE



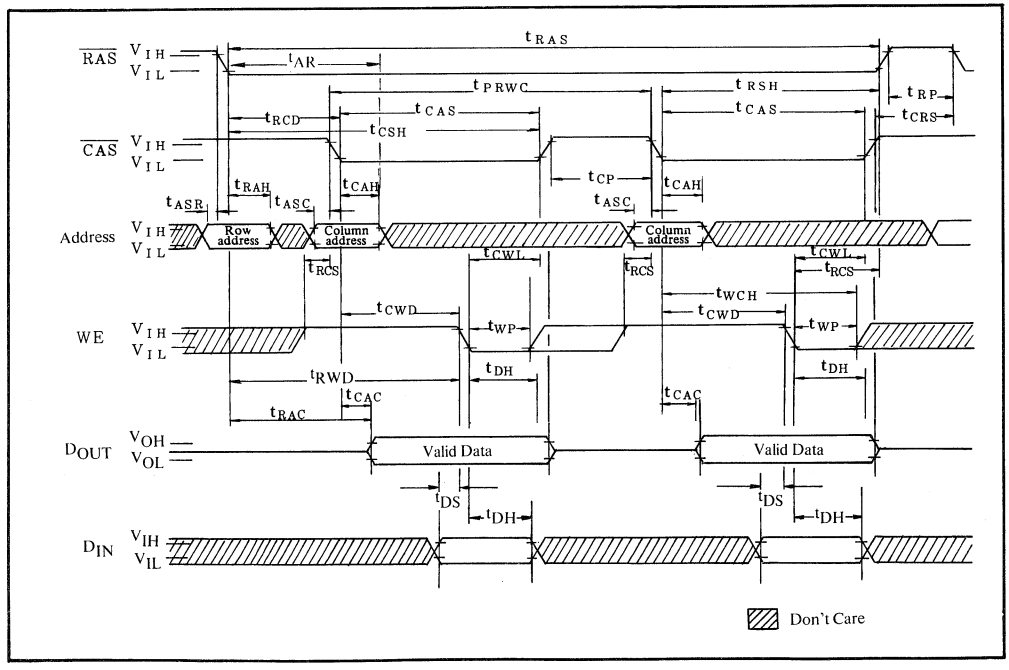
PAGE MODE READ CYCLE



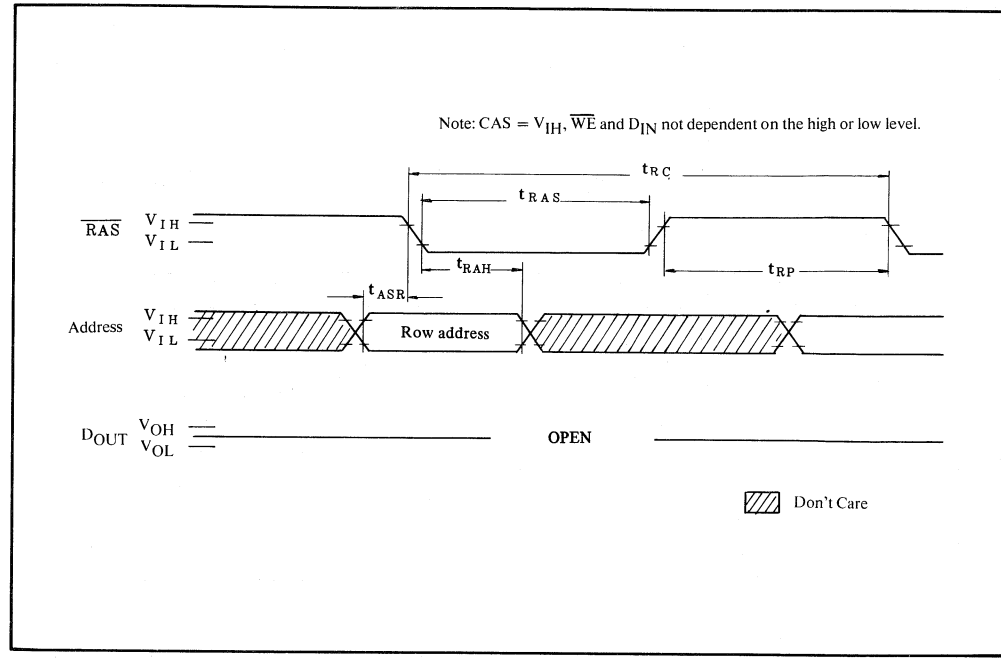
PAGE MODE WRITE CYCLE (EARLY WRITE)



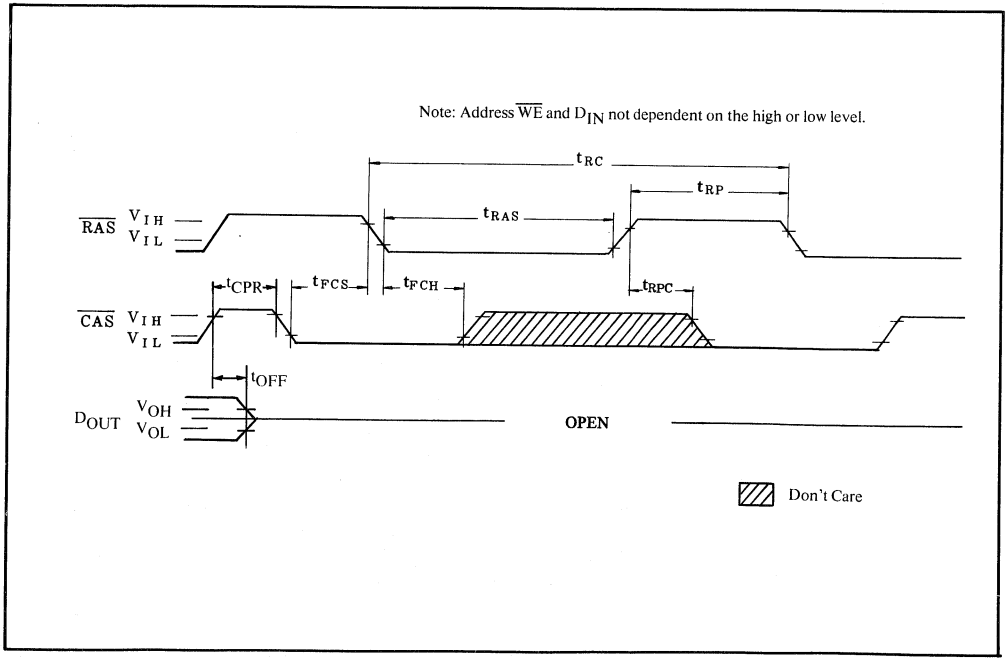
PAGE MODE READ/WRITE CYCLE



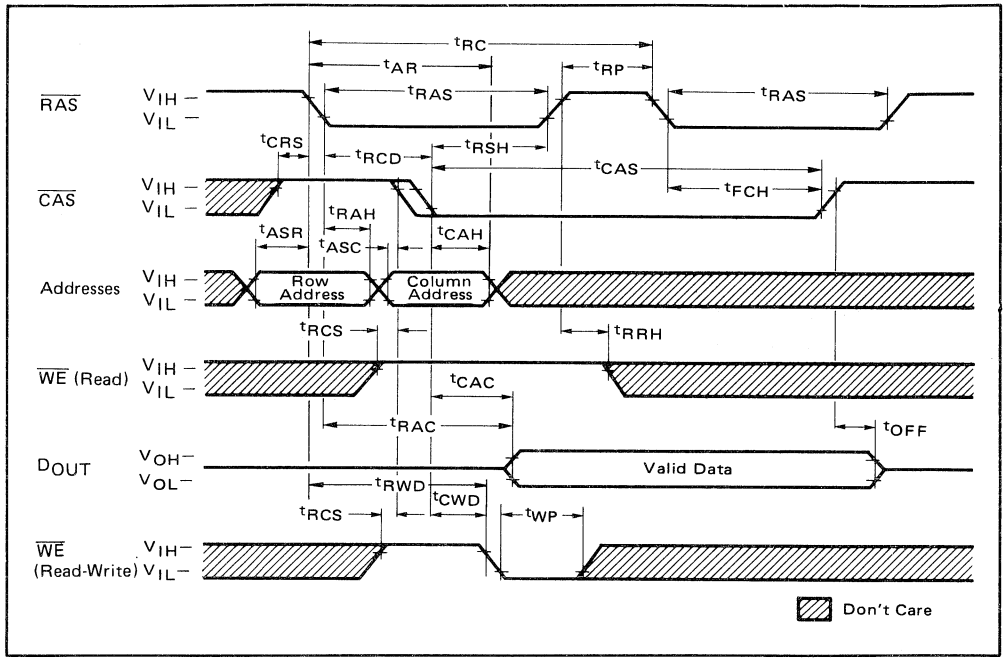
$\overline{RAS}$ ONLY REFRESH CYCLE



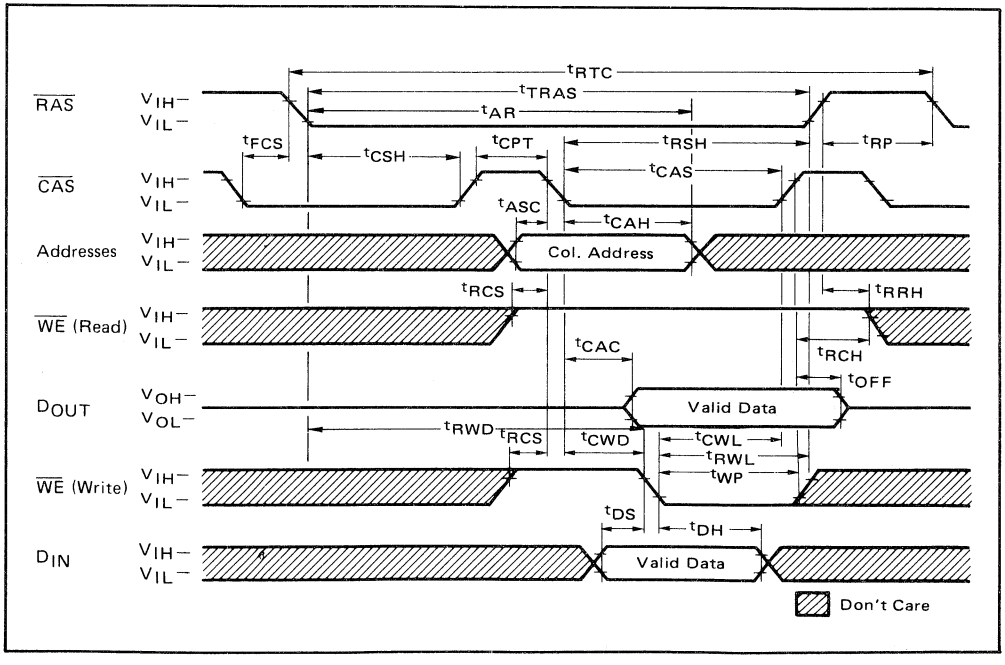
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

20 bits of binary address input are required to decode any one of the 1,048,576 words by 1 bit storage cell locations.

10 row-address bits are set up on address input pins A0 through A9 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 10 column-address bits are set up on pins A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every 8 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (9 bits) and a column address (10 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_8 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_9 are defined by latching levels on A_0 through A_9 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.

(2) Write a test pattern of lows into memory cells at a single column address and 512 row addresses.

(3) By using $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 512 times, and highs are written into the 512 memory cells.

(4) Read the high written at the last operation (Step (3)).

(5) Complement the test pattern and repeat the steps (2), (3) and (4).

OKI semiconductor

MSM411001RS

1,048,576-BIT DYNAMIC RANDOM ACCESS MEMORY < Nibble Mode Type >

GENERAL DESCRIPTION

The Oki MSM411001 is a fully decoded, dynamic NMOS random access memory organized as 1048576 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

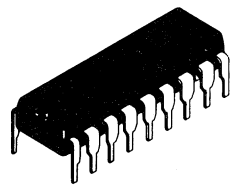
Multiplexed row and column address inputs permit the MSM411001 to be housed in a standard 18 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM411001 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability, also features "nibble mode" which allows high speed serial access to up to 4 bits of data.

The MSM411001 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

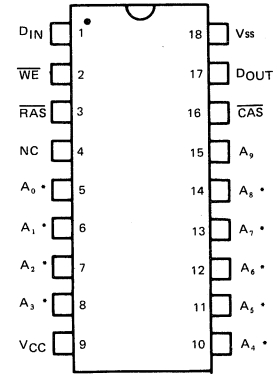
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 1048576 x 1 RAM, 18 pin package
- Silicon-gate, Tripple Poly NMOS, single transistor cell
- Row access time
  100 ns max (MSM411001-10RS)
  120 ns max (MSM411001-12RS)
- Cycle time
  200 ns min (MSM411001-10RS)
  230 ns min (MSM411001-12RS)
- Low power:
  413 mW/28 mW (MSM411001-10RS)
  385 mW/28 mW (MSM411001-12RS)
- Single+5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Gated $\overline{CAS}$
- 8ms/512 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability



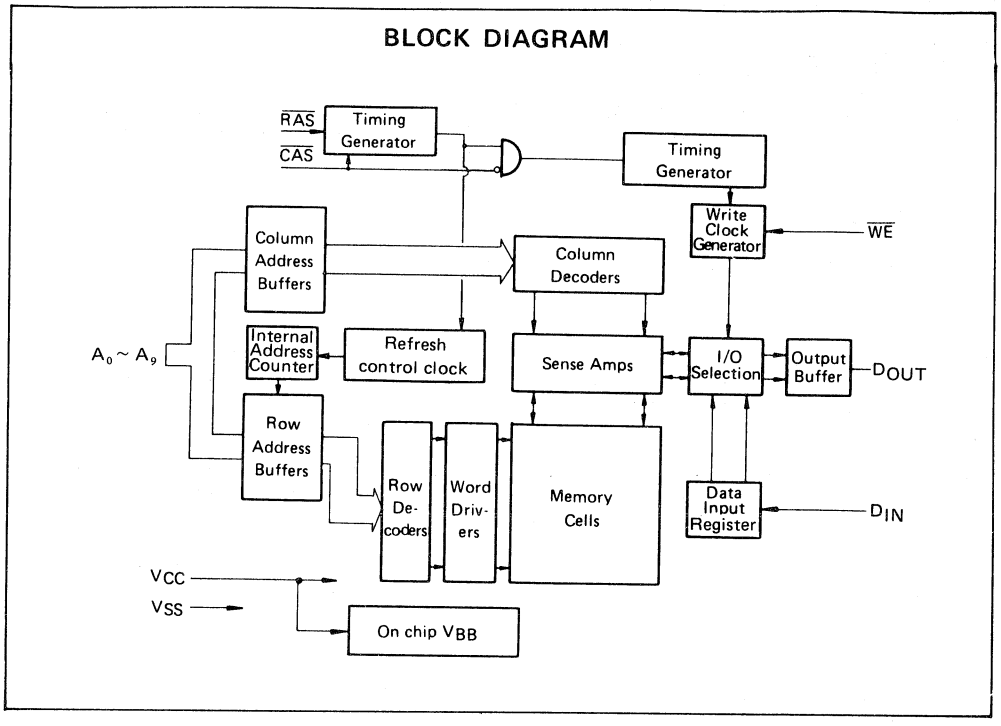
PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSM411001-10		MSM411001-12		Unit	Notes
		Min	Max	Min	Max		
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	–	75	–	70	mA	
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	5	–	5	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}	–	65	–	60	mA	
Nibble MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	I_{CC4}	–	35	–	30	mA	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}	–	65	–	60	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	-10	10	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	-10	10	-10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = -5 mA)	V_{OH}	2.4	–	2.4	–	V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	–	0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_9, D_{IN})	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noded.)

Parameter	Symbol	Unit	MSM411001 10		MSM411001 12		Notes
			Min	Max	Min	Max	
Refresh period	t_{REF}	ms		8		8	
Random read or write cycle time	t_{RC}	ns	200		230		
Read-write cycle time	t_{RWC}	ns	235		255		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	25	0	25	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10 μs	120	10 μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10 μs	60	10 μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	15		20		
Row address set-up time	t_{ASR}	ns	0		0		
Row address hold time	t_{RAH}	ns	15		15		
Column address set-up time	t_{ASC}	ns	0		0		
Column address hold time	t_{CAH}	ns	20		20		
Column address hold time from $\overline{RAS}$	t_{AR}	ns	70		80		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		
Write command hold time from $\overline{RAS}$	t_{WCR}	ns	70		85		
Write command set-up time	t_{WCS}	ns	0		0		8
Write command pulse width	t_{WP}	ns	20		25		
Write command hold time	t_{WCH}	ns	20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		40		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		40		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	20		25		
Data-in hold time from $\overline{RAS}$	t_{DHR}	ns	70		85		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	40		40		8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	ns	90		100		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	30		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		
Nibble mode read/write cycle time	t_{NC}	ns	65		70		9
Nibble mode read-write cycle time	t_{NRWC}	ns	65		70		9
Nibble mode access time	t_{NCAC}	ns		30		35	9
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	30		35		9

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM411001 10		MSM411001 12		Notes
			Min	Max	Min	Max	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	ns	25		25		9
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	ns	40		40		9
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	ns	40		40		9
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	20		20		9
Refresh counter test cycle time	t_{RTC}	ns	355		385		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	255	10,000	275	10,000	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		10

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2) AC measurements assume t_T = 5 ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} \leqq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

5) Assumes that $t_{RCD} \geqq t_{RCD}$ (max.)

6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

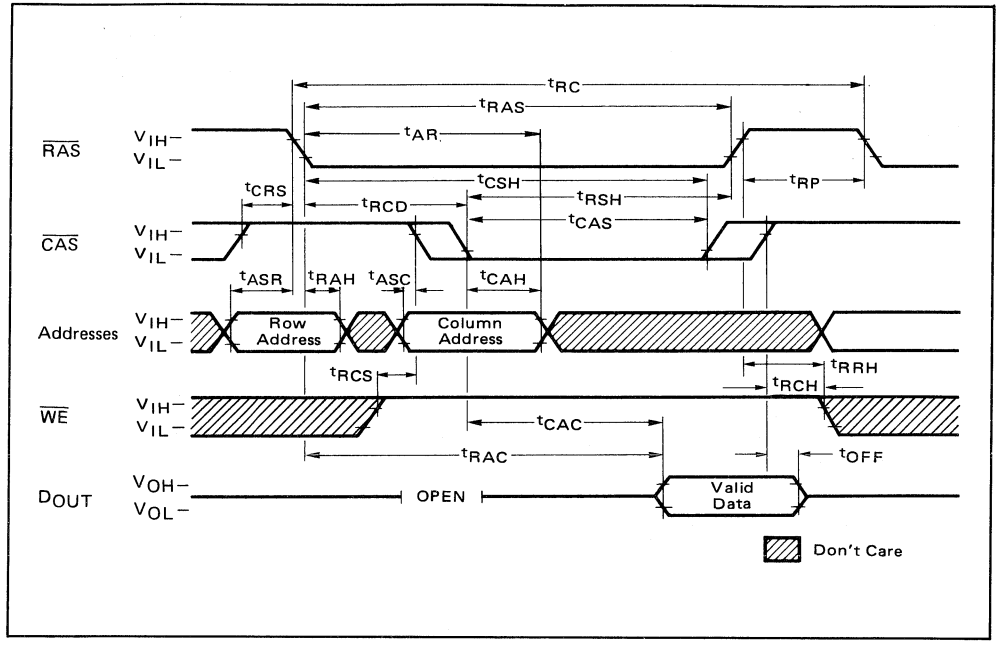
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data dheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$(min.), and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at acccess time) is indeterminate.

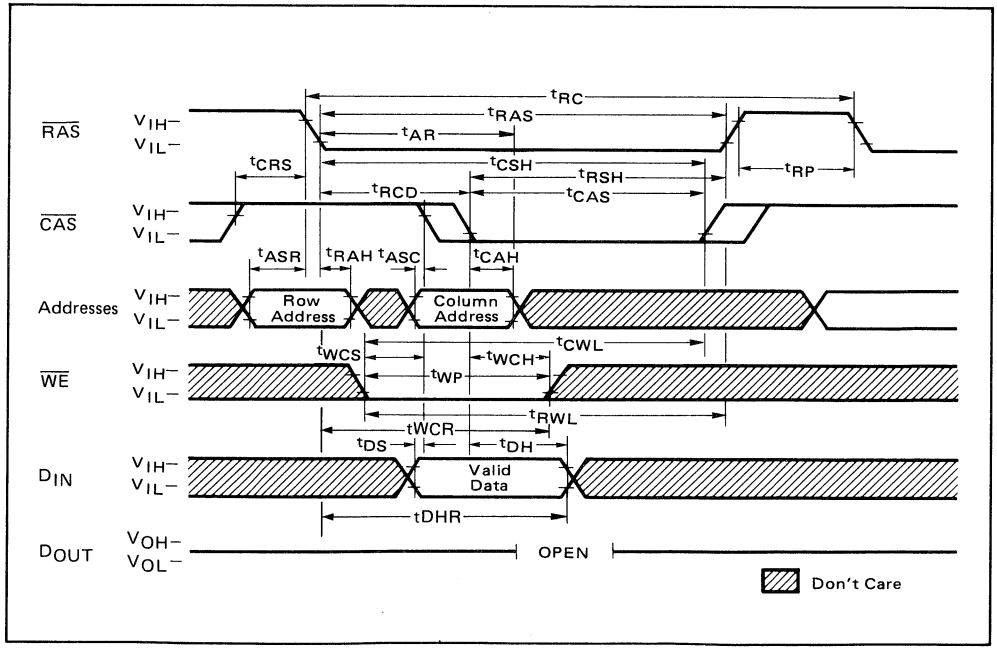
9) Nibble mode cycle.

10) $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

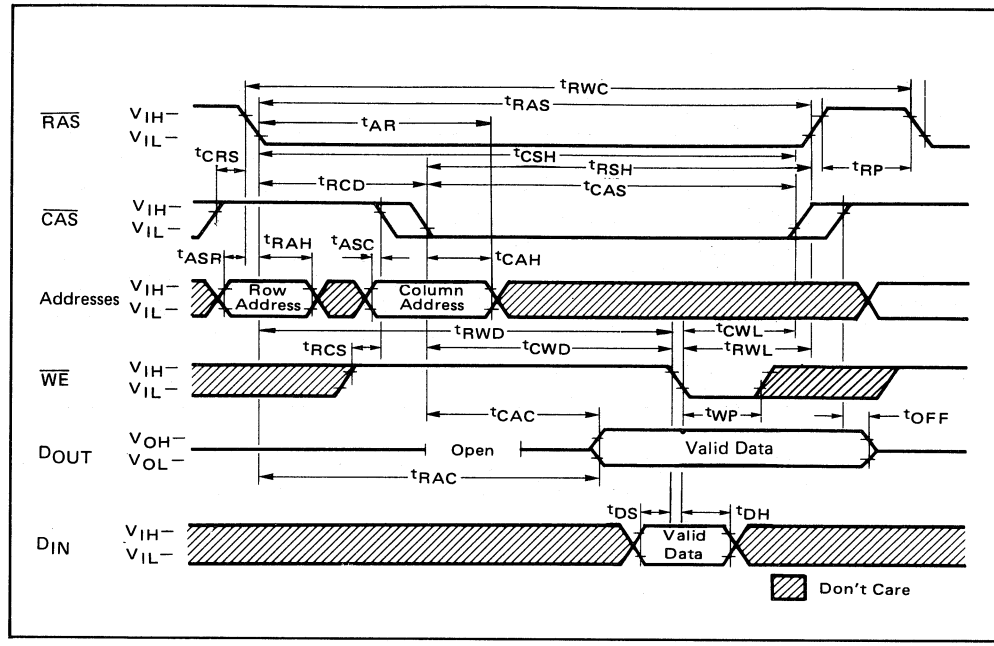
READ CYCLE



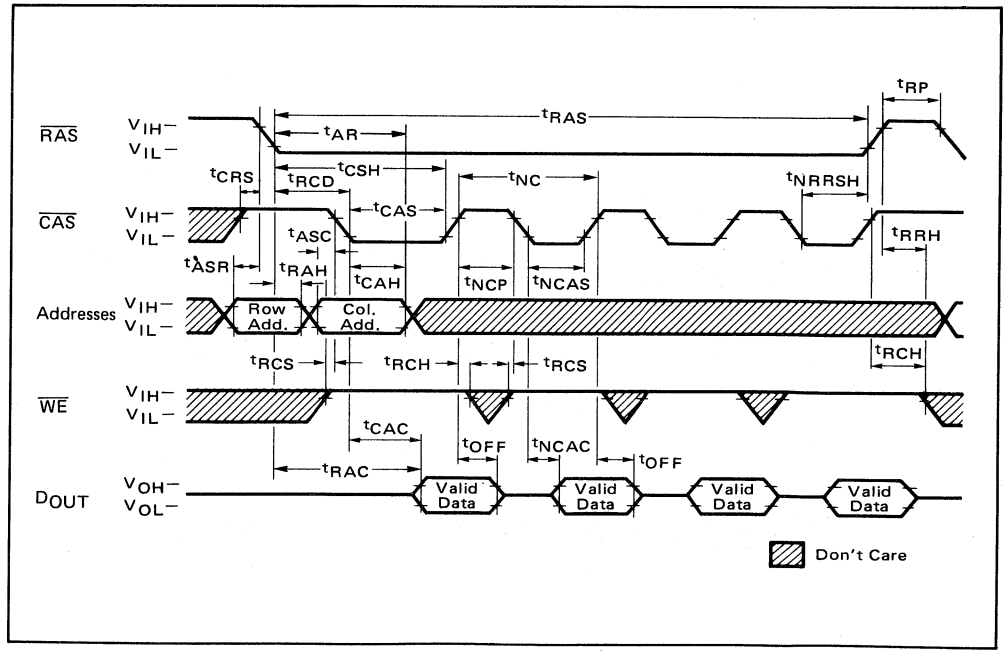
WRITE CYCLE (EARLY WRITE)



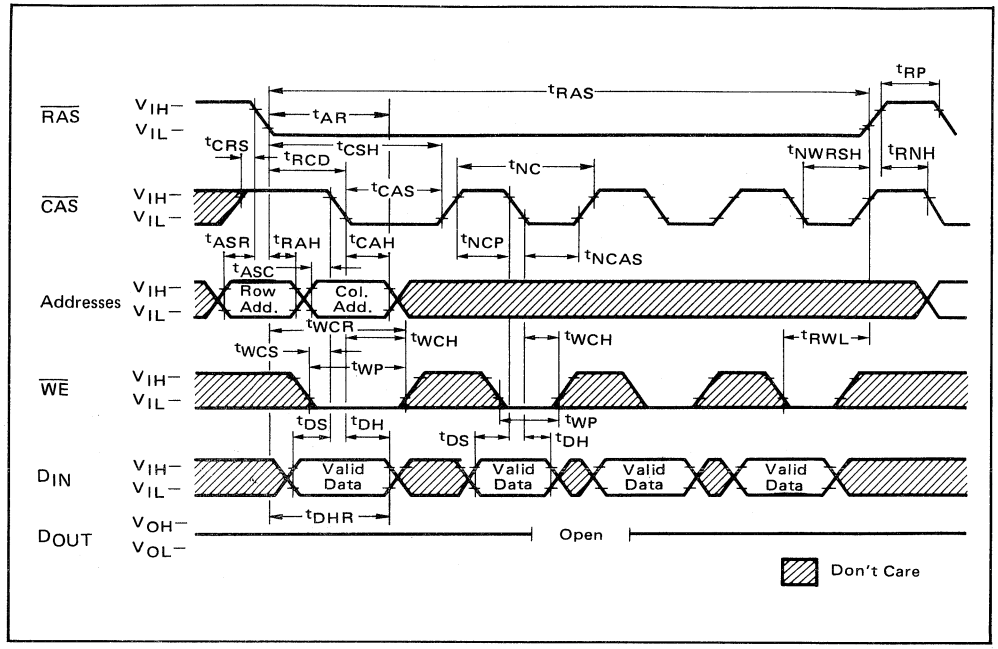
READ-WRITE/READ-MODIFY-WRITE CYCLE



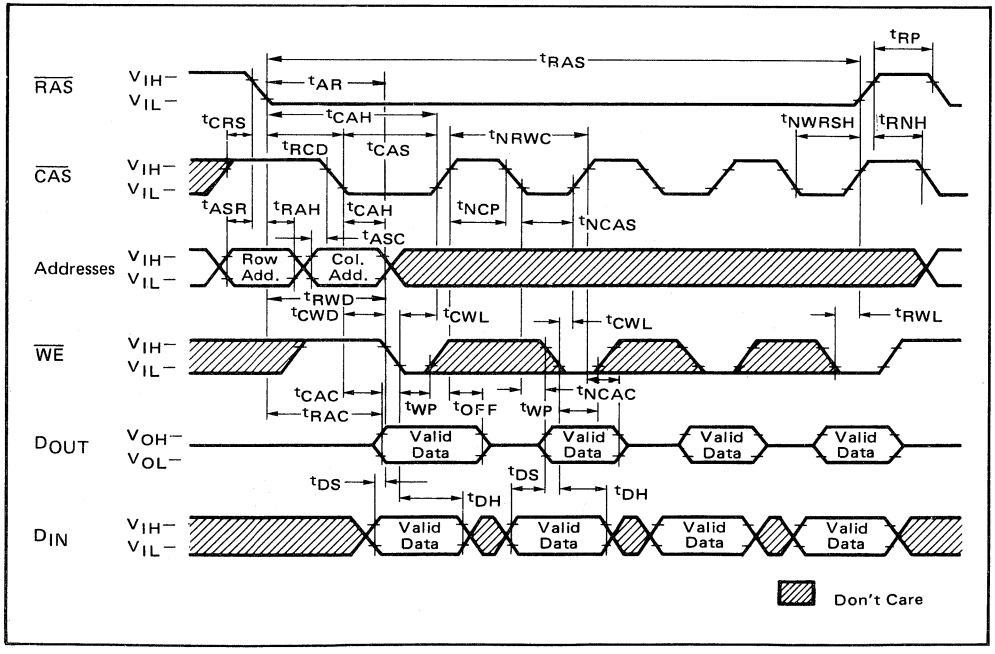
NIBBLE MODE READ CYCLE



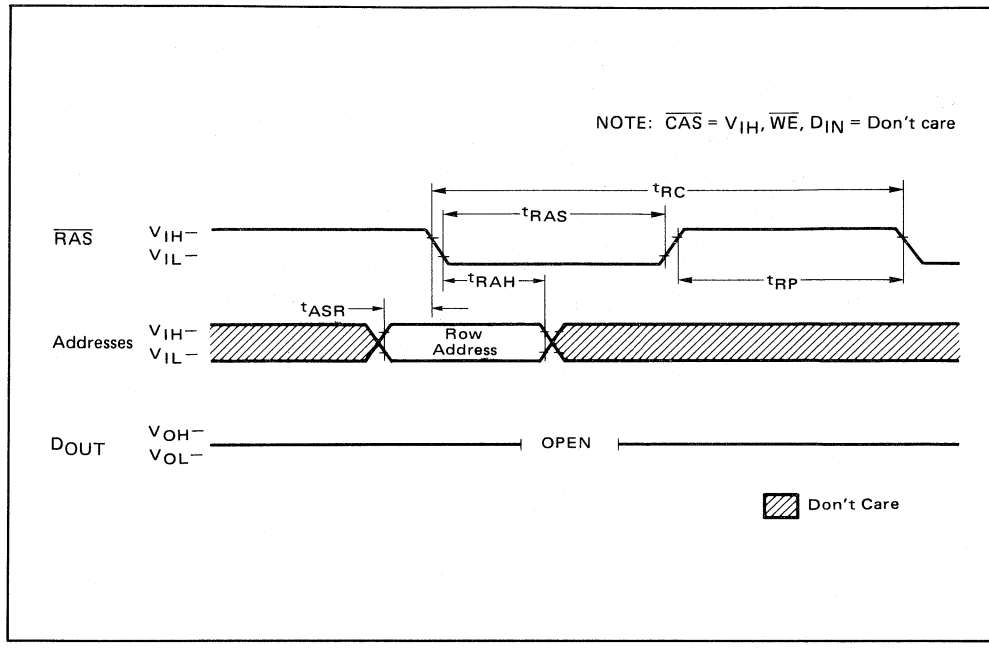
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



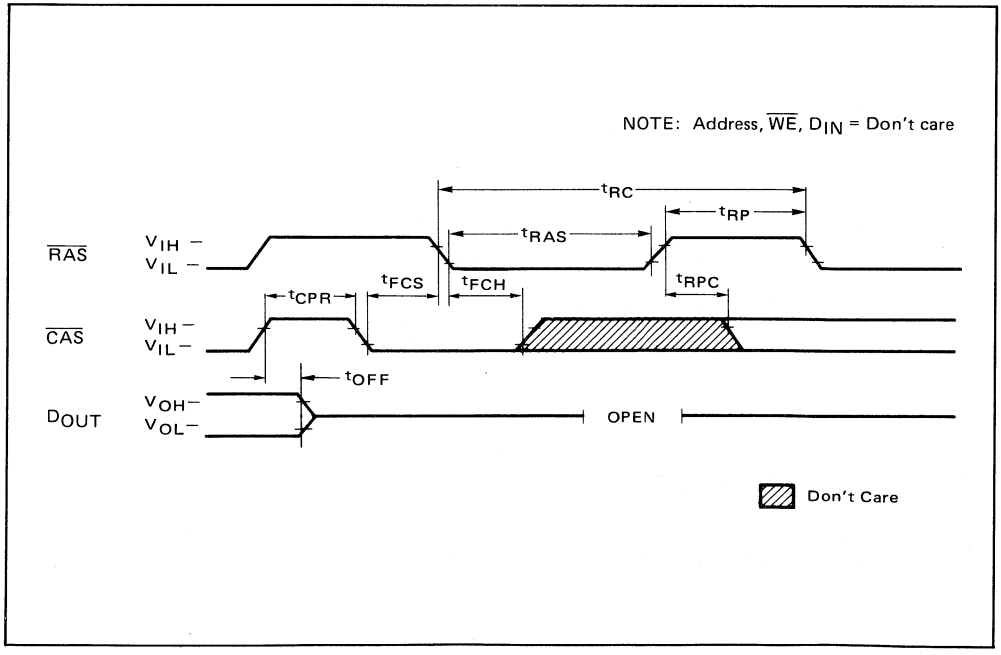
NIBBLE MODE READ-WRITE CYCLE



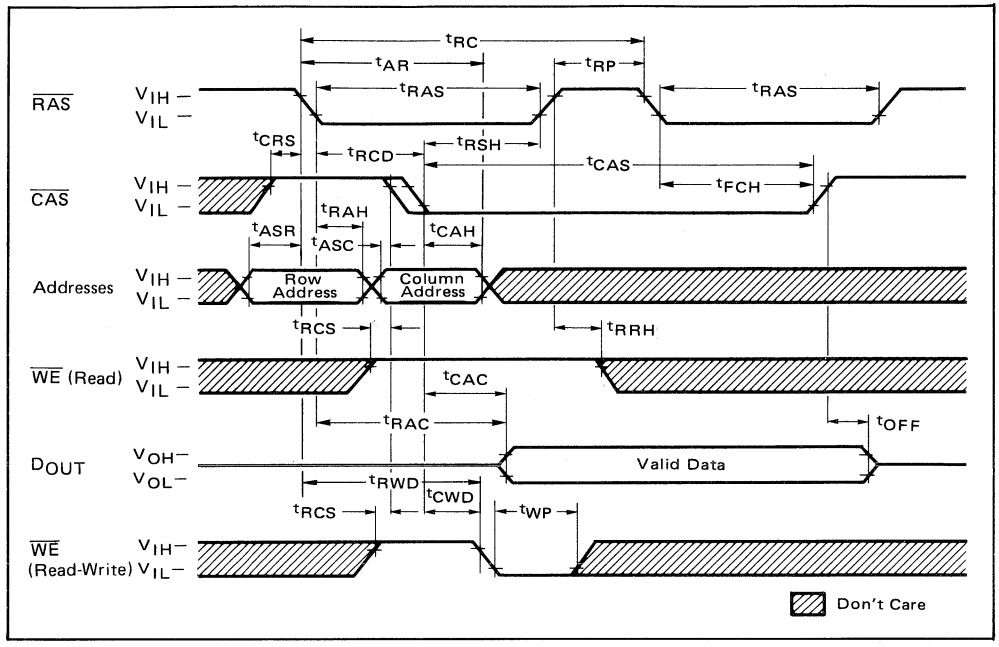
$\overline{RAS}$ ONLY REFRESH CYCLE



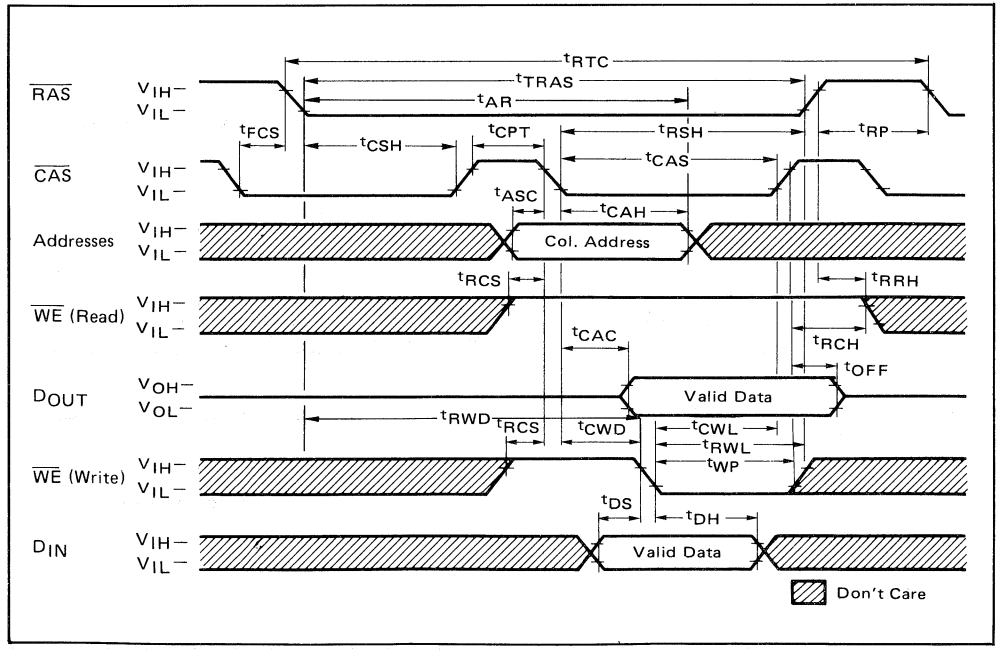
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DESCRIPTION

Simple Timing Requirement

The MSM411001 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM411001 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM411001 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM411001 can commit better memory system through-put during operations in an inter-leaved system.

Fast Read- While-Write cycle

The MSM411001 has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM411001 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM411001 goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs

A total of twenty binary input address bits are required to decode any 1 of 1048576 storage cell locations within the MSM411001. Nine row-address bits are established on the input pins (A_0 through A_9) and latched with the Row Address Strobe ($\overline{RAS}$). Then ten column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of RAS. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MSM411001 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transistion of $\overline{RAS}$ when t_{RCD}(max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row addresses and the 9 column addresses. The 2 bits of addresses (CA_9 RA_9) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_9 and CA_9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_9	ROW ADDRESS	CA_9	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	101010101	0	101010101	----- input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	101010101	0	101010101	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	0	101010101	1	101010101	
toggle $\overline{CAS}$ (nibble mode)	4	1	101010101	1	101010101	
toggle $\overline{CAS}$ (nibble mode)	1	0	101010101	0	101010101	sequence repeats

$\overline{RAS}$ only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 through A_8) at least every 8 millisecond. $\overline{RAS}$ only refresh avoids any output during refresh because the buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 512 row-addresses (A_0 through A_8) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM411001 offers an alternate refresh method. If $\overline{CAS}$ is held on "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM411001 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always "low" when $\overline{RAS}$ goes to "low" in hidden refresh.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activted circuitry.

As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to "high" and goes to "low" again while $\overline{RAS}$ is held "low", the read and write operations are enabled. A memory cell address (consisting of a row address (10 bits) and a column address (10 bits)) to be accessed can be defined as follows:

* A ROW ADDRESS – Bits A_0 through A_8 are defined by the refresh counter.
  The other bit A_9 is set "high" internally.
* A COLUMN ADDRESS – All the bits A_0 through A_9 are defined by latching levels on A_0 throgh A_9 at the second falling edge of CAS.

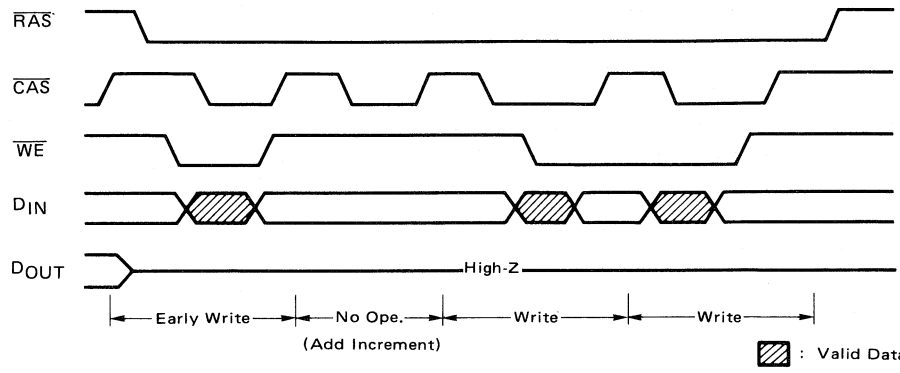
Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure

The timing as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle is used for all the operations described as follows:

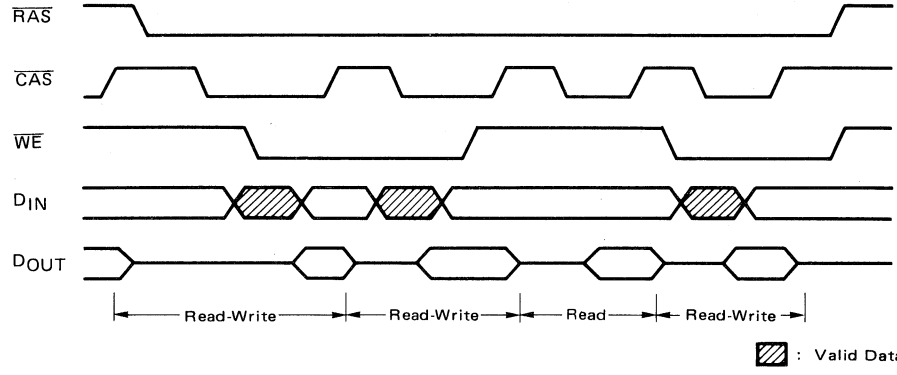
(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
(2) Write a test pattern of data "low" into memory cells at a single column address and 512 row addresses.
(3) By using $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test cycle, read the "low" written at the last operation (Step (2)) and write a new data "high" in the same cycle. This cycle is repeated 512 times, and data "high" are written into the 512 memory cells.
(4) Read the data "high" written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

NIBBLE MODE

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geqq t_{CWD}$ (min)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$ Only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Preliminary

OKI semiconductor

MSM511000RS

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

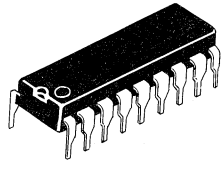
The MSM511000RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511000RS is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

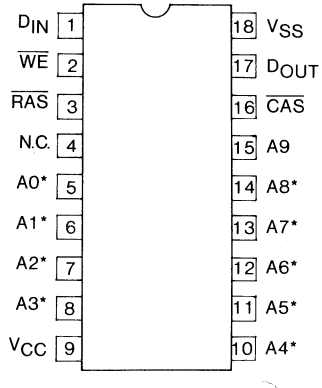
- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511000-10RS	100 ns	190 ns	385 mW	5.5 mW
MSM511000-12RS	120 ns	220 ns	330 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



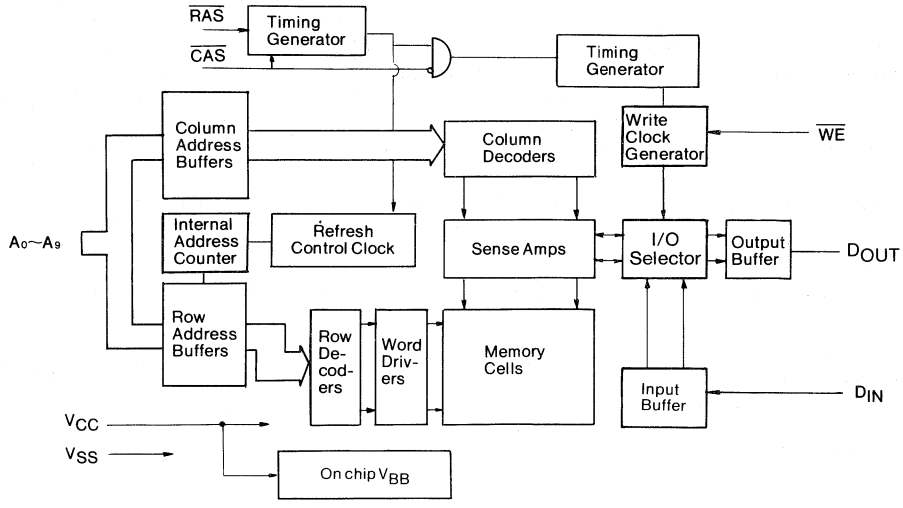
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 511000-10		MSM 511000-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	70	–	60	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hz — TTL	–	2	–	2	mA	
		$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hz — MOS	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	–	70	–	60	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	70	–	60	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min	–	50	–	45	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM511000-10		MSM511000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	190	–	220	–	ns	
Read/write cycle time	t_{RWC}	220	–	255	–	ns	
Fast page mode cycle time	t_{PC}	55	–	70	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	85	–	105	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	35	–	45	ns	4, 5
Access time from column address	t_{AA}	–	50	–	60	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	65	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	25	0	35	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	35	–	45	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	10000	15	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	35	–	45	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	65	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	25	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	–	90	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50	–	60	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM511000-10		MSM511000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	20	–	25	–	ns	
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	30	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	35	–	45	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100	–	120	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	60	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	15	–	20	–	ns	

Notes:

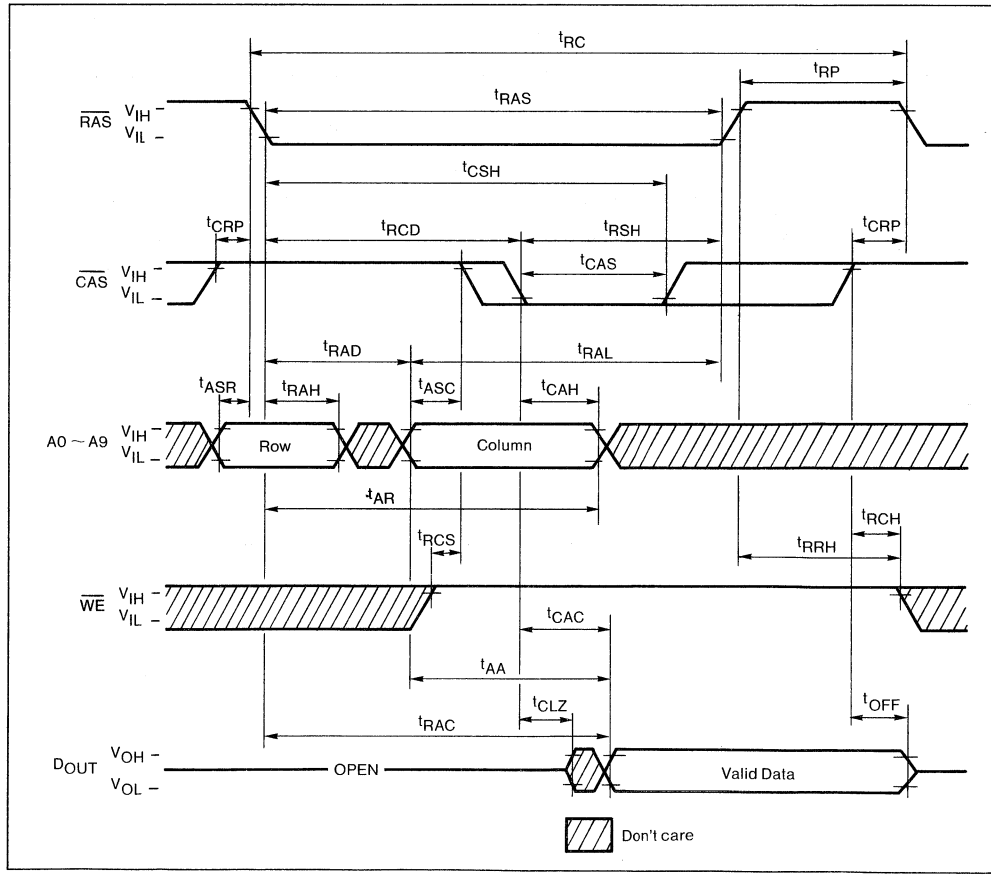
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

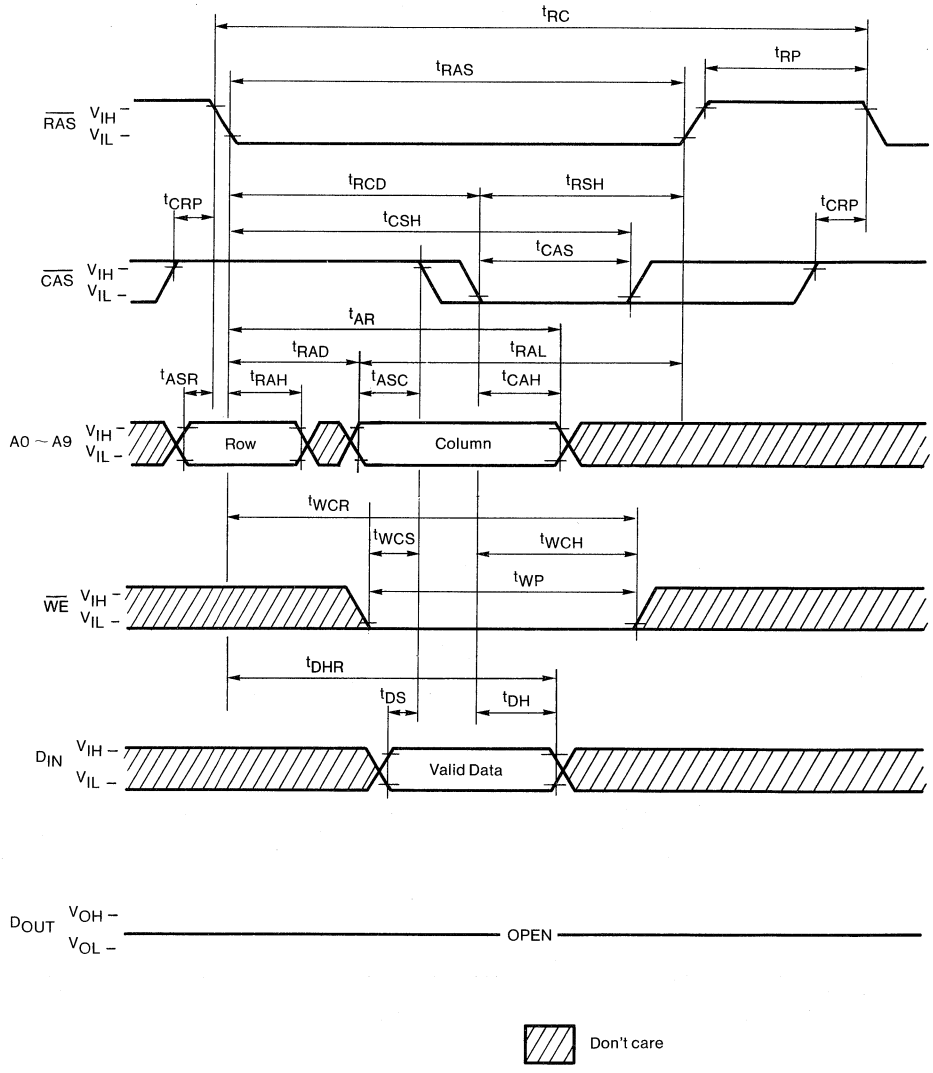
7 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

8 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

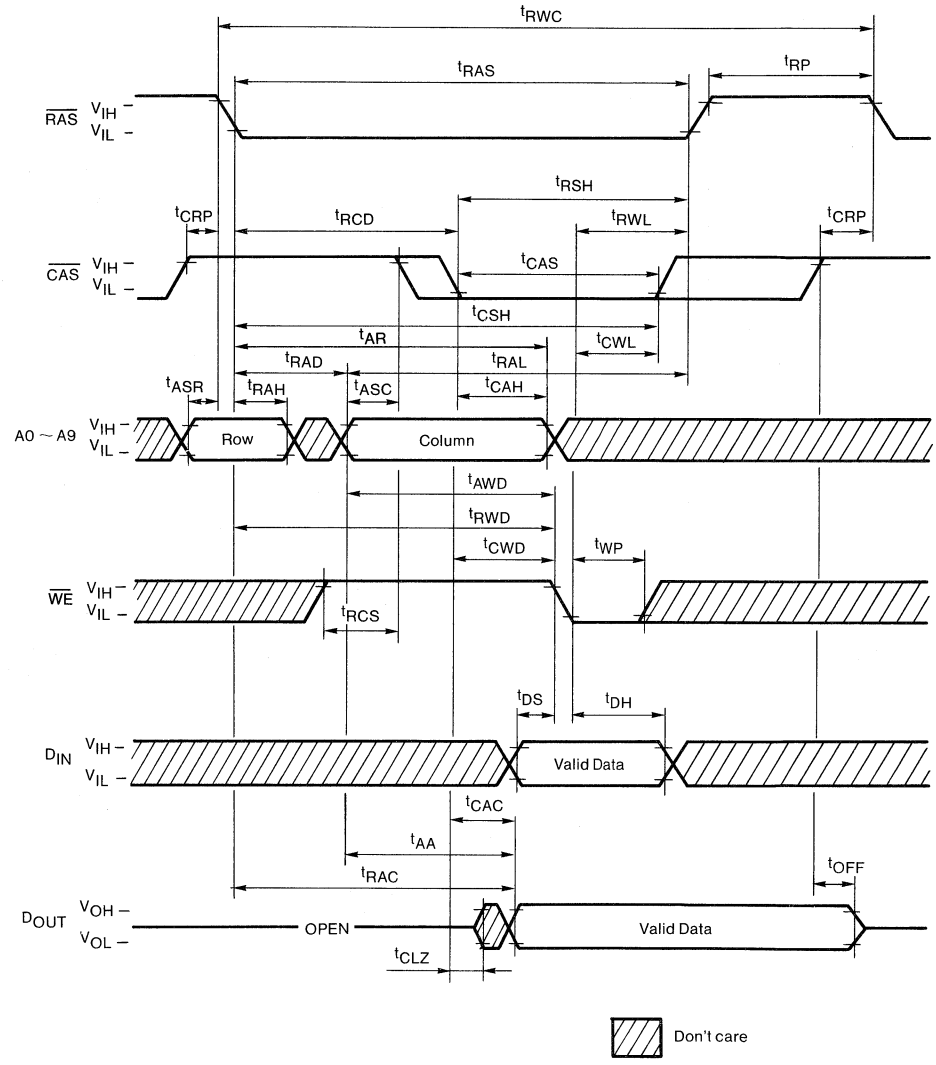
READ CYCLE



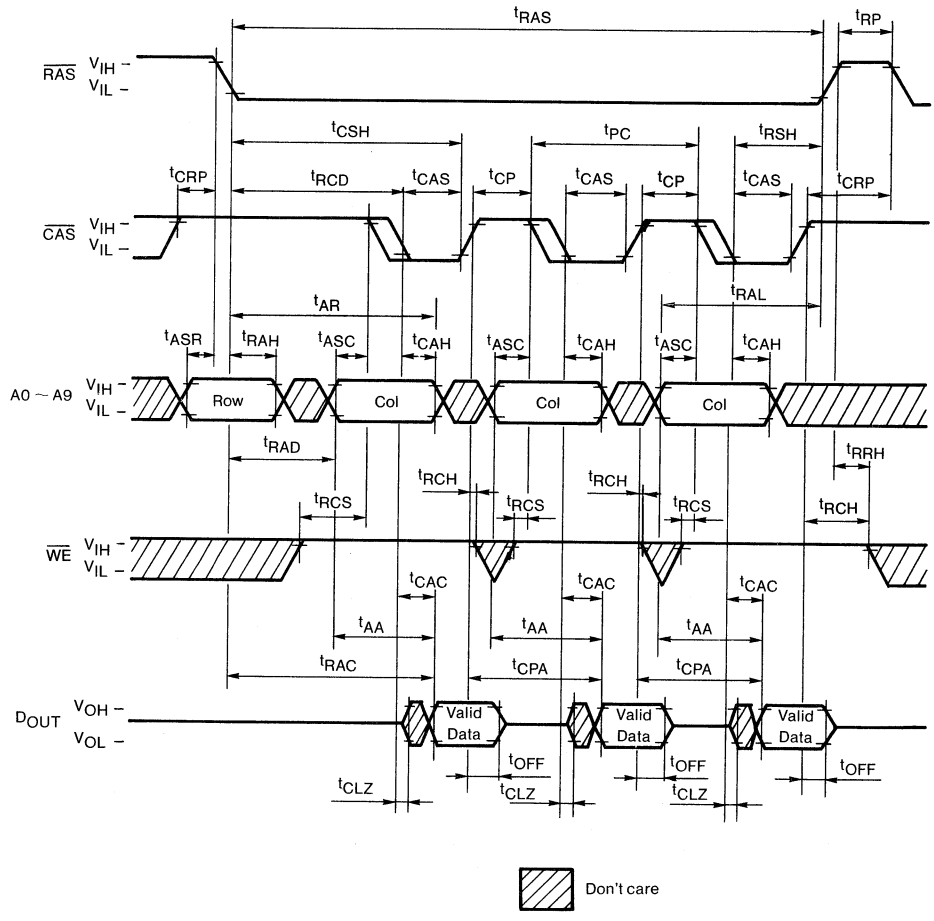
WRITE CYCLE (EARLY WRITE)



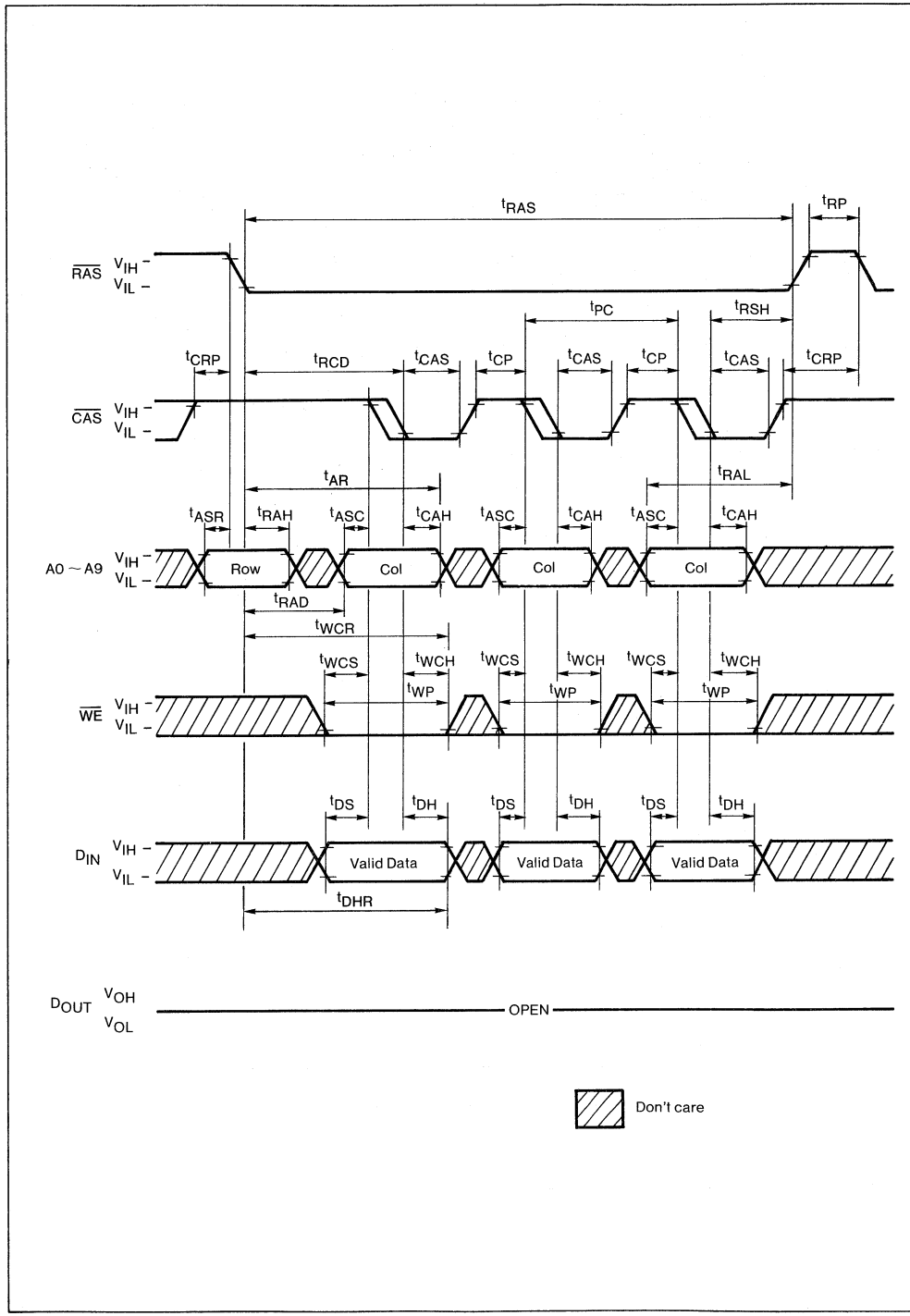
READ/WRITE CYCLE



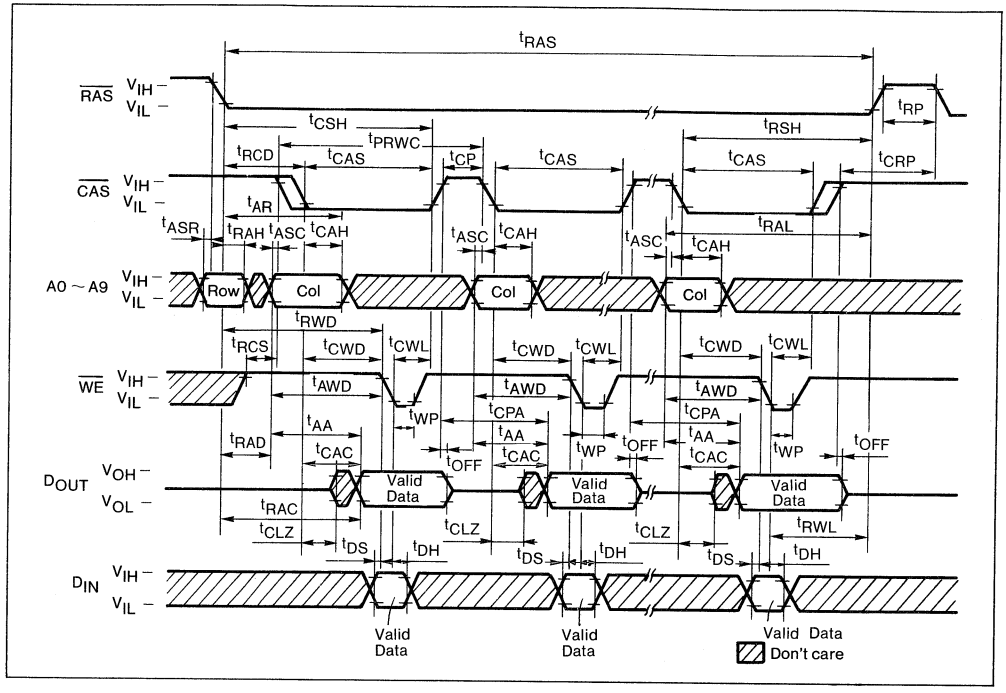
FAST PAGE MODE READ CYCLE



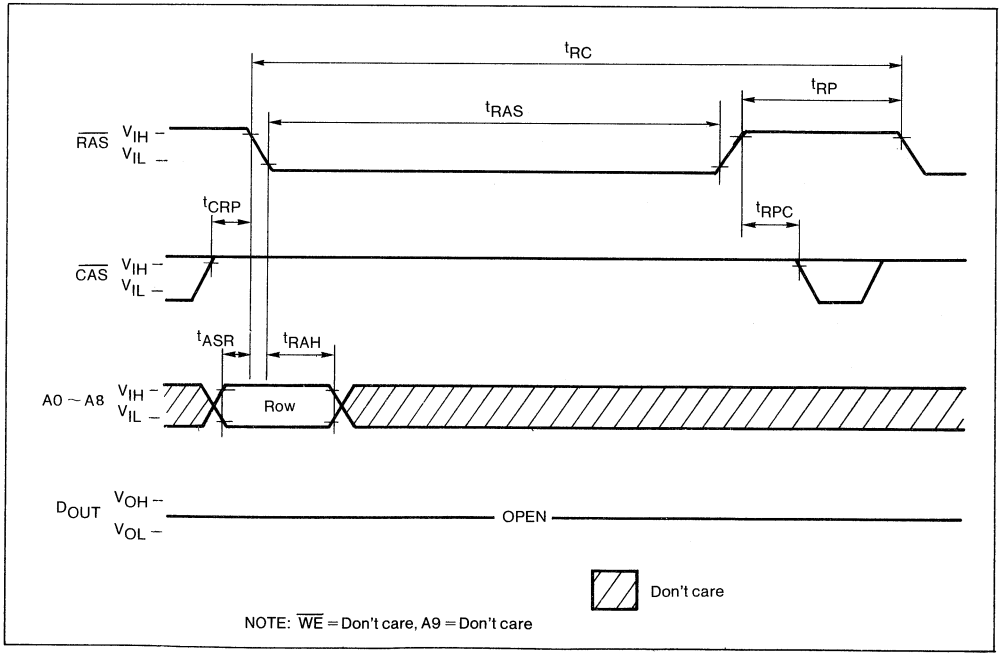
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



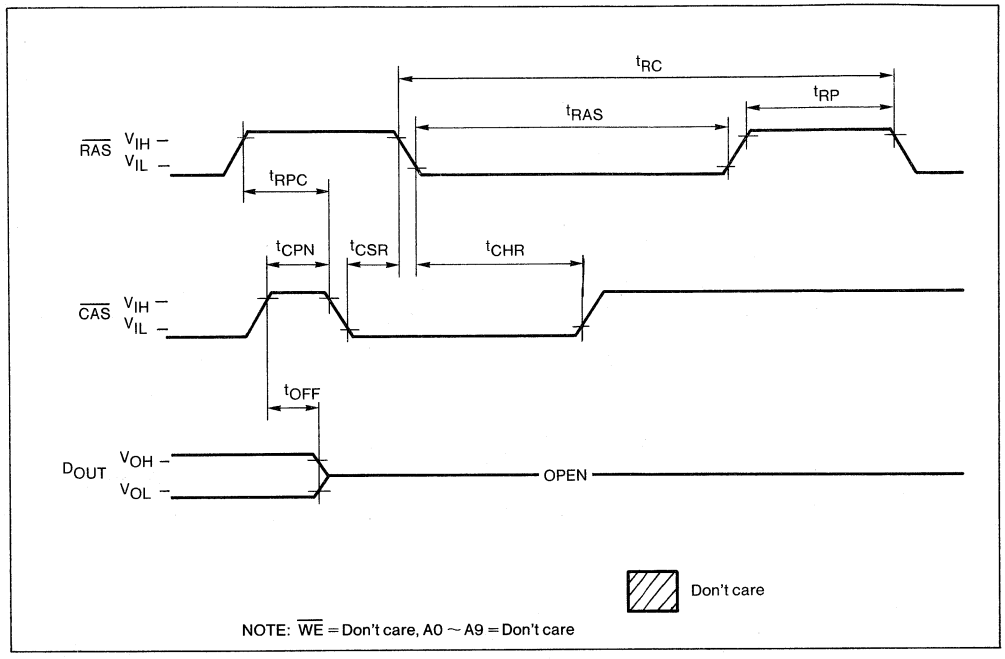
FAST PAGE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

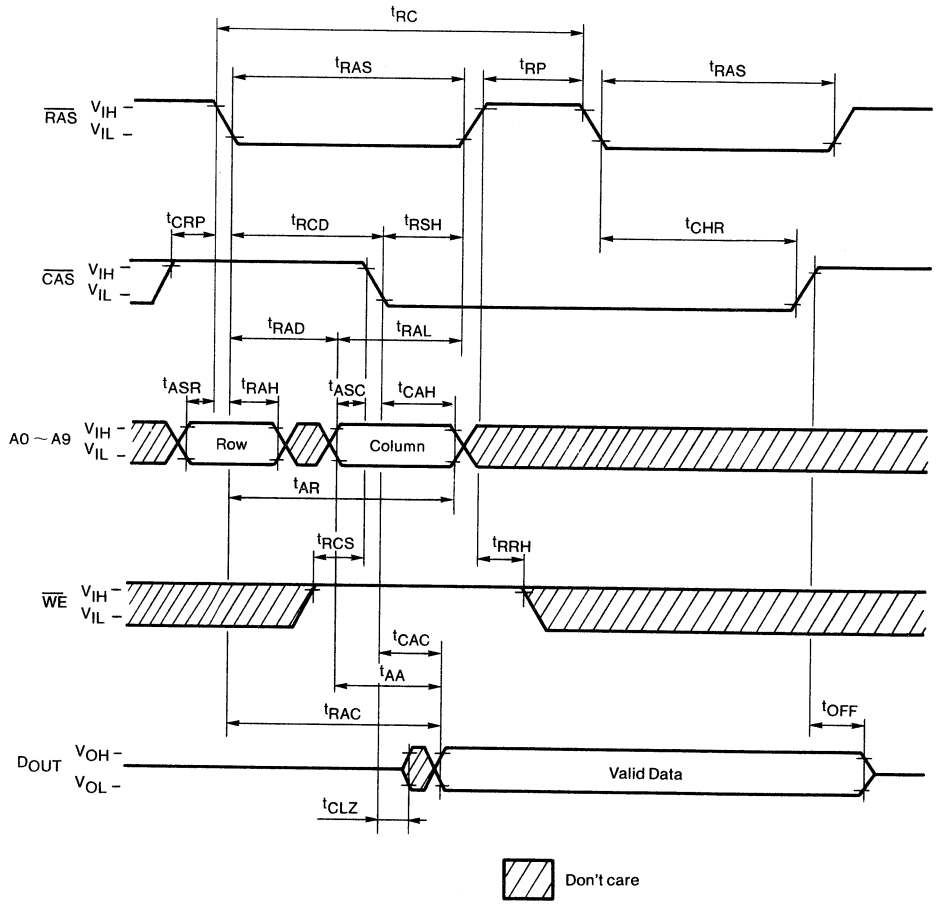


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

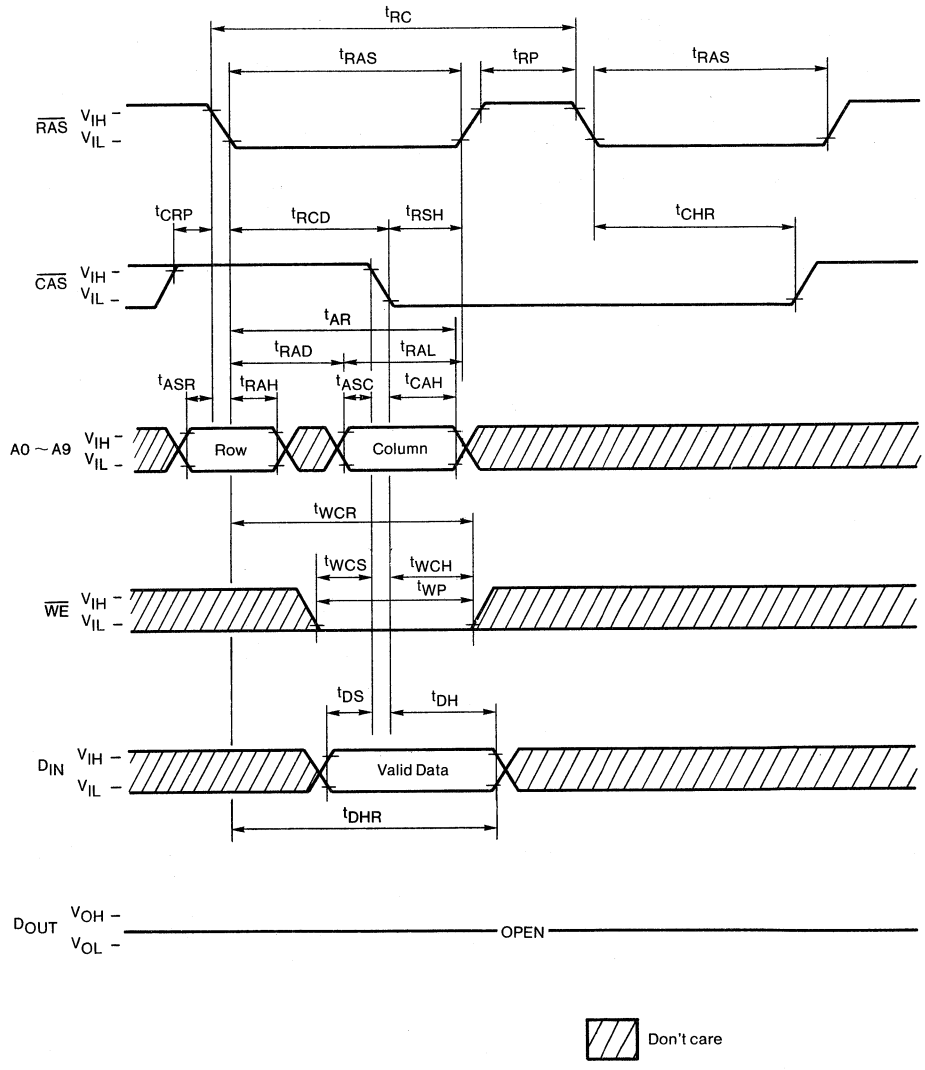


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

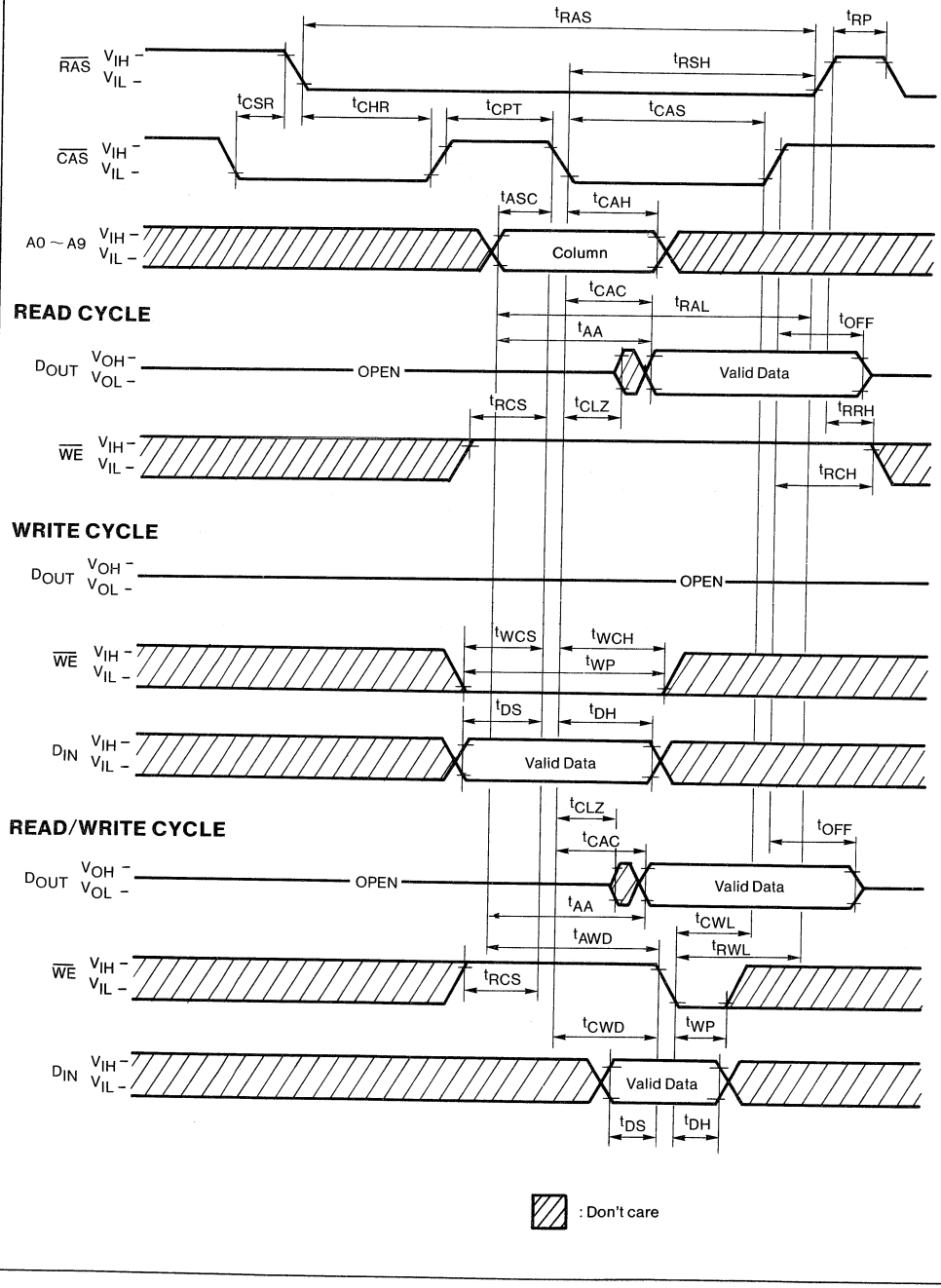
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Preliminary

OKI semiconductor

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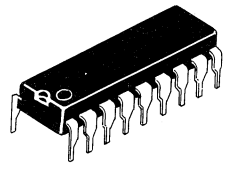
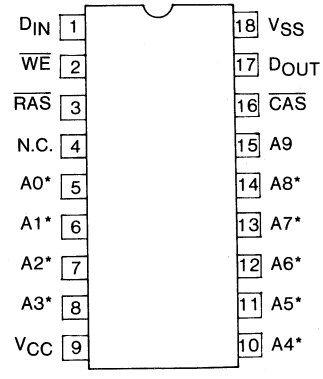
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511001-10RS	100 ns	190 ns	385 mW	5.5 mW
MSM511001-12RS	120 ns	220 ns	330 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Nibble mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



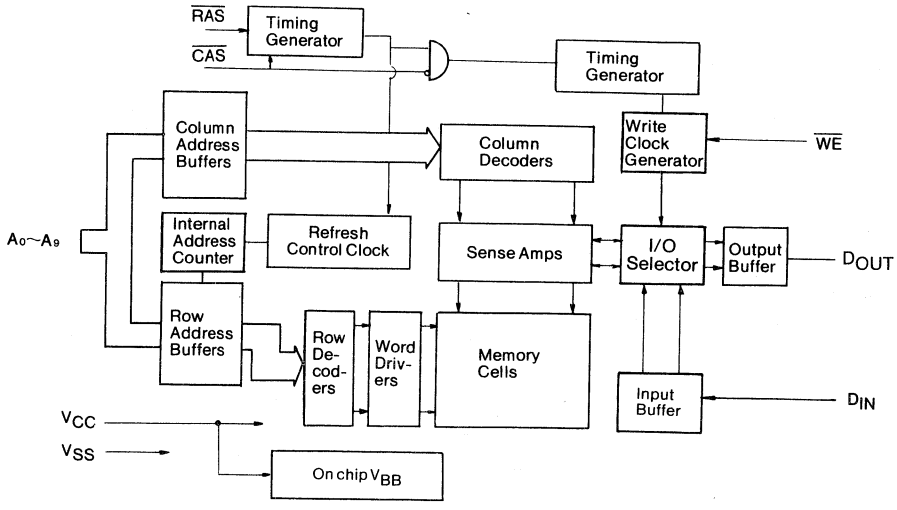
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 511001-10		MSM 511001-12		Unit	Note
				MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA		2.4	Vcc	2.4	Vcc	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V		−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V		−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min		–	70	–	60	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ D_{OUT} = Hz	TTL	–	2	–	2	mA	
			MOS	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ t_{RC} = min		–	70	–	60	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		–	70	–	60	mA	
Average power supply current* (Nibble mode)	I_{CC8}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling t_{NC} = min		–	50	–	45	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Note 1, 2, 3

Parameter	Symbol	MSM511001-10		MSM511001-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	190	–	220	–	ns	
Read/write cycle time	t_{RWC}	220	–	255	–	ns	
Nibble mode cycle time	t_{NC}	50	–	65	–	ns	
Nibble mode read/write cycle time	t_{NRMW}	75	–	90	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	35	–	45	ns	4, 5
Access time from column address	t_{AA}	–	50	–	60	ns	4, 6
Nibble mode access time	t_{NCAC}	–	20	–	30	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	25	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	35	–	45	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	35	10000	45	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	65	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	25	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	–	90	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50	–	60	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	

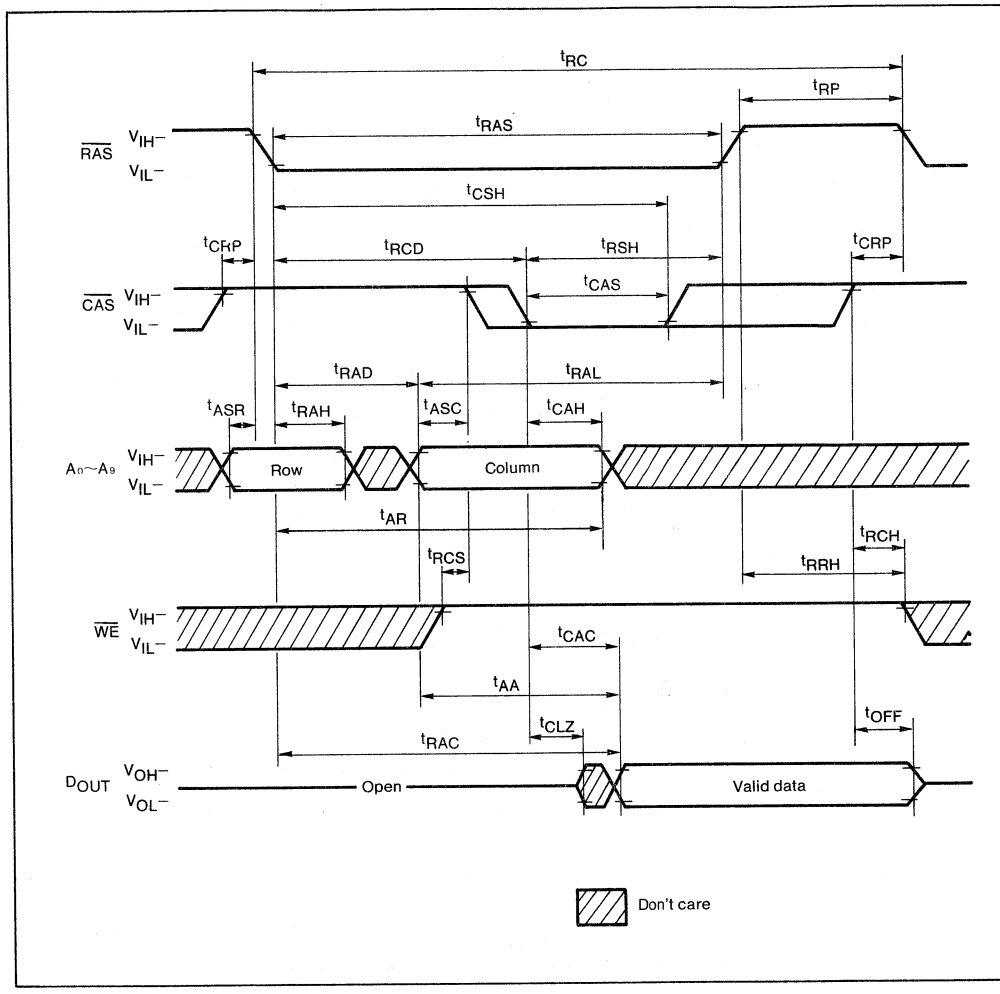
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM511001-10		MSM511001-12		Unit	Note
		MIN	MAX	MIN	MAX		
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	20	–	25	–	ns	
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	30	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	35	–	45	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100	–	120	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	60	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	15	–	20	–	ns	
Nibble mode pulse width	t_{NCAS}	20	–	30	–	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20	–	25	–	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20	–	25	–	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay	t_{NCWD}	20	–	25	–	ns	
Nibble mode write command to $\overline{RAS}$ lead time	t_{NRWL}	25	–	30	–	ns	
Nibble mode write command to $\overline{CAS}$ lead time	t_{NCWL}	20	–	25	–	ns	

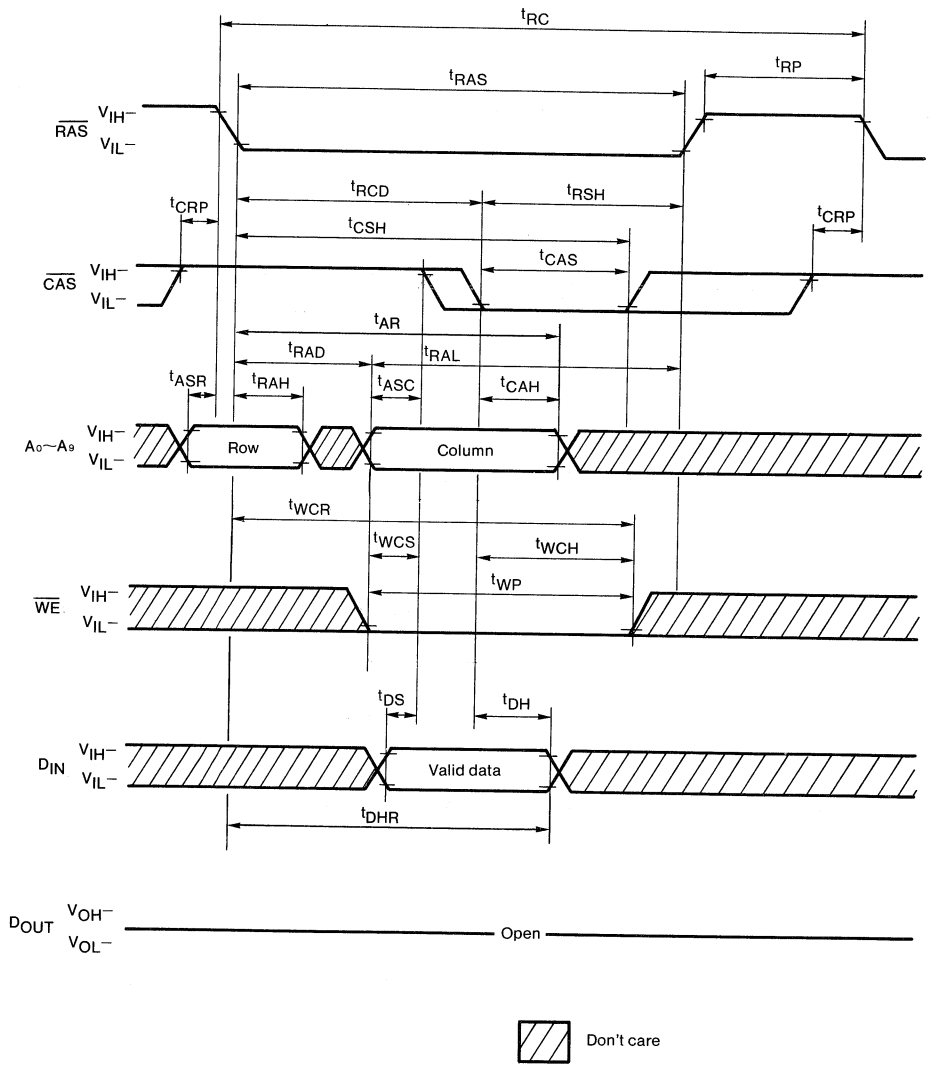
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

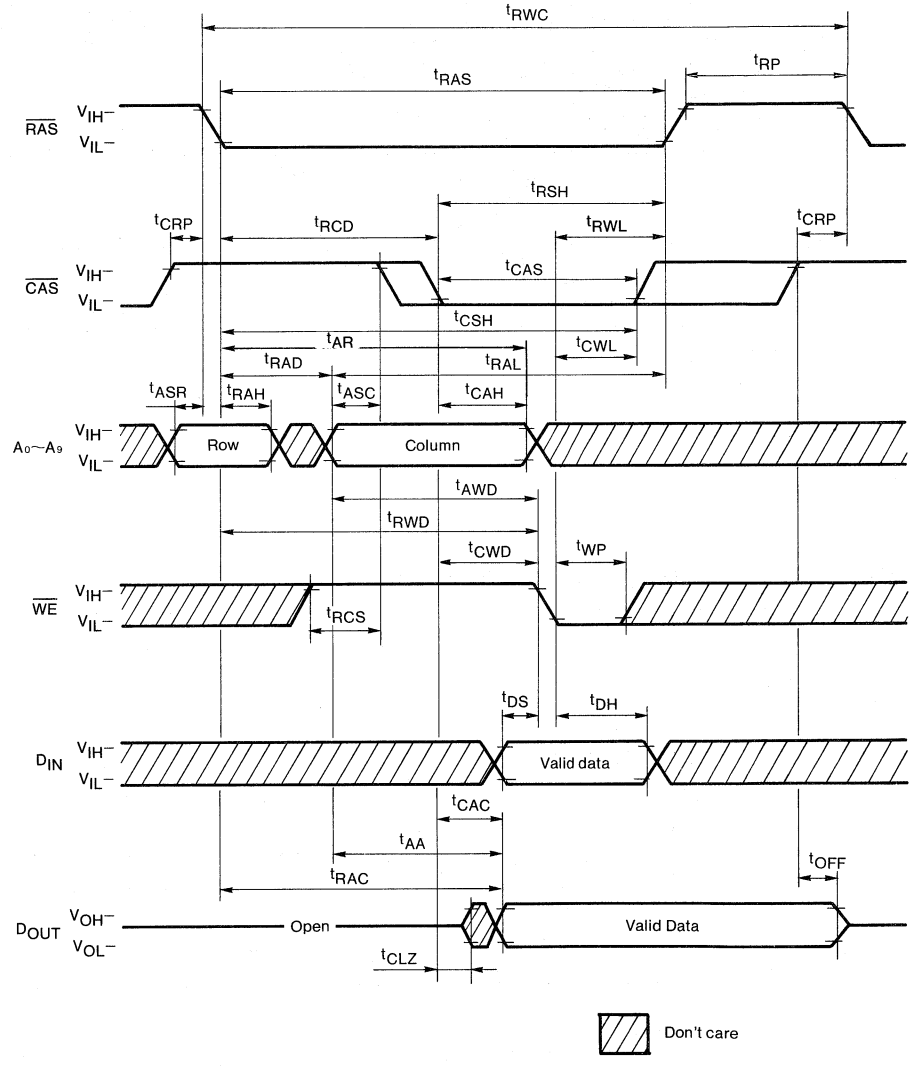
READ CYCLE


tRC
tRP
tRAS
RAS VIH− VIL−
tCSH
tCRP
tRCD
tRSH
tCRP
CAS VIH− VIL−
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9 VIH− VIL−
Row
Column
tAR
tRCH
tRCS
tRRH
WE VIH− VIL−
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT VOH− VOL−
Open
Valid data
Don't care

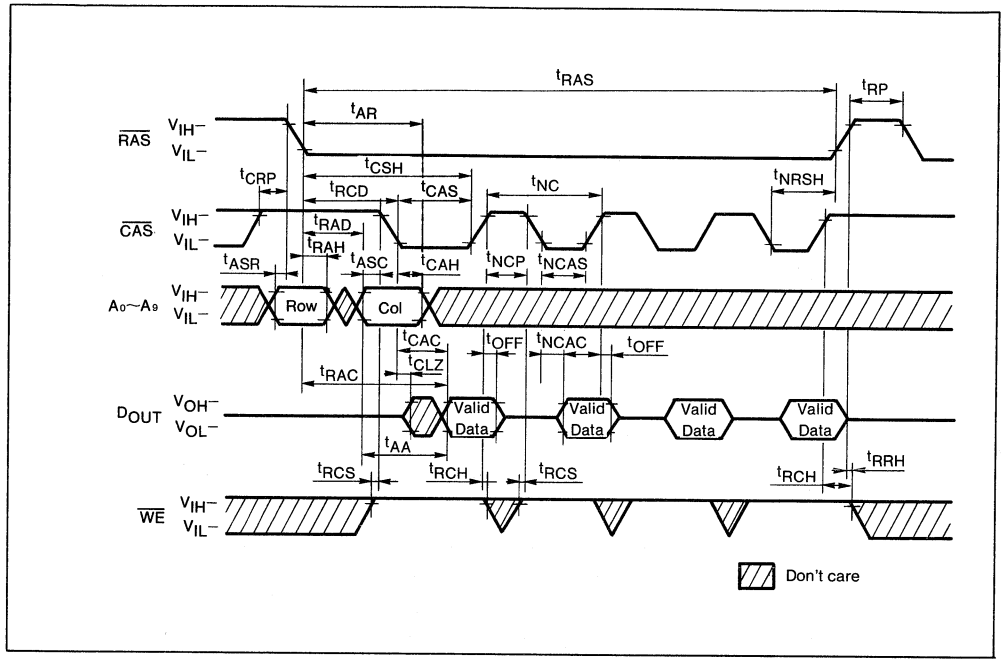
WRITE CYCLE (EARLY WRITE)



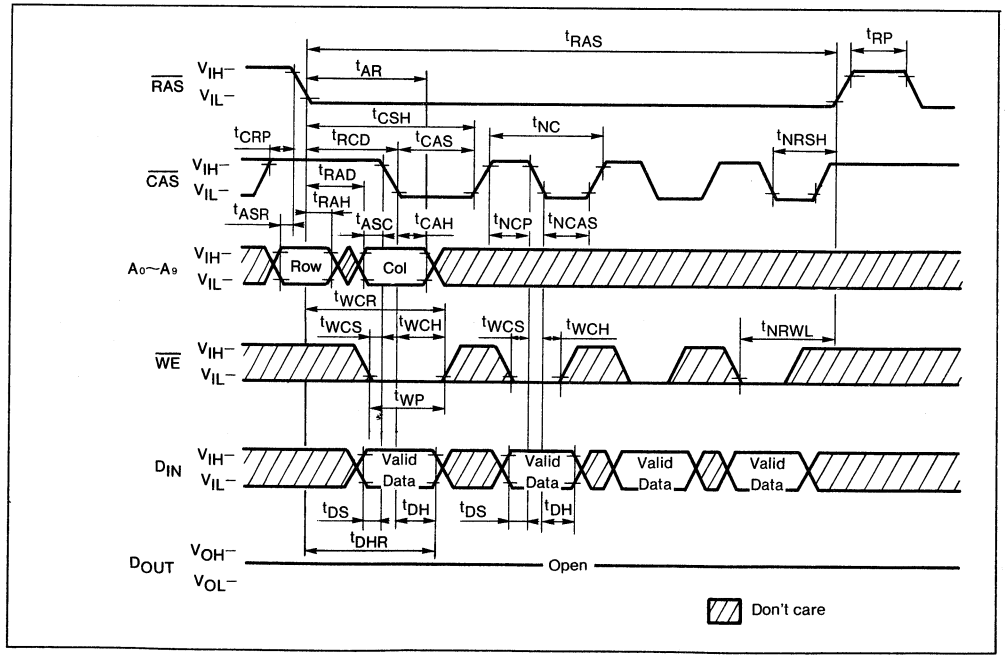
READ/WRITE CYCLE



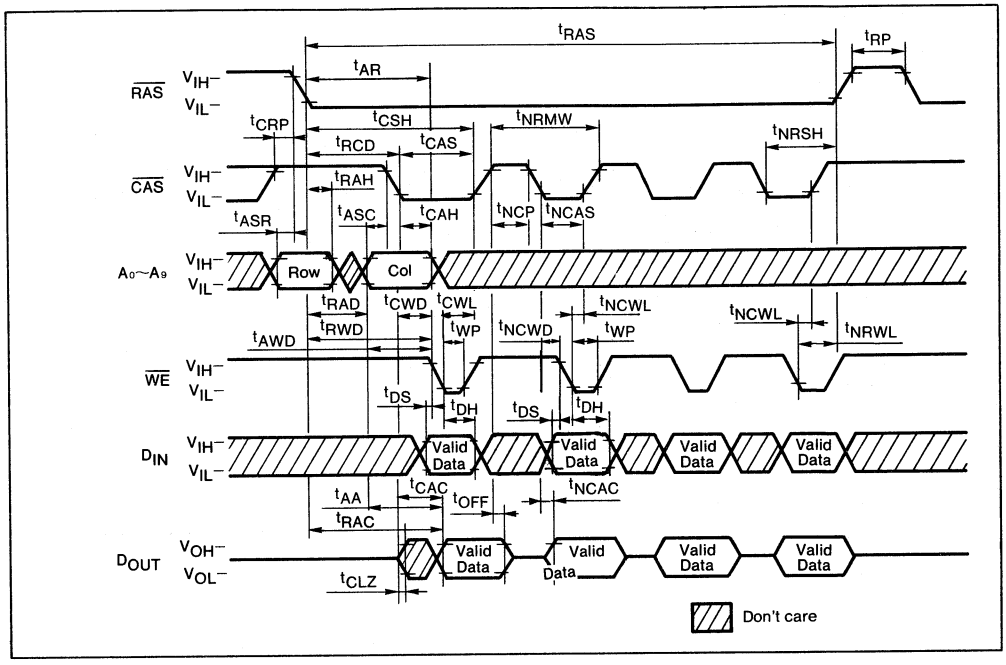
NIBBLE MODE READ CYCLE



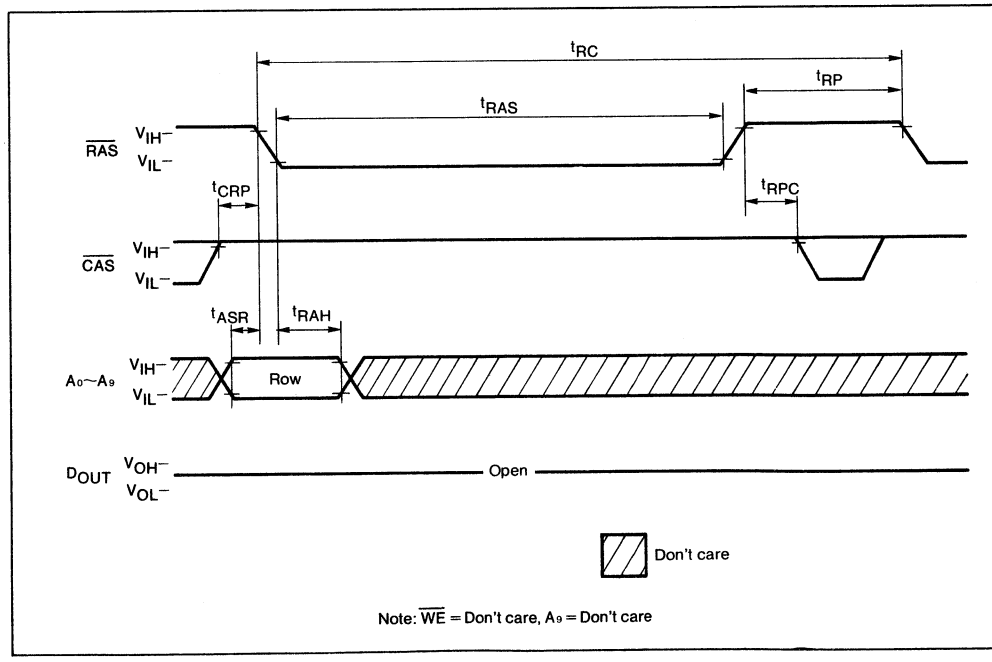
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



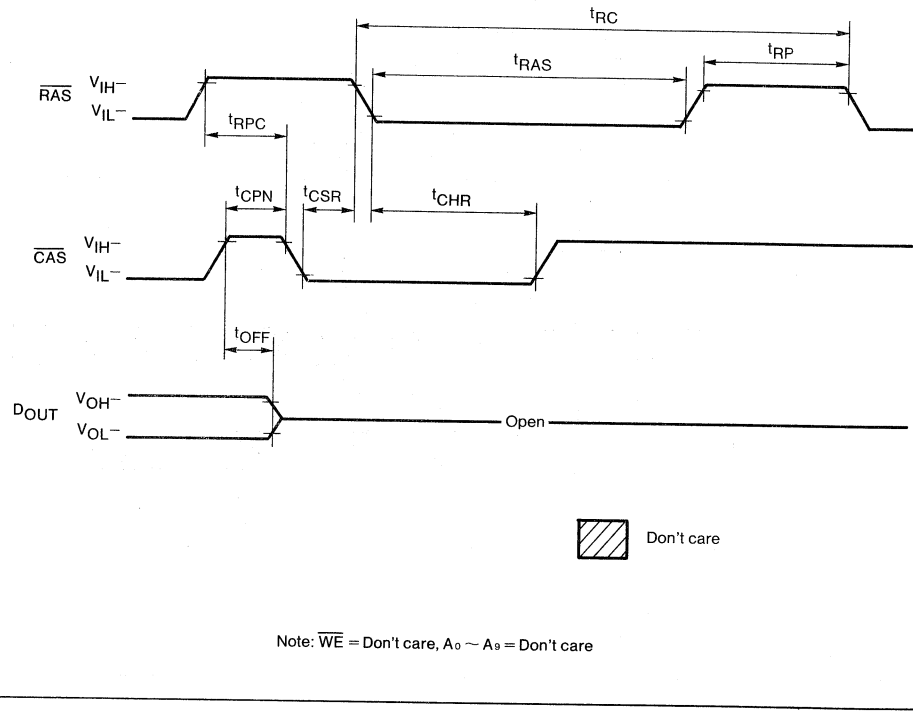
NIBBLE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

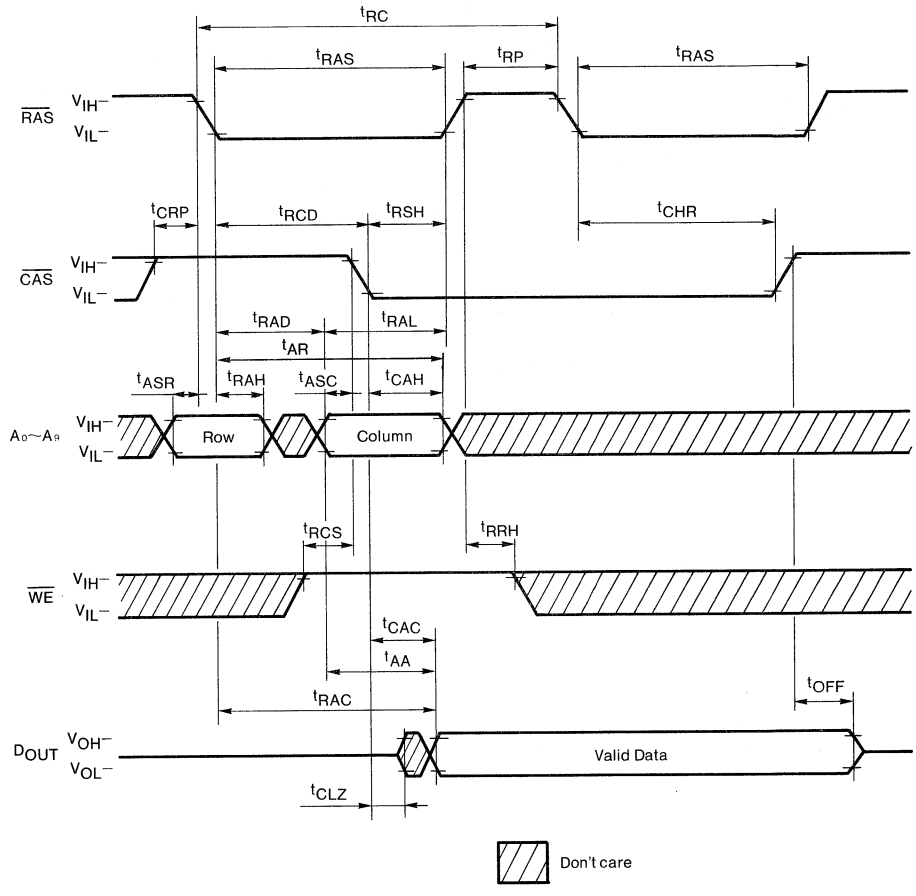


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

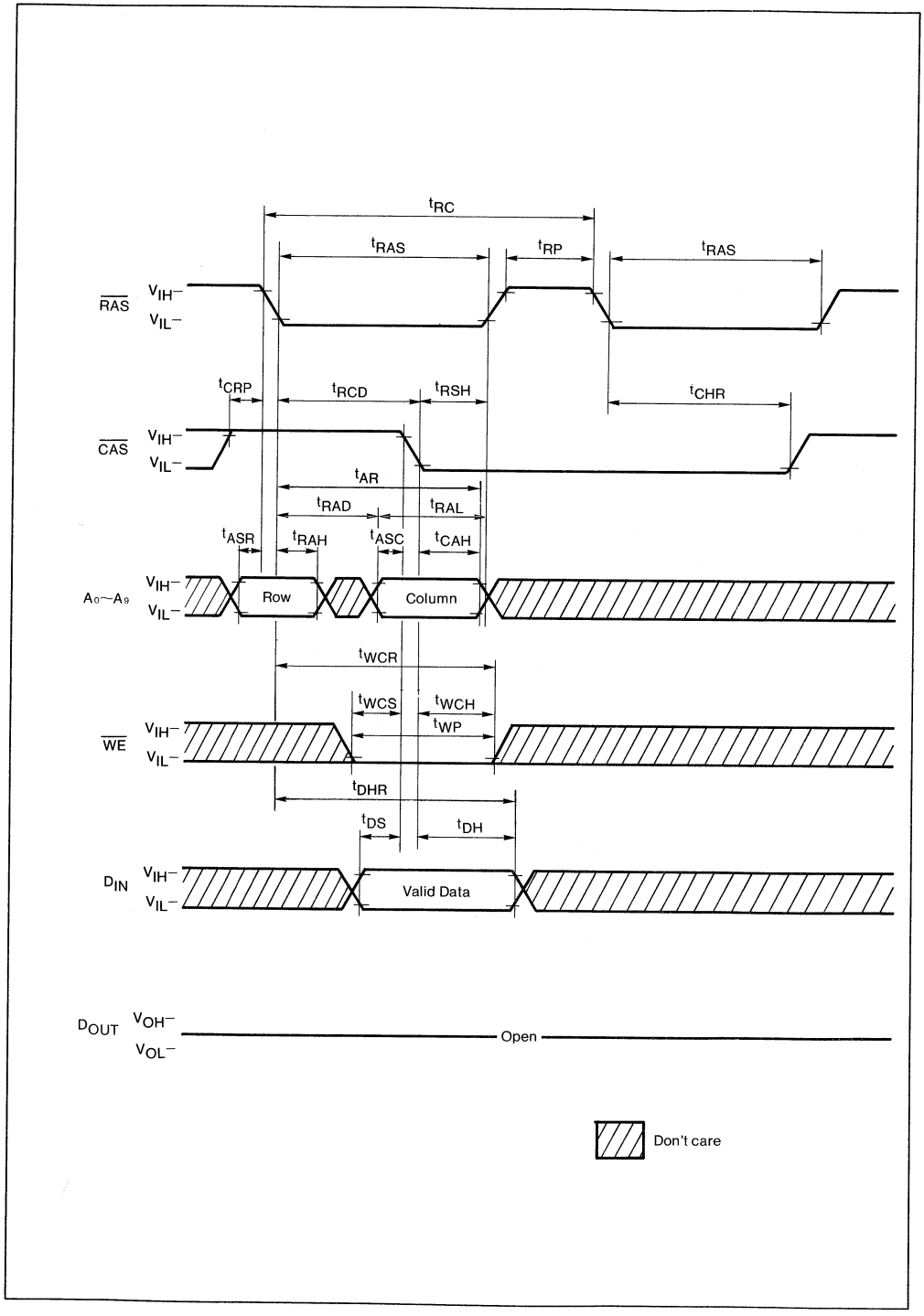


Note: $\overline{WE}$ = Don't care, $A_0 \sim A_9$ = Don't care

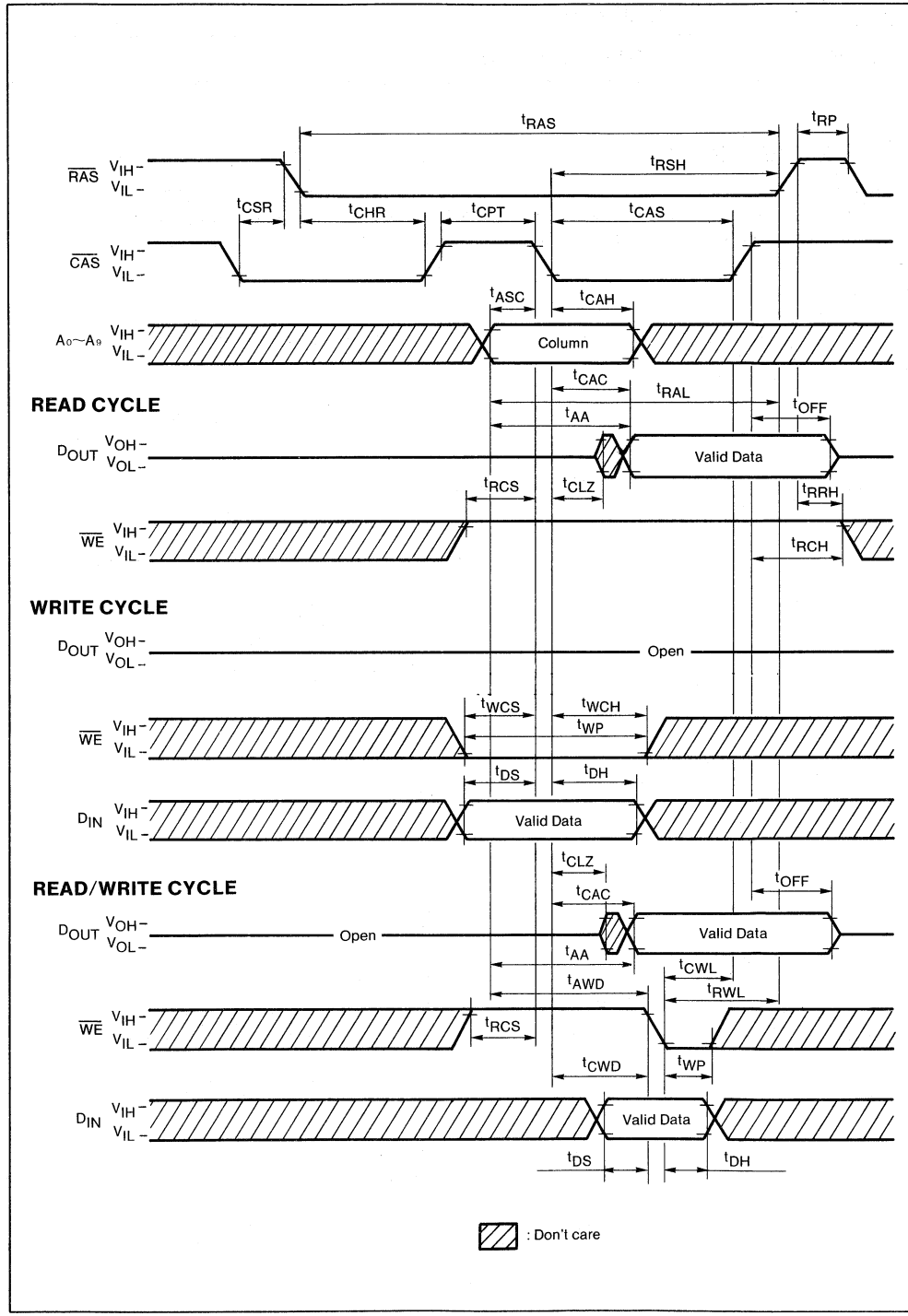
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Preliminary

OKI semiconductor

MSM511002RS

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

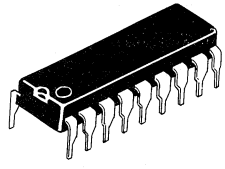
The MSM511002RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511002RS is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

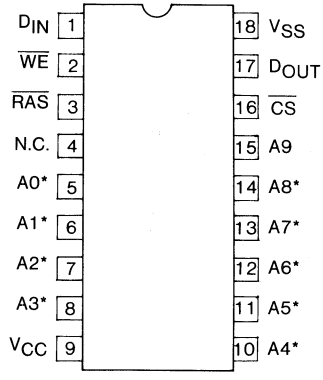
- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511002-10RS	100 ns	190 ns	385 mW	5.5 mW
MSM511002-12RS	120 ns	220 ns	330 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Static column mode, read/write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit



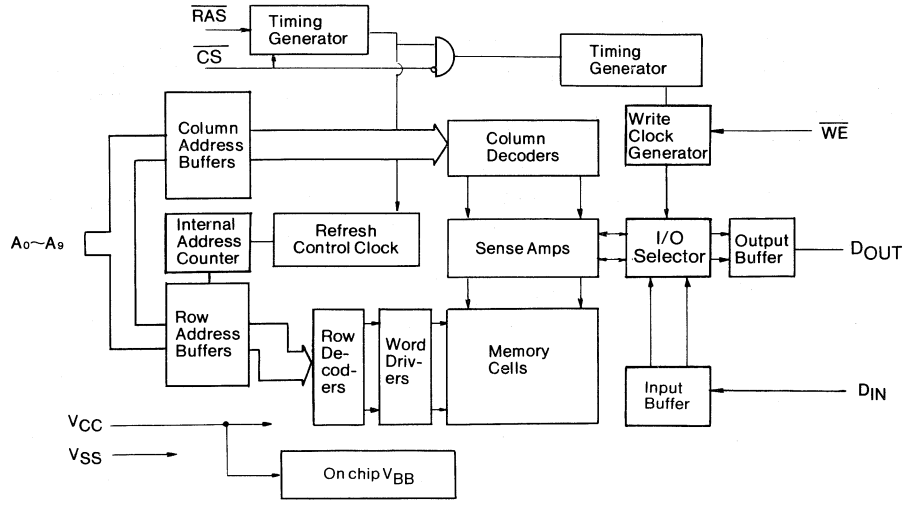
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 511002-10		MSM 511002-12		Unit	Note
				MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA		2.4	Vcc	2.4	Vcc	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V		−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V		−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min		–	70	–	60	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz	TTL	–	2	–	2	mA	
			MOS	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, t_{RC} = min		–	70	–	60	mA	
Average power supply current* ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$		–	70	–	60	mA	
Average power supply current* (Static column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ cycling, t_{SC} = min		–	50	–	45	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM511002-10		MSM511002-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	190	–	220	–	ns	
Read/write cycle time	t_{RWC}	220	–	255	–	ns	
Static column mode cycle time	t_{SC}	55	–	65	–	ns	
Static column mode read/write cycle time	t_{SRWC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5, 6
Access time from $\overline{CS}$	t_{CAC}	–	35	–	45	ns	4, 5
Access time from column address	t_{AA}	–	50	–	60	ns	4, 6, 7
Access time from last write	t_{ALW}	–	95	–	115	ns	4, 7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	30	–	35	ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	35	–	45	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	15	–	ns	
$\overline{CS}$ pulse width	t_{CS}	35	10000	45	10000	ns	
$\overline{CS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	65	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	6
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	25	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM511002-10		MSM511002-12		Unit	Note
		MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ lead time	t_{RAL}	50	–	60	–	ns	
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	75	–	90	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	115	–	140	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	15	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	95	–	115	–	ns	
Last write to column address delay	t_{LWAD}	25	45	30	55	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	8
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write invalid time	t_{WI}	10	–	15	–	ns	
Write command hold time (Dout disable)	t_{WH}	0	–	0	–	ns	8
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	30	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	25	–	30	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	35	–	45	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100	–	120	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	60	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	9
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	

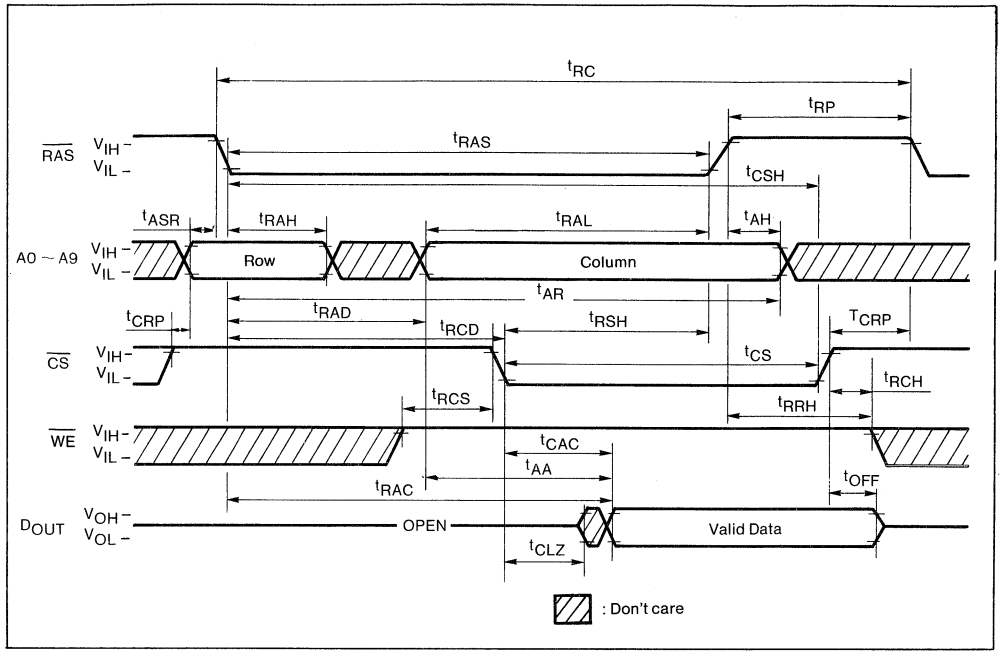
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM511002-10		MSM511002-12		Unit	Note
		MIN	MAX	MIN	MAX		
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	
$\overline{CS}$ precharge time	t_{CPN}	15	–	20	–	ns	

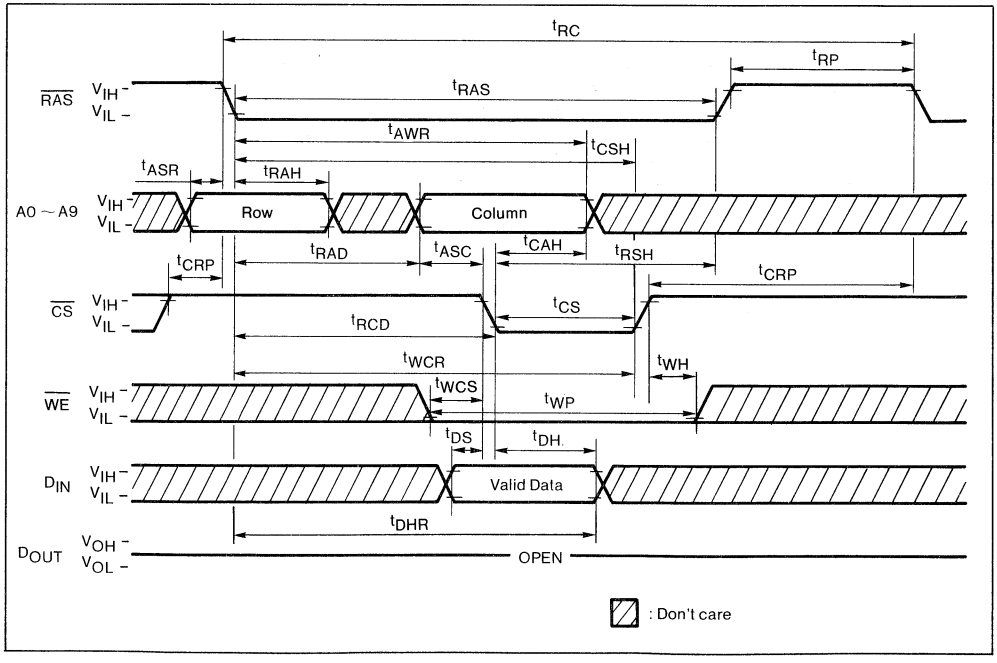
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
8. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

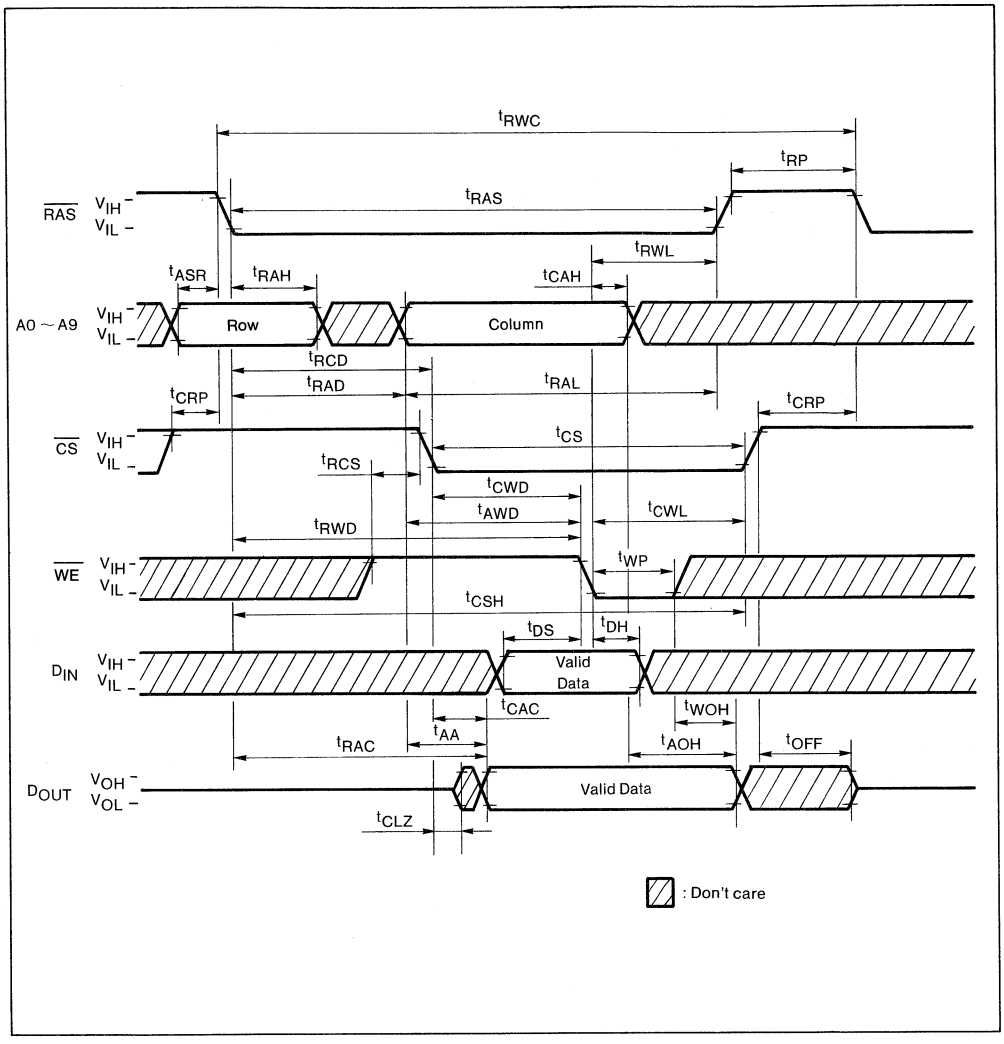
READ CYCLE



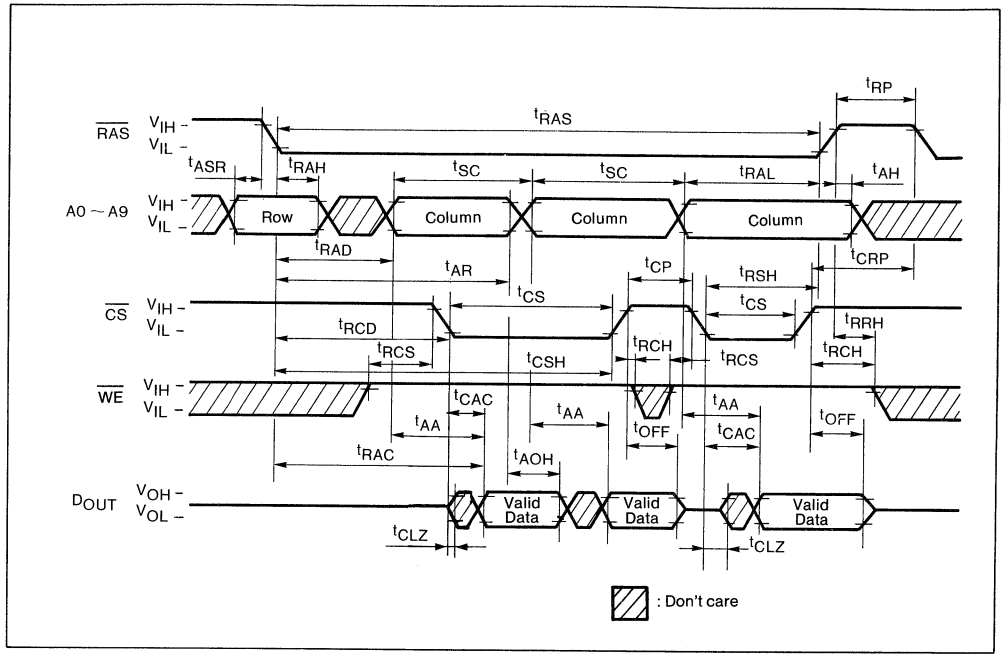
WRITE CYCLE (EARLY WRITE)



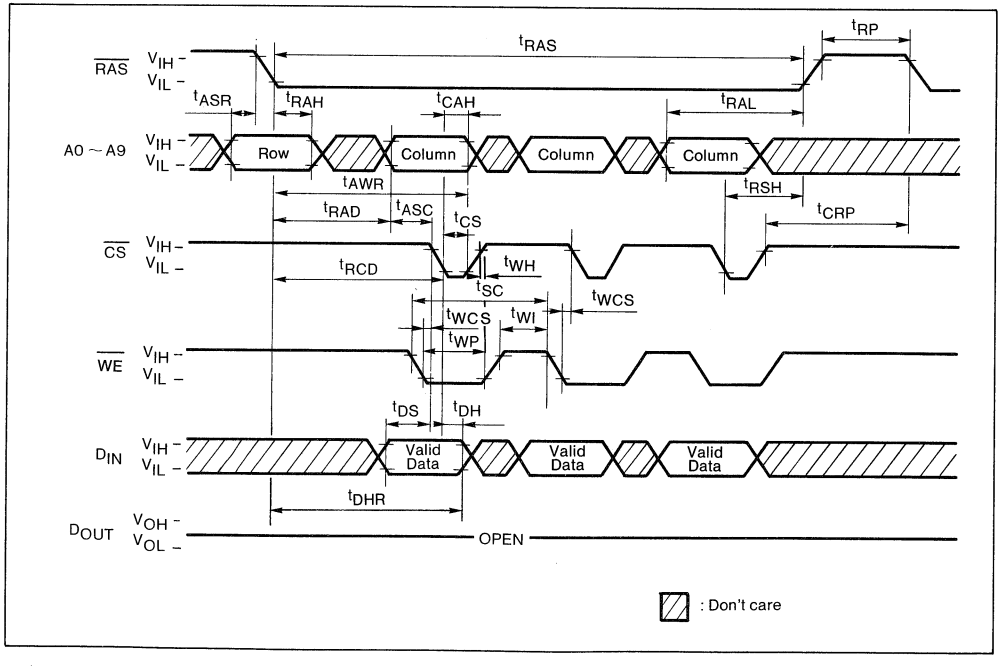
READ/WRITE CYCLE



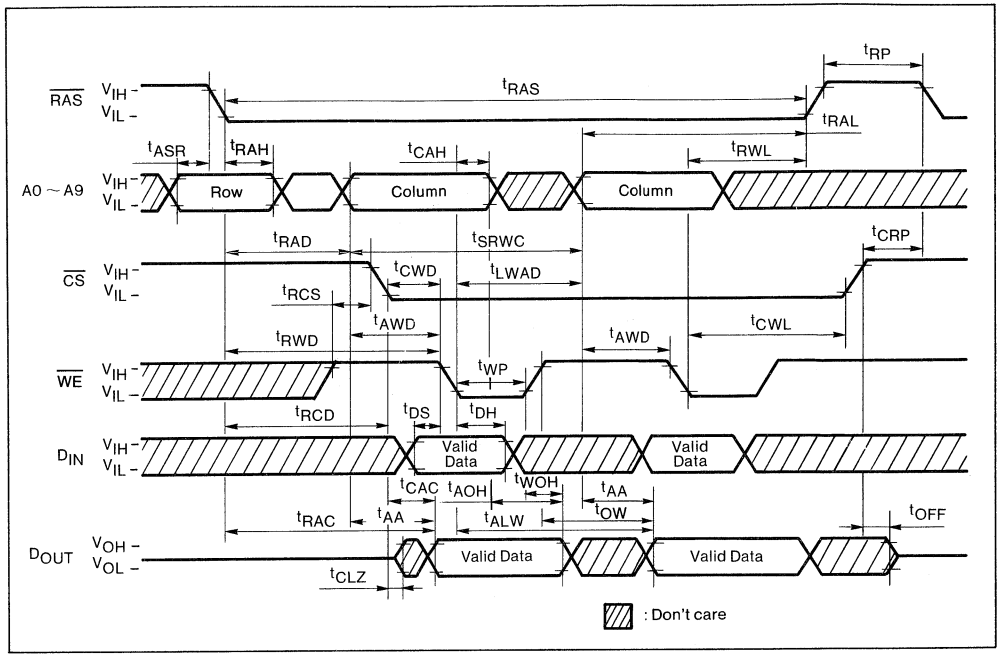
STATIC COLUMN MODE READ CYCLE



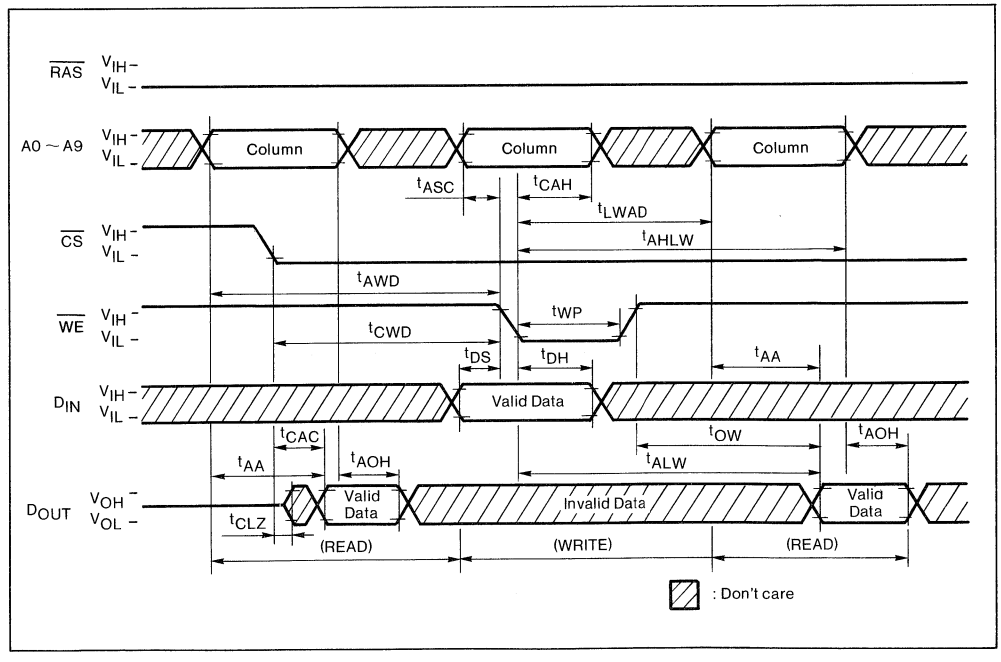
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



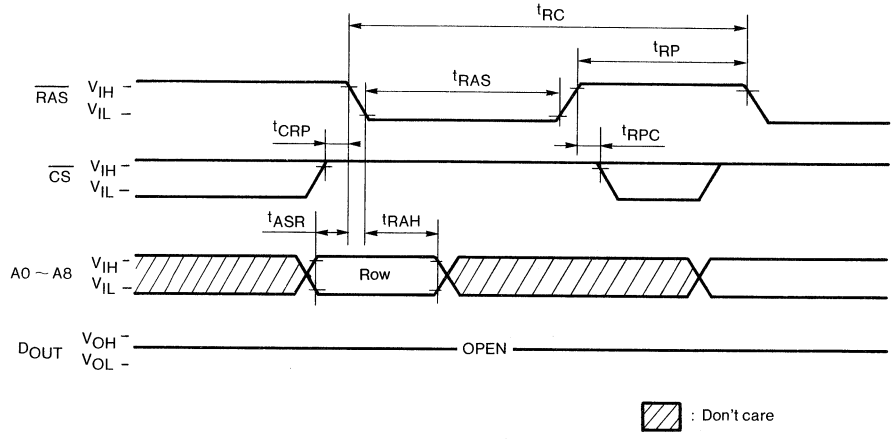
STATIC COLUMN MODE READ/WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

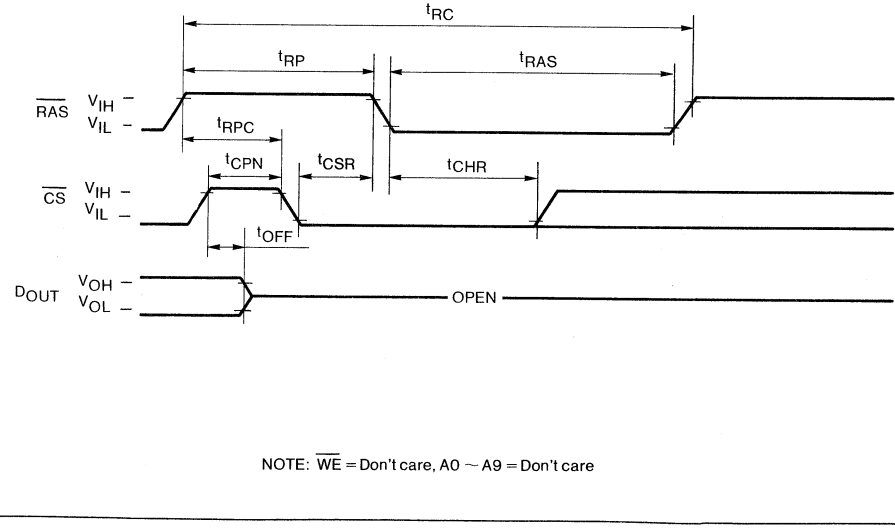


$\overline{RAS}$ ONLY REFRESH CYCLE



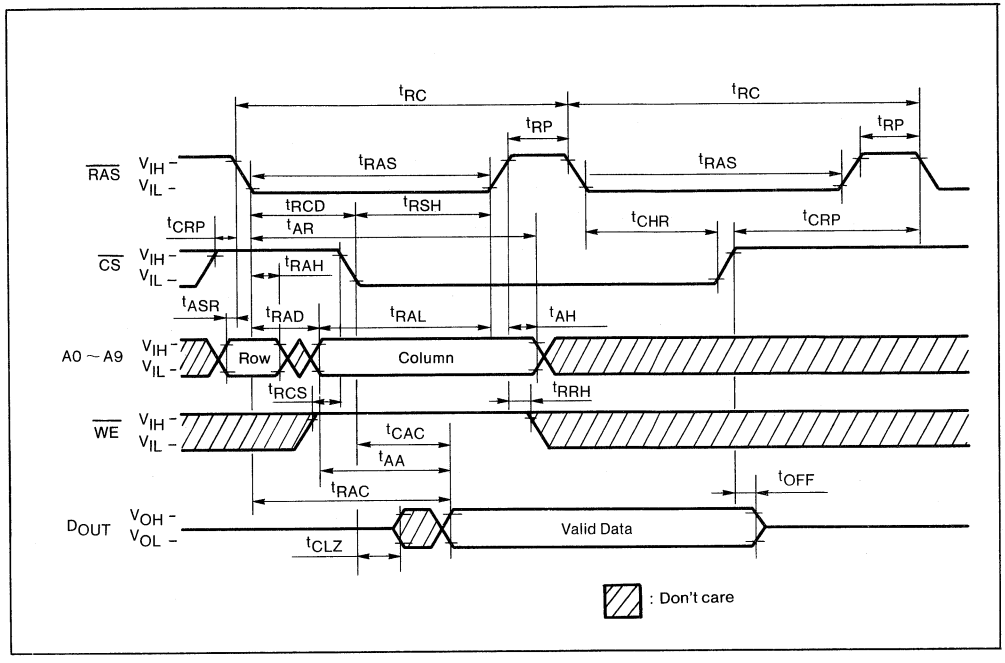
NOTE: $\overline{WE}$ = Don't care, A9 = Don't care

$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

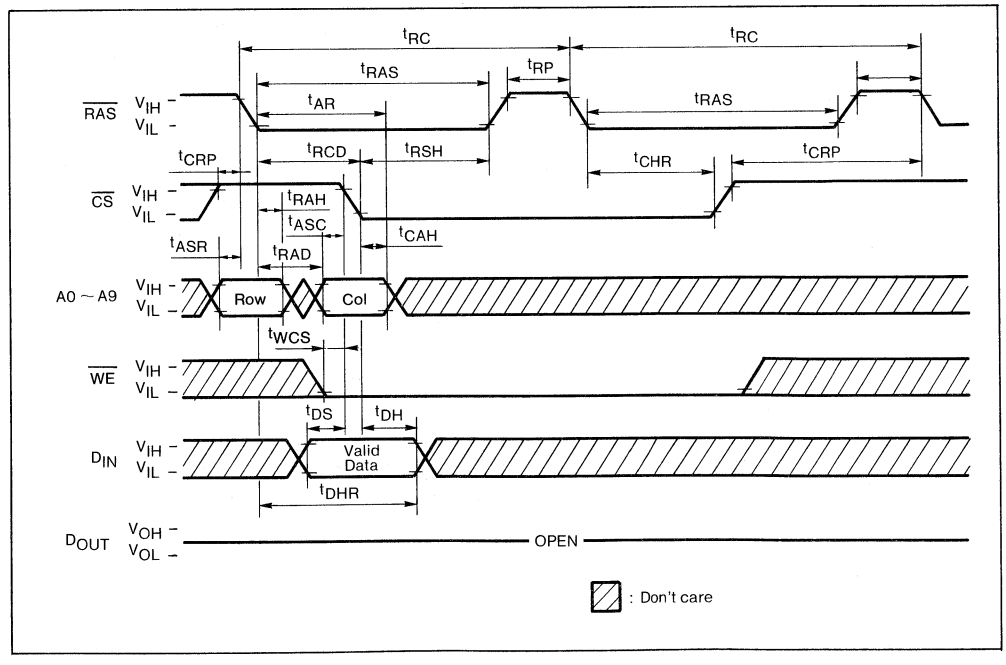


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

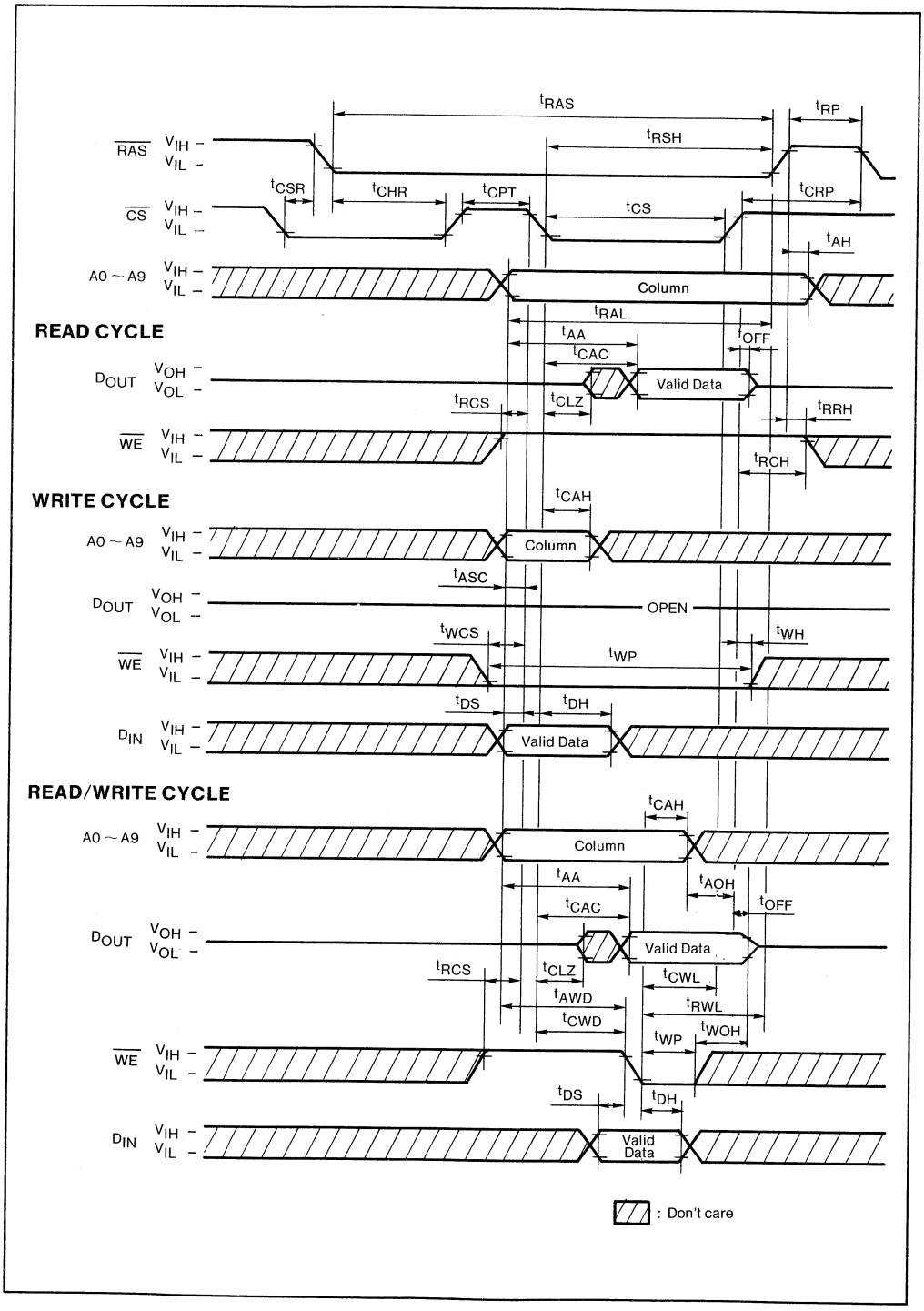
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



Preliminary

OKI semiconductor

MSM514256RS

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

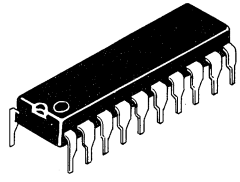
The MSM514256RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514256RS is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

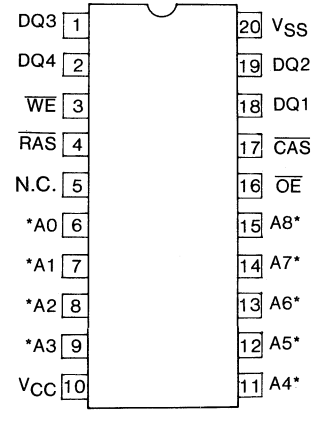
- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514256-10RS	100 ns	190 ns	413 mW	5.5 mW
MSM514256-12RS	120 ns	220 ns	358 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



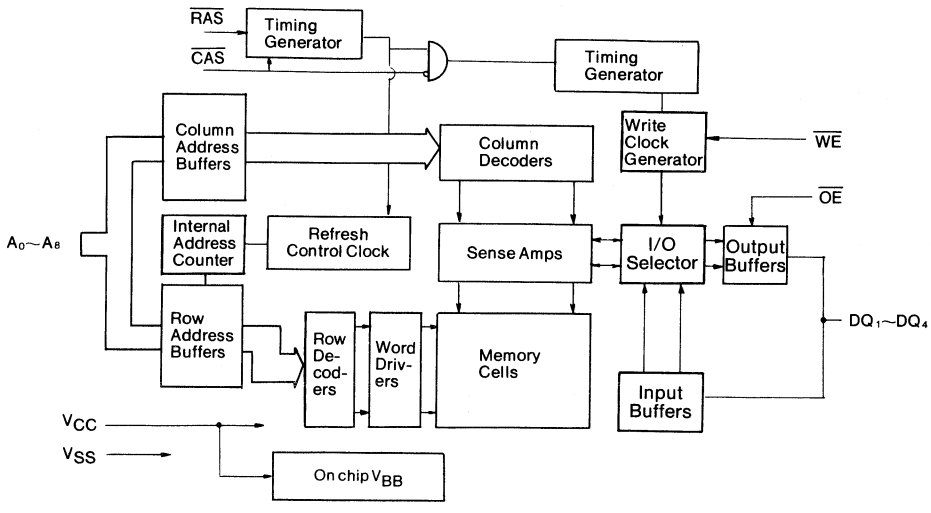
PIN CONFIGURATION (TOP VIEW)



*Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514256-10		MSM 514256-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = HZ — TTL	–	2	–	2	mA	
		MOS	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	–	75	–	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	75	–	65	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min	–	55	–	50	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Note 1, 2, 3

Parameter	Symbol	MSM514256-10		MSM514256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	190	–	220	–	ns	
Read/write cycle time	t_{RWC}	255	–	295	–	ns	
Fast page mode cycle time	t_{PC}	55	–	70	–	ns	
Fast page mode read/write cycle time	t_{PRMW}	120	–	140	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	**4, 5, 6**
Access time from $\overline{CAS}$	t_{CAC}	–	35	–	45	ns	4, 5
Access time from column address	t_{AA}		50		60	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	65	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	25	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	35	–	45	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	15	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	35	10000	45	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	65	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
$\overline{Row}$ address set-up time	t_{ASR}	0	–	0	–	ns	
$\overline{Row}$ address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	–	90	–	ns	
Column address hold time	t_{CAH}	20	–	25	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50	–	60	–	ns	

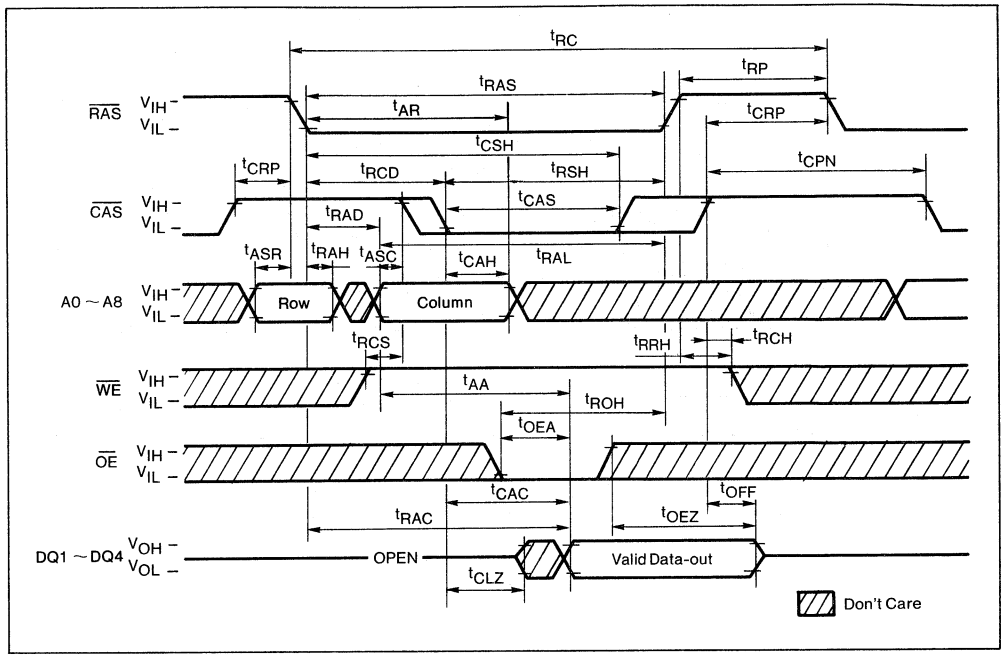
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514256-10		MSM514256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	20	–	25	–	ns	
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	30	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	–	30	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	70	–	85	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	135	–	160	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	85		100		ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	15	–	20	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	25	–	30	ns	
$\overline{OE}$ delay time	t_{OED}	25	–	30	–	ns	
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	25	0	30	ns	
$\overline{OE}$ command hold time	t_{OEH}	25	–	30	–	ns	

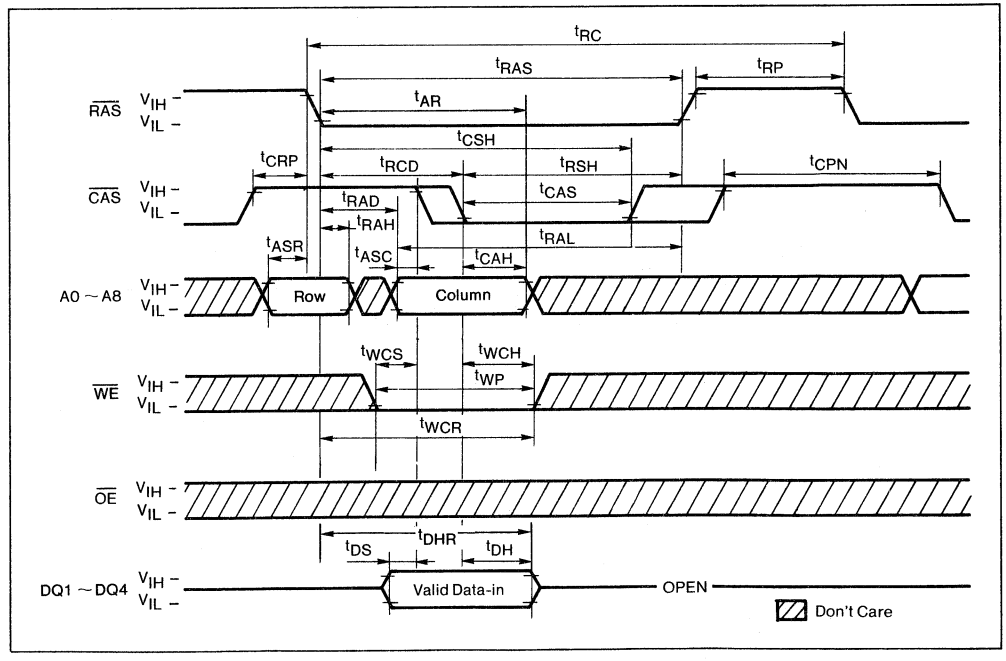
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

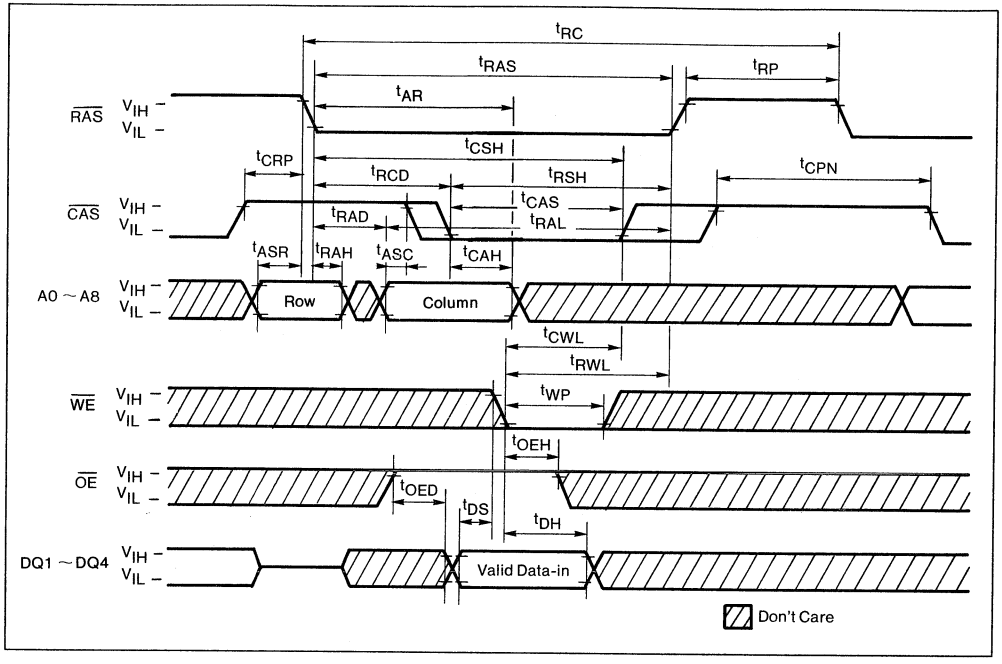
READ CYCLE



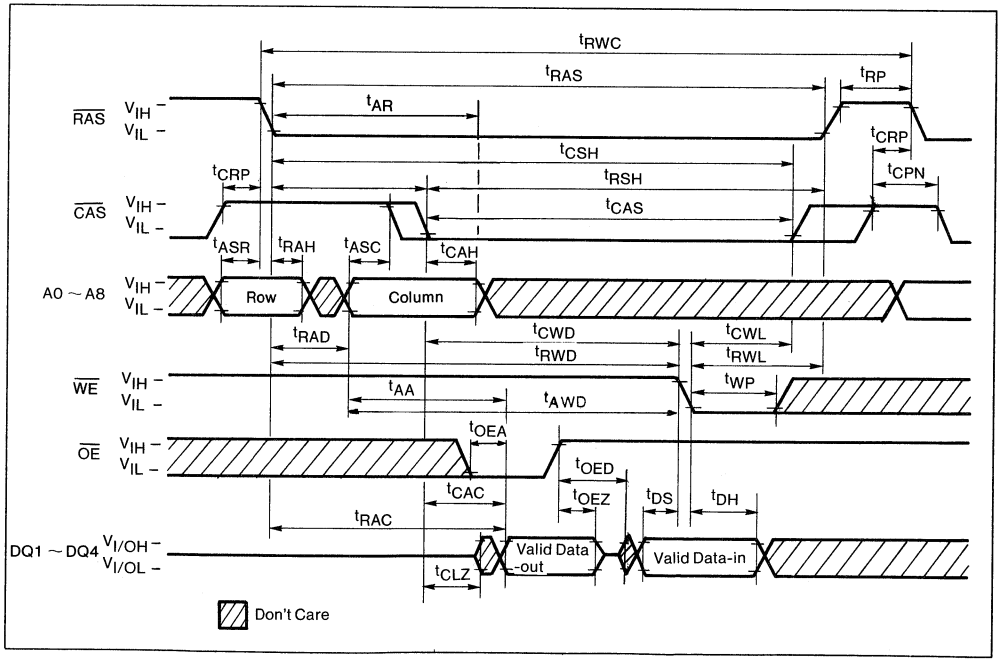
WRITE CYCLE (EARLY WRITE)



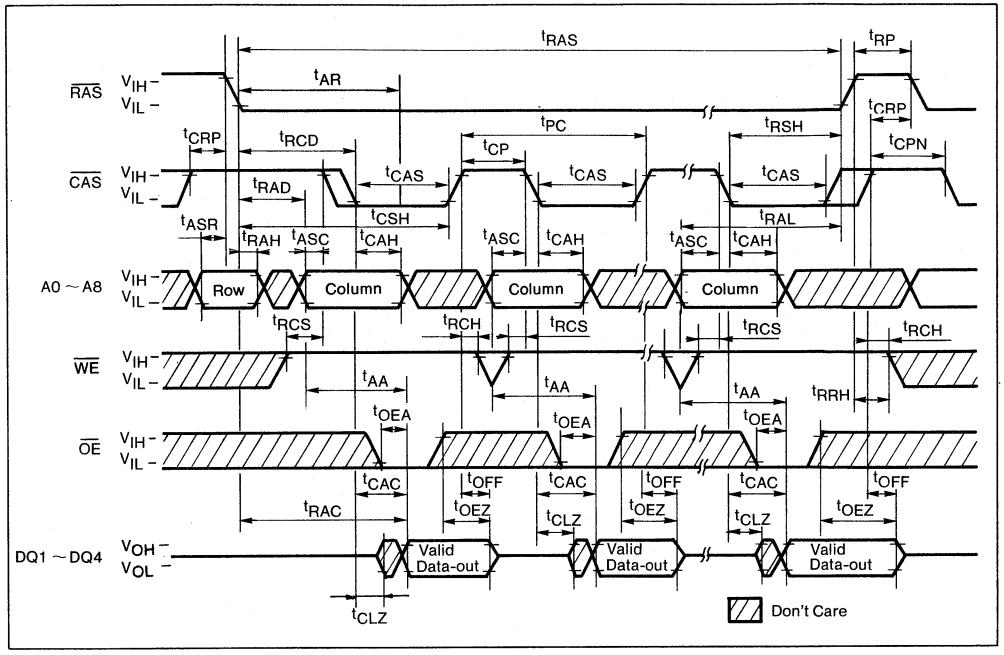
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



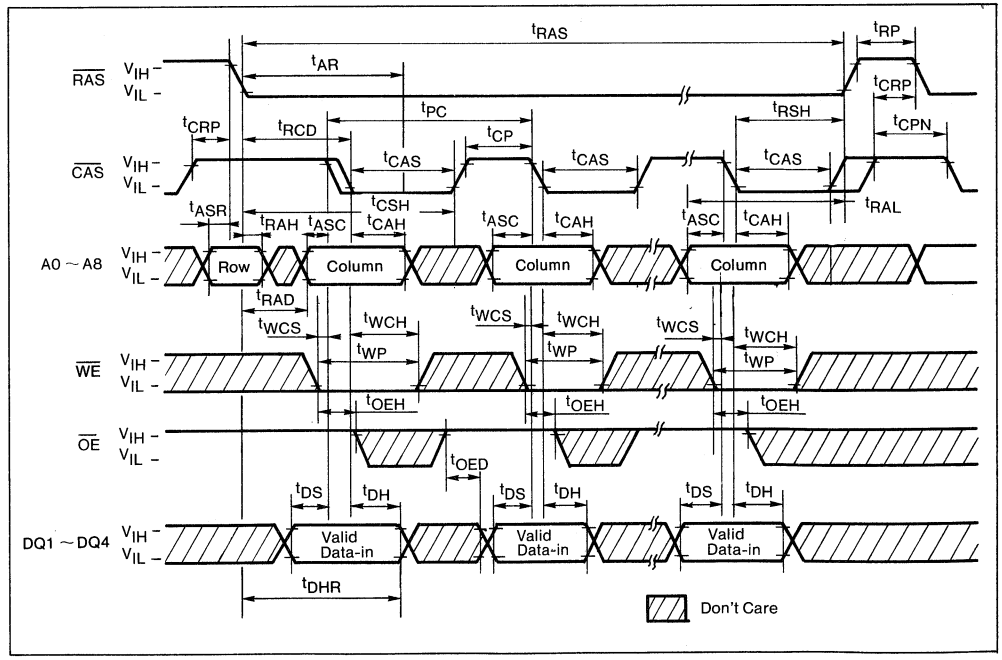
READ/WRITE CYCLE



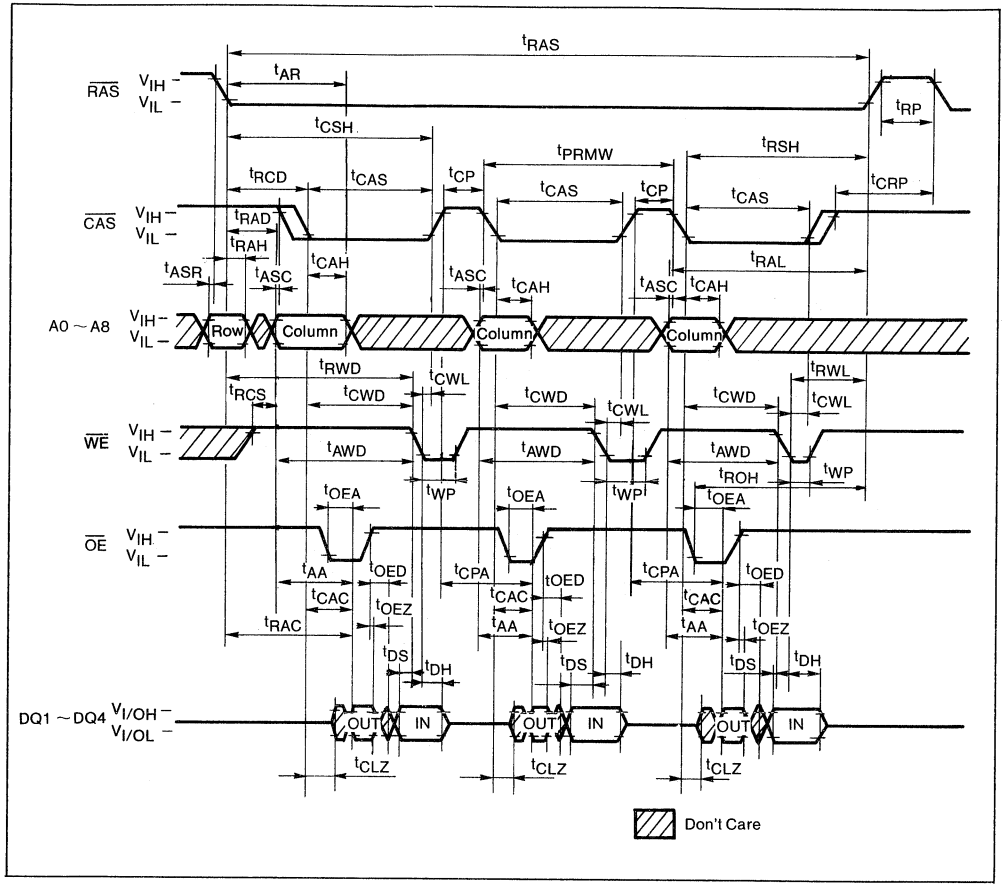
FAST PAGE MODE READ CYCLE



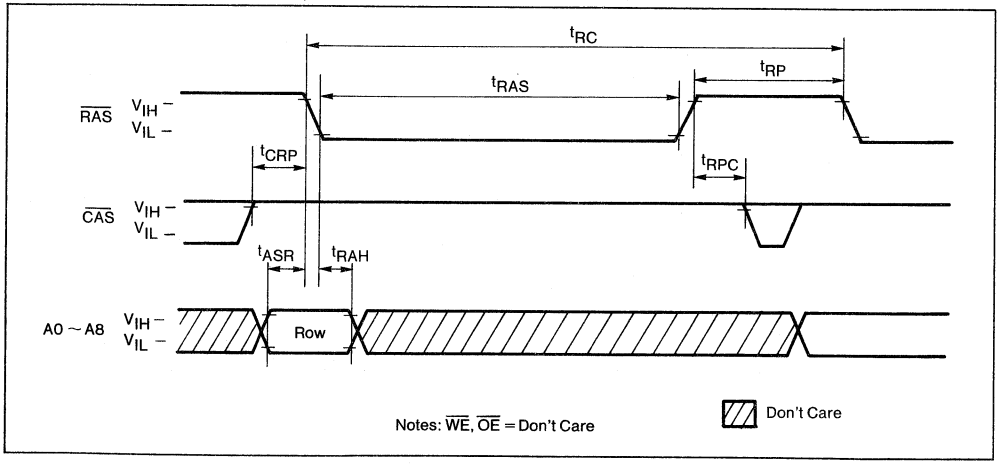
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



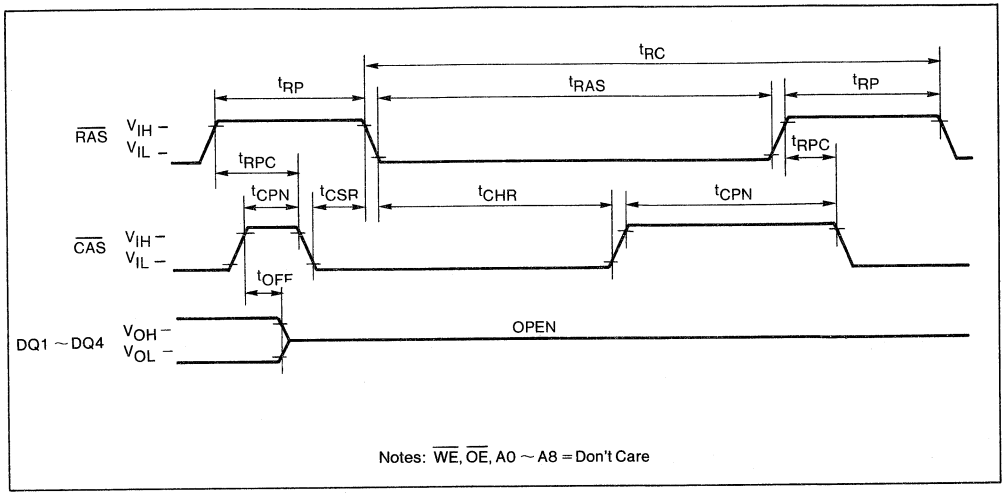
FAST PAGE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

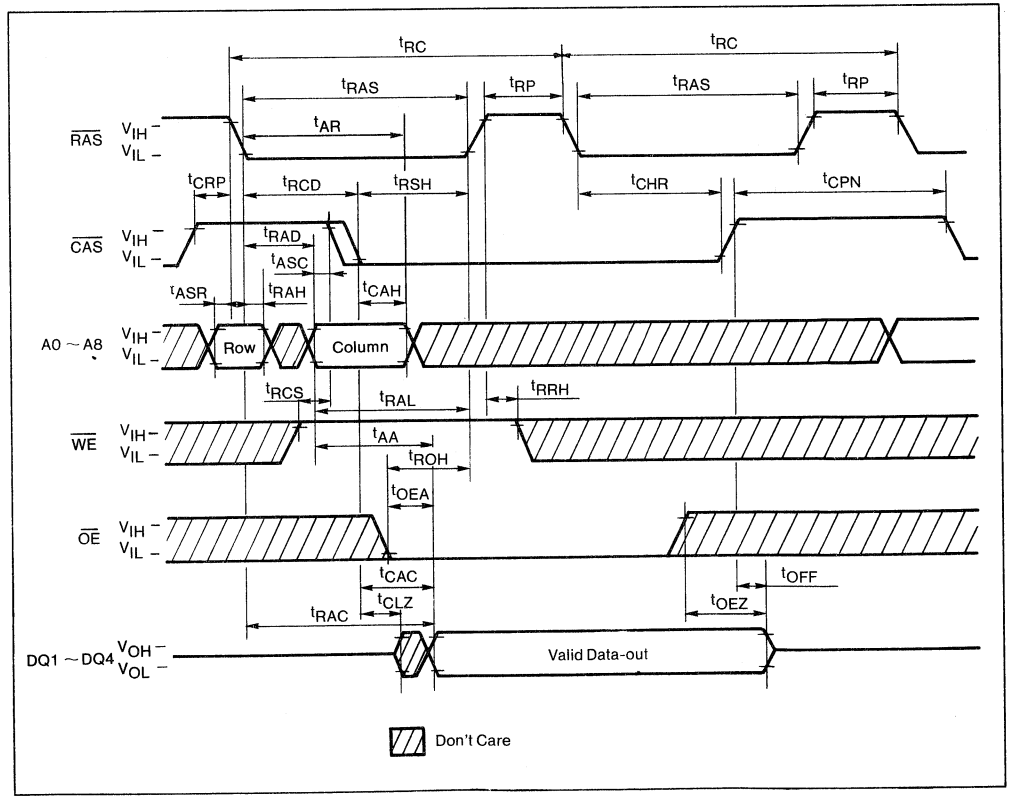


CAS BEFORE RAS AUTO REFRESH CYCLE

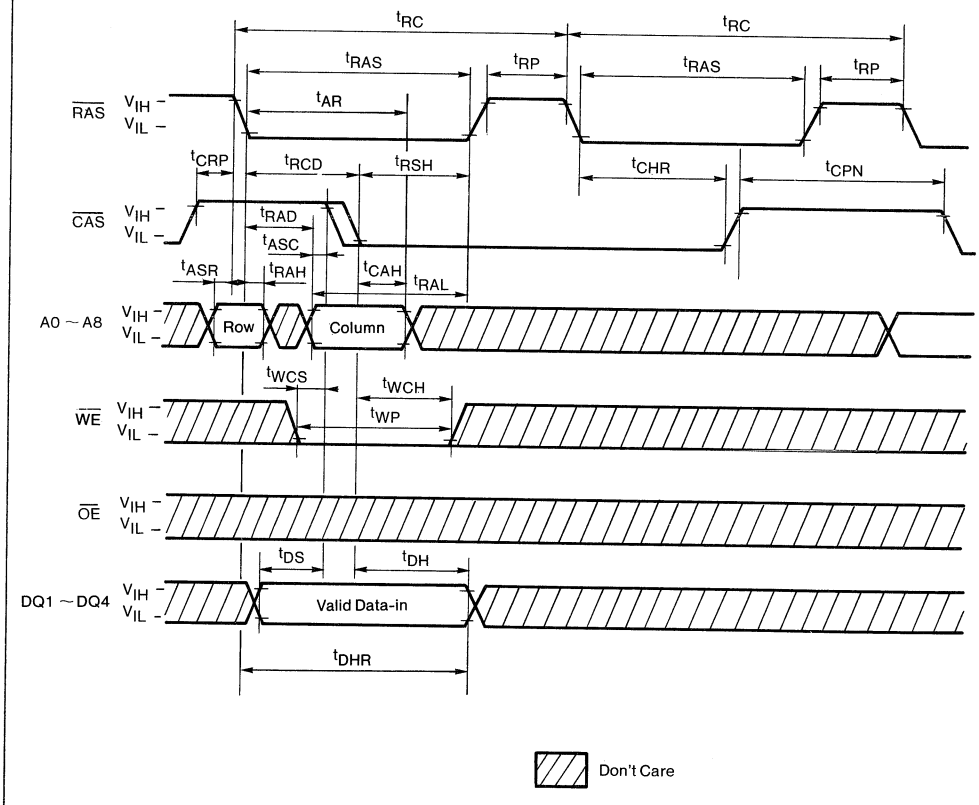


Notes: $\overline{WE}$, $\overline{OE}$, A0 ~ A8 = Don't Care

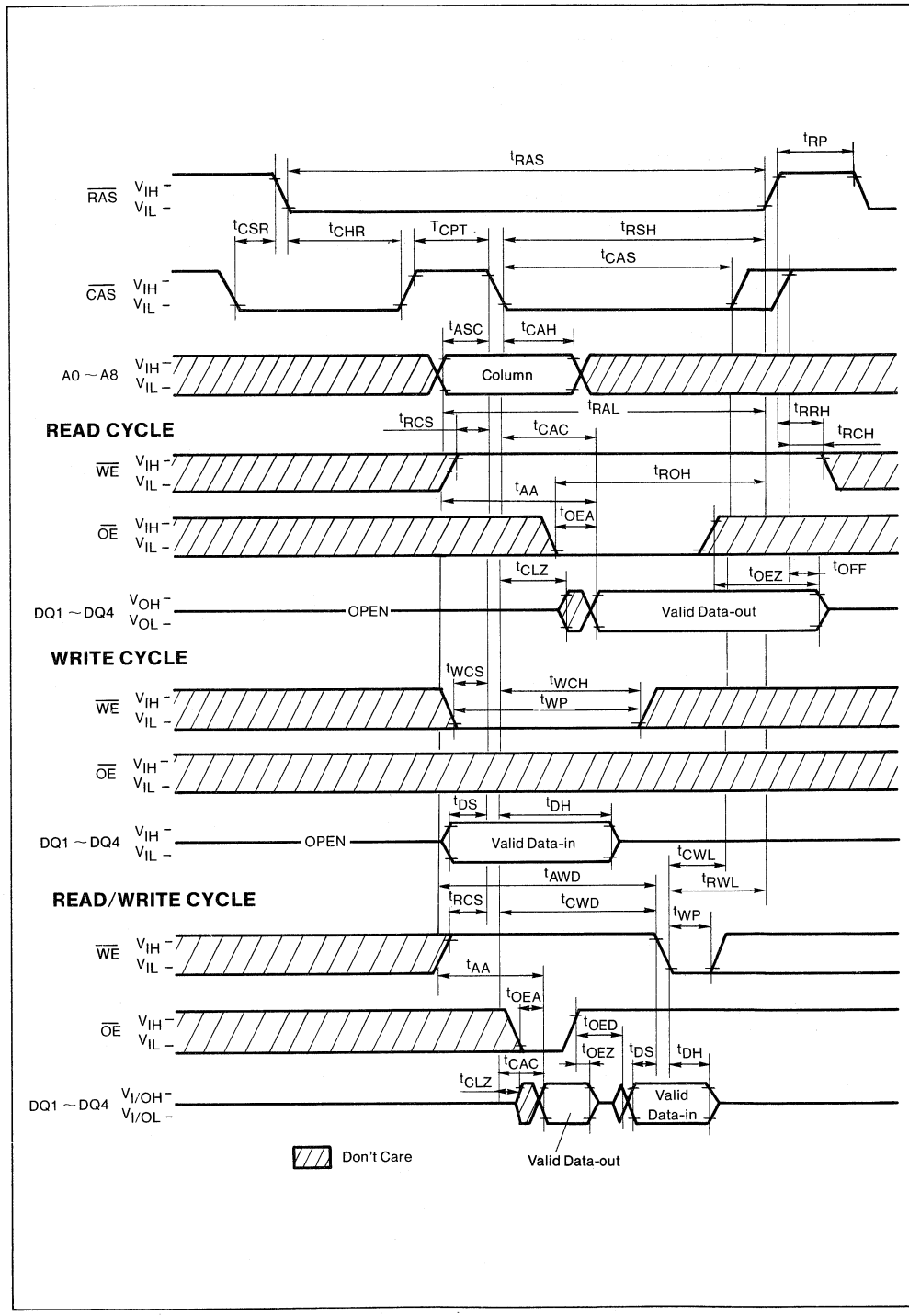
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



Preliminary

OKI semiconductor

MSM514258RS

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

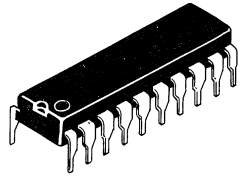
The MSM514258RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514258RS is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

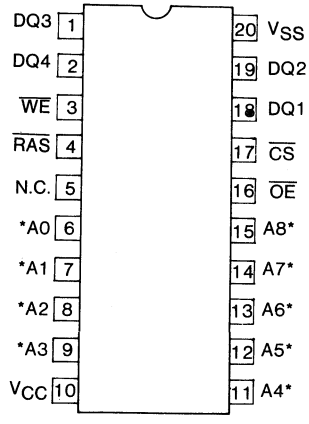
- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514258-10RS	100 ns	190 ns	413 mW	5.5 mW
MSM514258-12RS	120 ns	220 ns	358 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Static column mode, read/write capability capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit



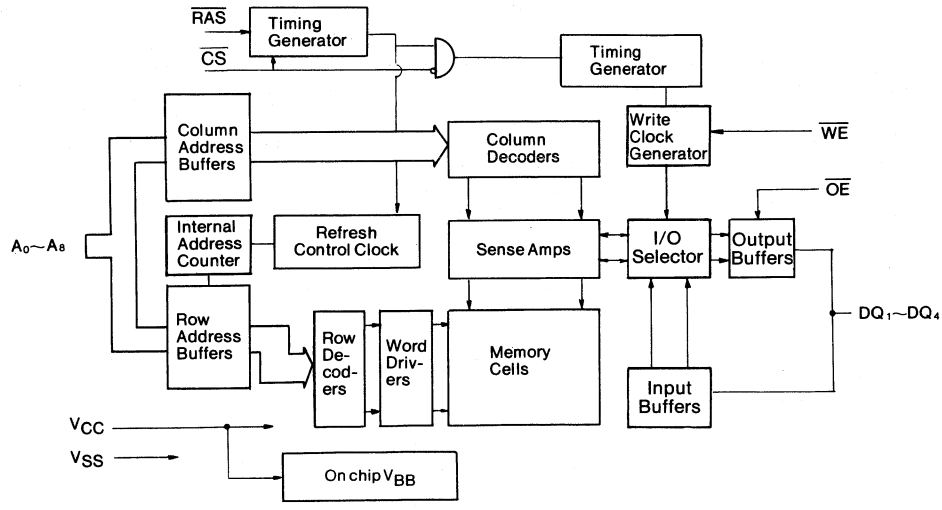
PIN CONFIGURATION (TOP VIEW)



*Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select input
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 514258-10		MSM 514258-12		Unit	Note
				MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V		−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V		−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min		–	75	–	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz	TTL	–	2	–	2	mA	
			MOS	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, t_{RC} = min		75	–	65	mA		
Average power supply current* ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$		75	–	65	mA		
Average power supply current* (Static column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ cycling, t_{SC} = min		55	–	50	mA		

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM514258-10		MSM514258-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	190	–	220	–	ns	
Read or write cycle time	t_{RWC}	255	–	295	–	ns	
Static column mode cycle time	t_{SC}	55	–	65	–	ns	
Static column mode read/write cycle time	t_{SRWC}	120	–	140	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5, 6
Access time from $\overline{CS}$	t_{CAC}	–	35	–	45	ns	4, 5
Access time from column address	t_{AA}	–	50	–	60	ns	4, 6, 7
Access time from last write	t_{ALW}	–	95	–	115	ns	4, 7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	30	–	35	ns	
Output buffer turn-off delay	t_{OFF}	0	25	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	35	–	45	–	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10	–	15	–	ns	
$\overline{CS}$ pulse width	t_{CS}	35	10000	45	10000	ns	
$\overline{CS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	65	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	6
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	25	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514258-10		MSM514258-12		Unit	Note
		MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ lead time	t_{RAL}	50	–	60	–	ns	
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	75	–	90	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	115	–	140	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	15	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	95	–	115	–	ns	
Last write to column address delay	t_{LWAD}	25	45	30	55	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	8
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write invalid time	t_{WI}	10	–	15	–	ns	
Write command hold time (D_{OUT} disable)	t_{WH}	0	–	0	–	ns	8
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	–	30	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	25	–	30	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	70	–	85	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	135	–	160	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	85	–	100	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	9
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	

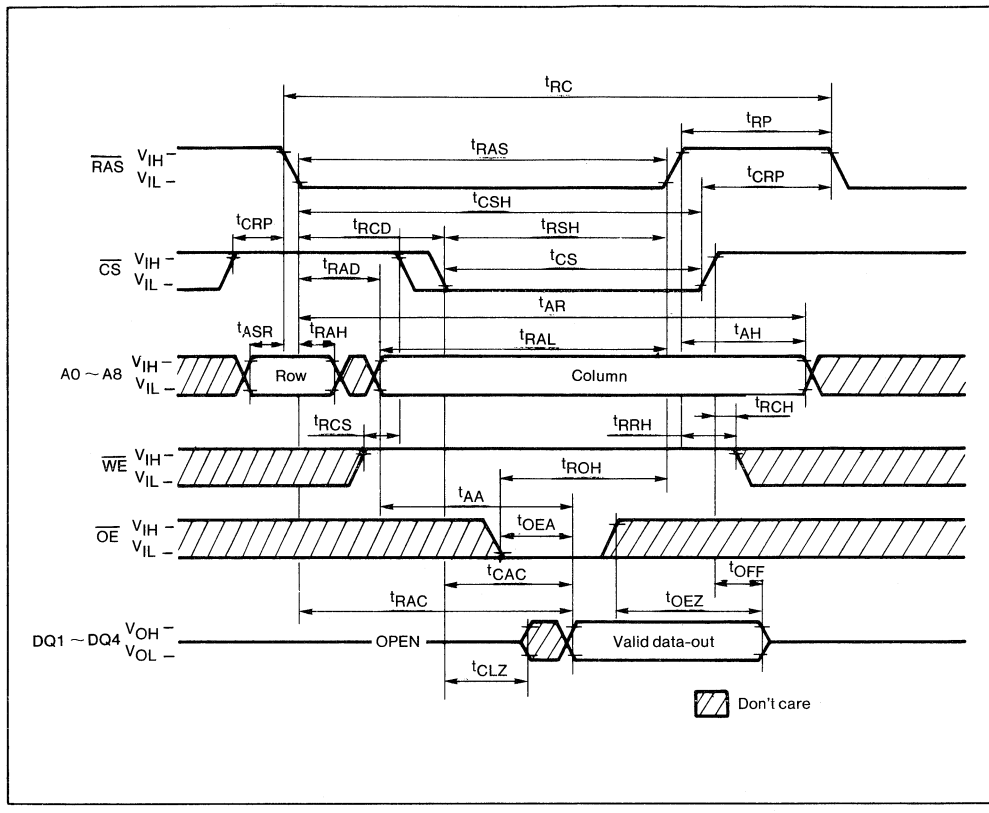
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514258-10		MSM514258-12		Unit	Note
		MIN	MAX	MIN	MAX		
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	
$\overline{CS}$ precharge time	t_{CPN}	15	–	20	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	25	–	30	ns	
$\overline{OE}$ delay time	t_{OED}	25	–	30	–	ns	
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	25	0	30	ns	
$\overline{OE}$ command hold time	t_{OEH}	25	–	30	–	ns	

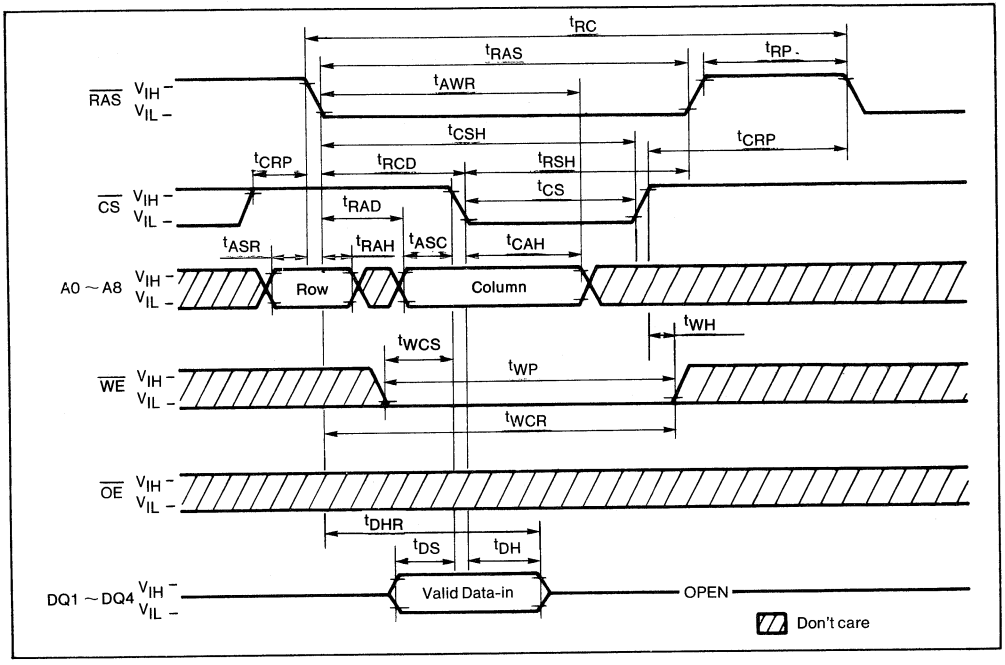
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively t_{AA}.
8. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

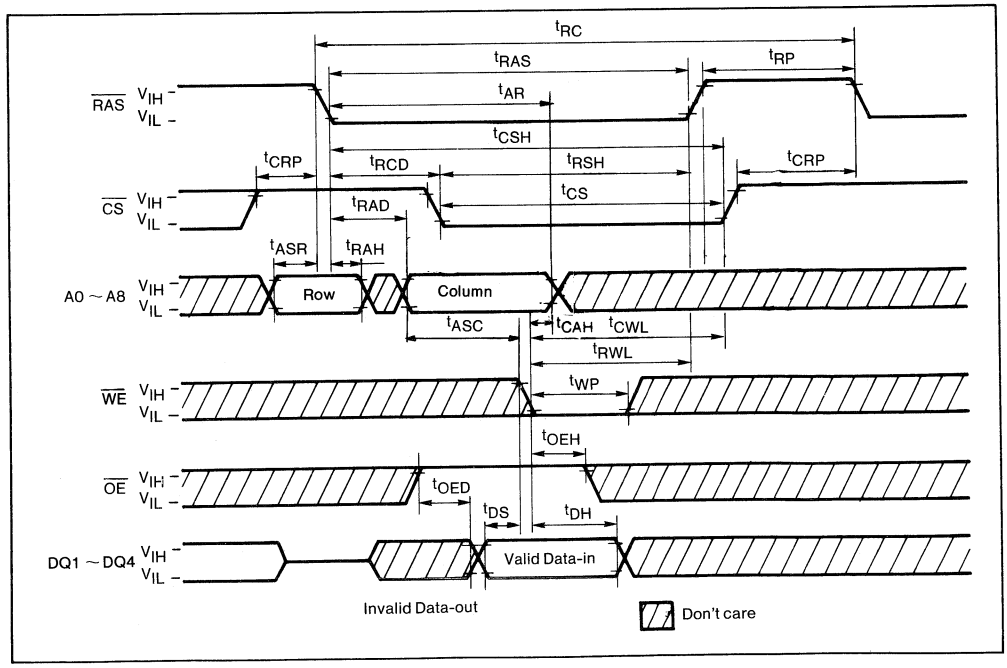
READ CYCLE


tRC
tRP
RAS VIH VIL
tRAS
tCRP
tCSH
tCRP
tRCD
tRSH
CS VIH VIL
tRAD
tCS
tAR
tASR
tRAH
tRAL
tAH
A0 ~ A8 VIH VIL
Row
Column
tRCH
tRCS
tRRH
WE VIH VIL
tROH
tAA
OE VIH VIL
tOEA
tCAC
tOFF
tRAC
tOEZ
DQ1 ~ DQ4 VOH VOL
OPEN
Valid data-out
tCLZ
Don't care

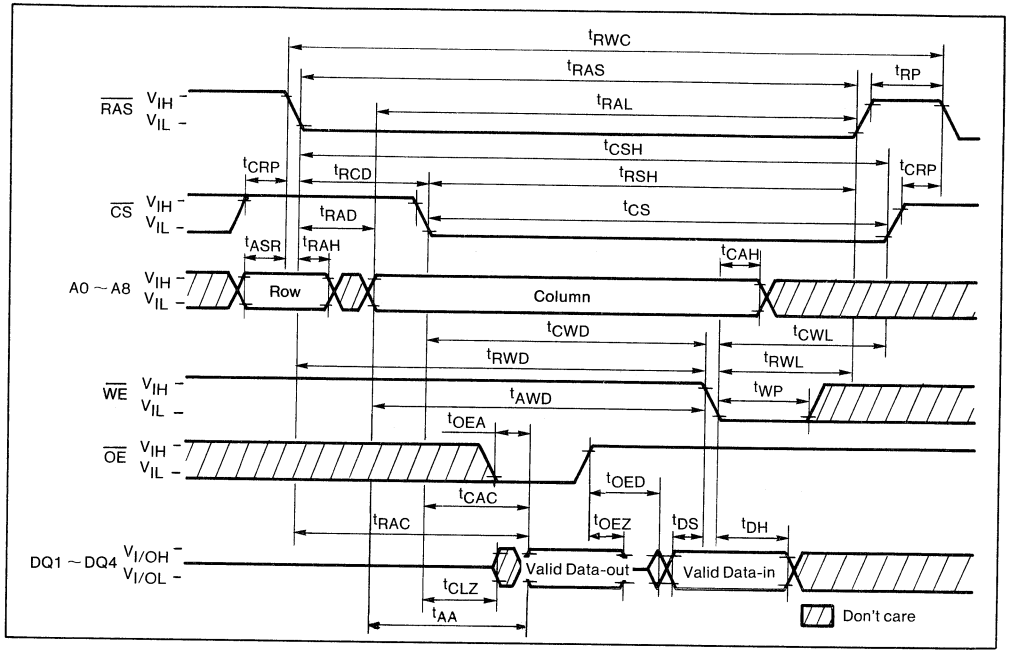
WRITE CYCLE (EARLY WRITE)



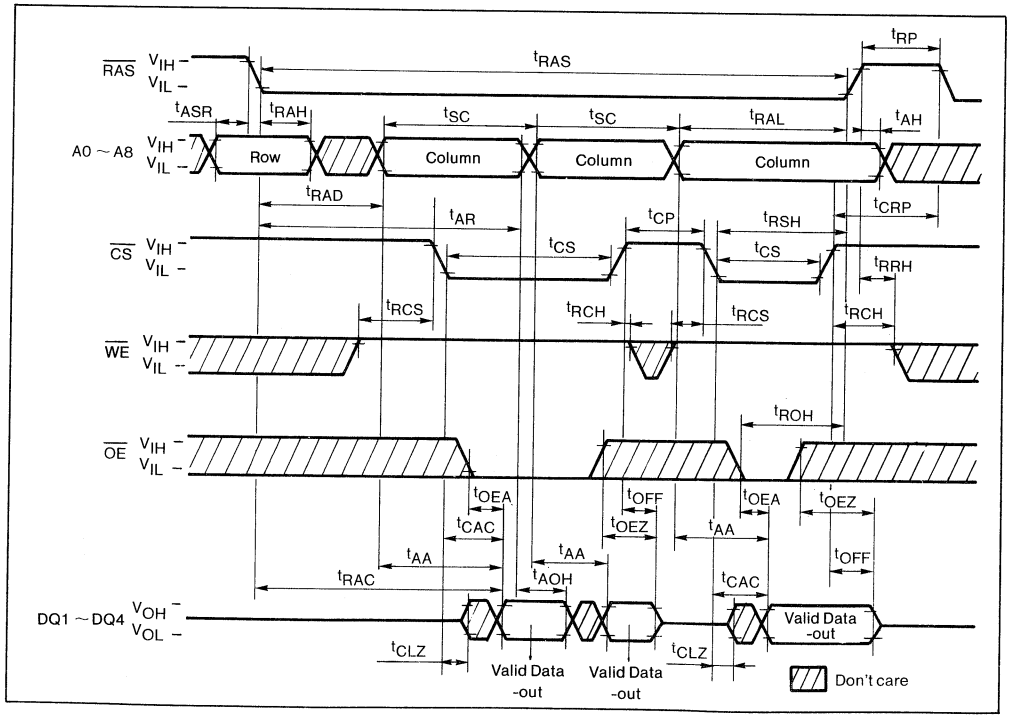
WRITE ($\overline{OE}$ CONTROL WRITE)



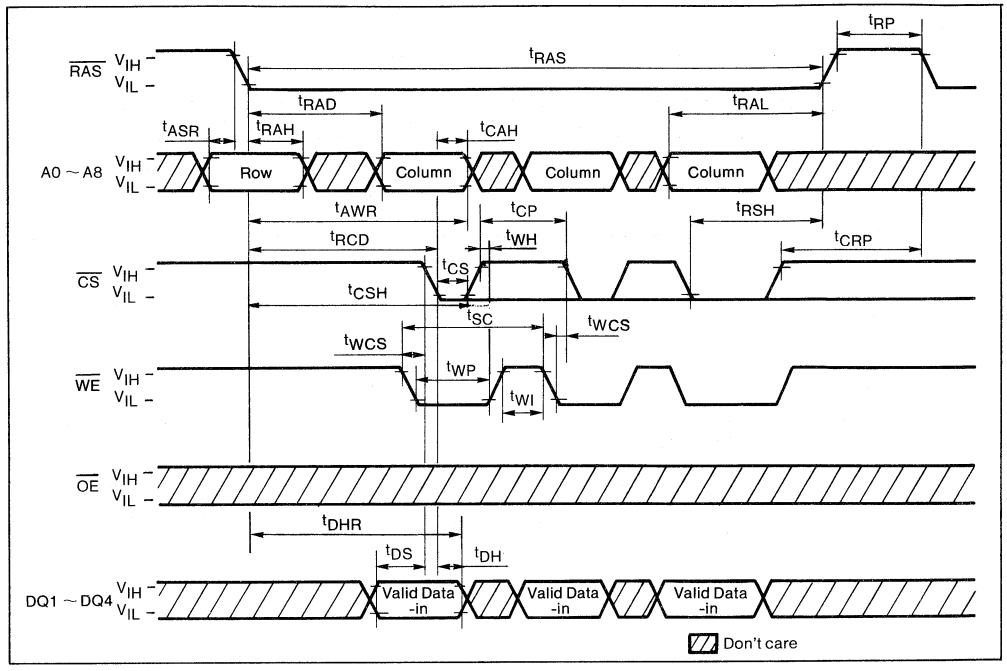
READ/WRITE CYCLE



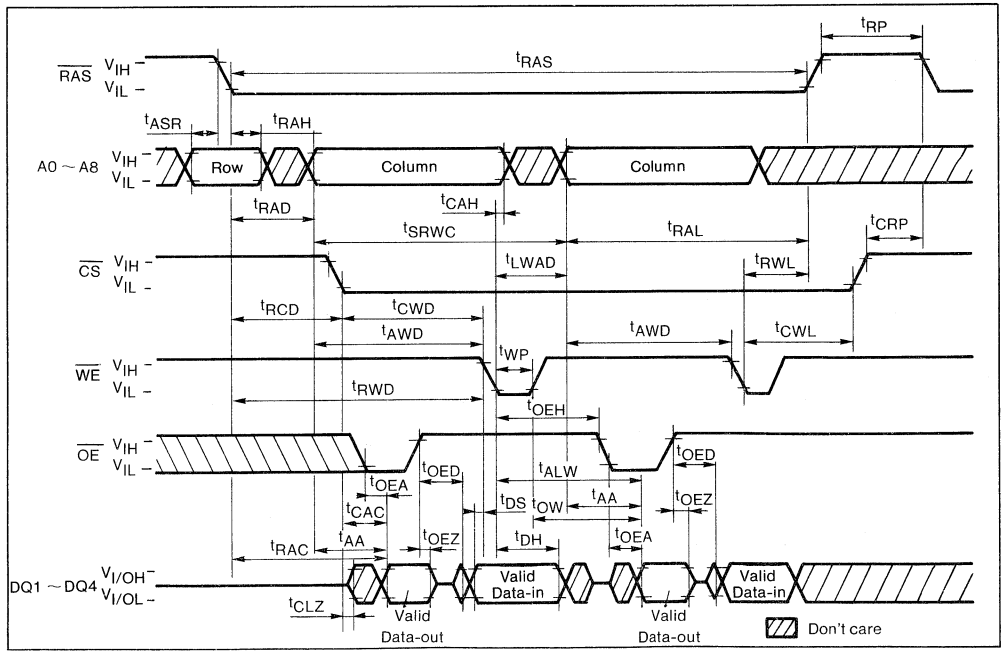
STATIC COLUMN MODE READ CYCLE



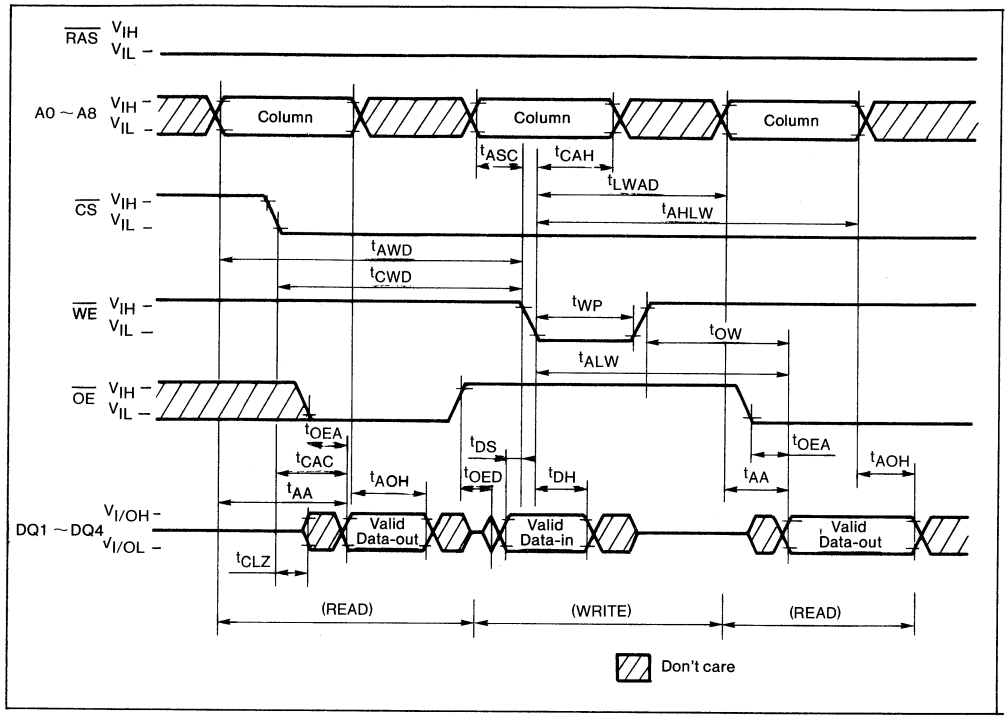
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



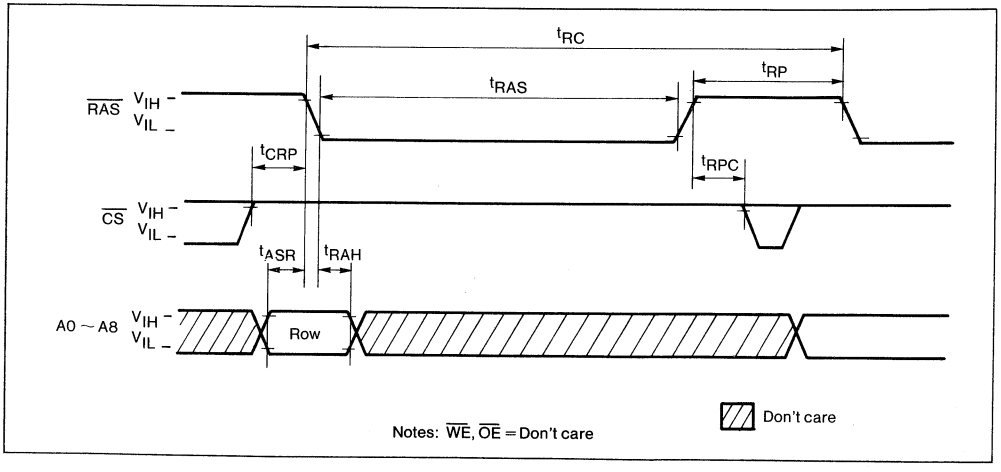
STATIC COLUMN MODE READ/WRITE CYCLE



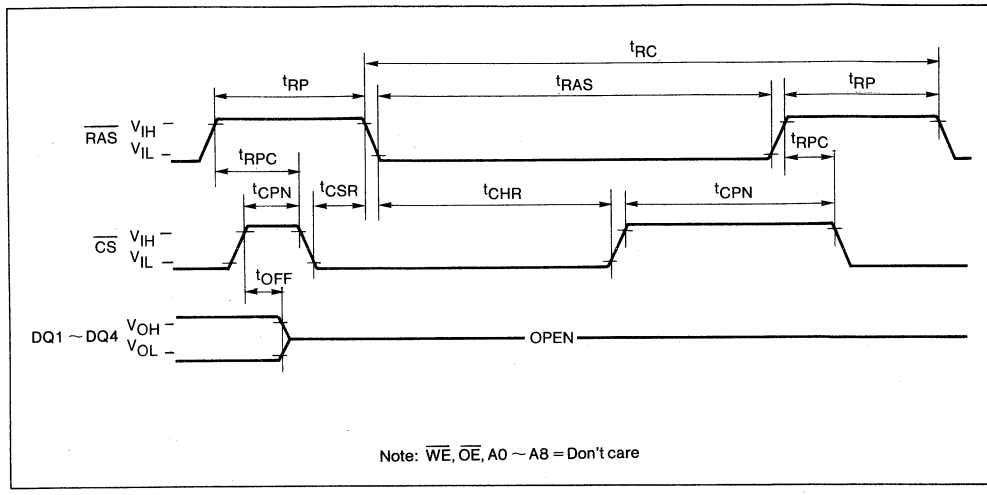
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



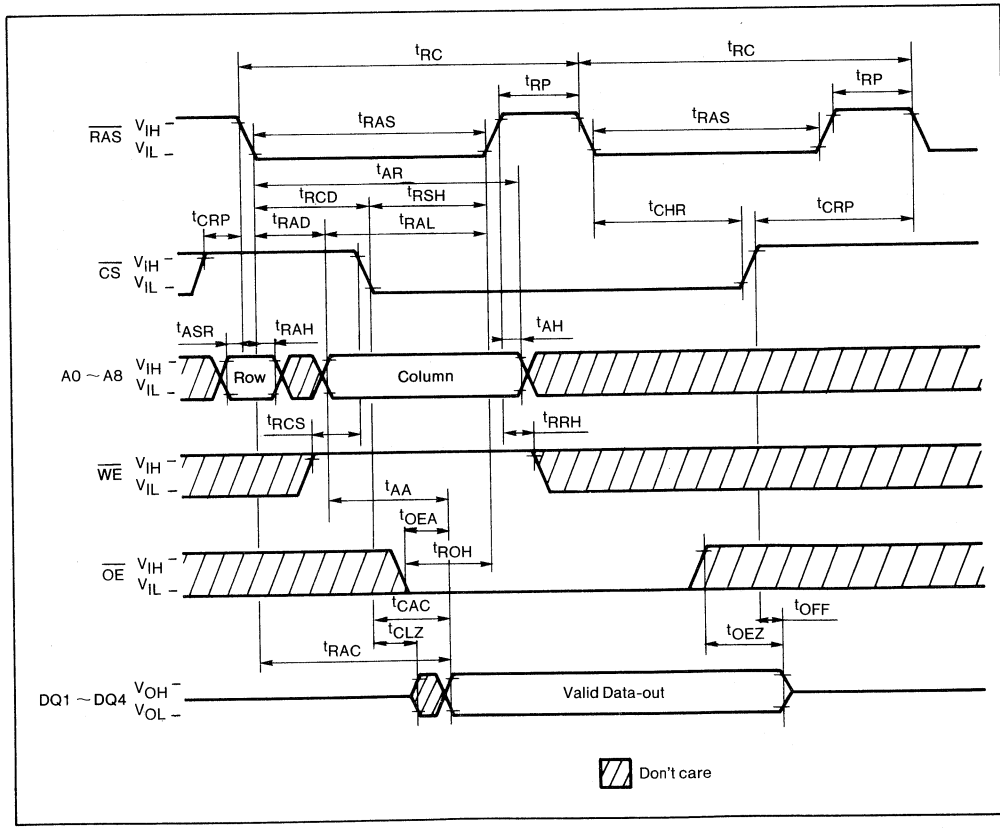
RAS ONLY REFRESH CYCLE



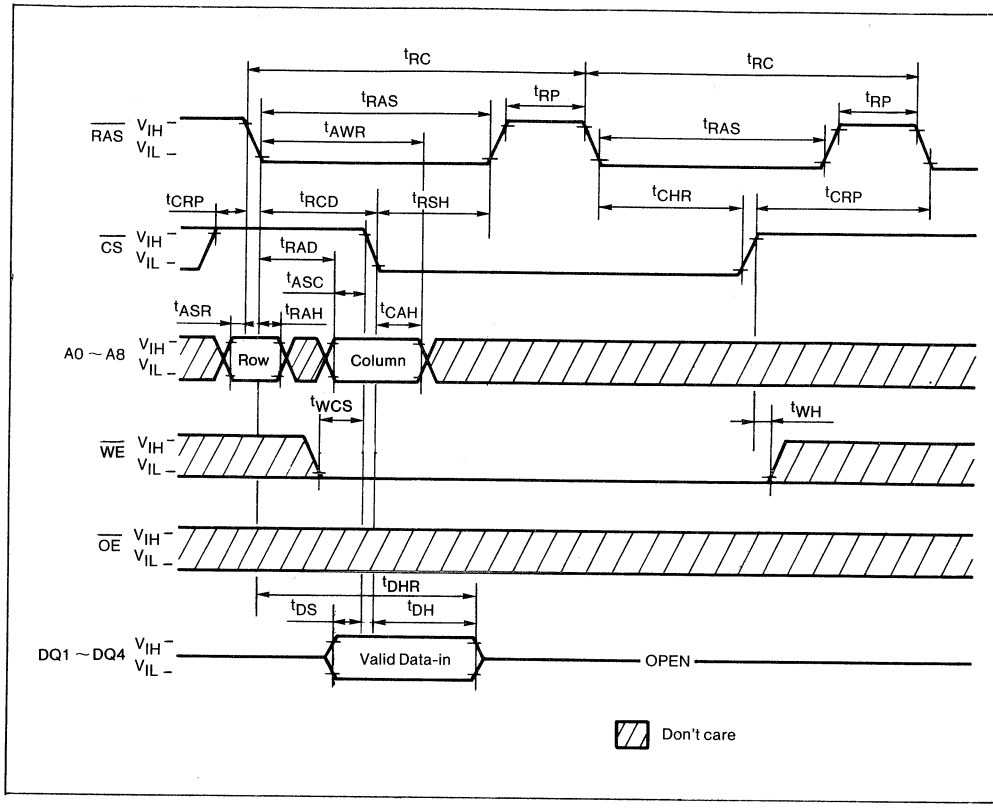
$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



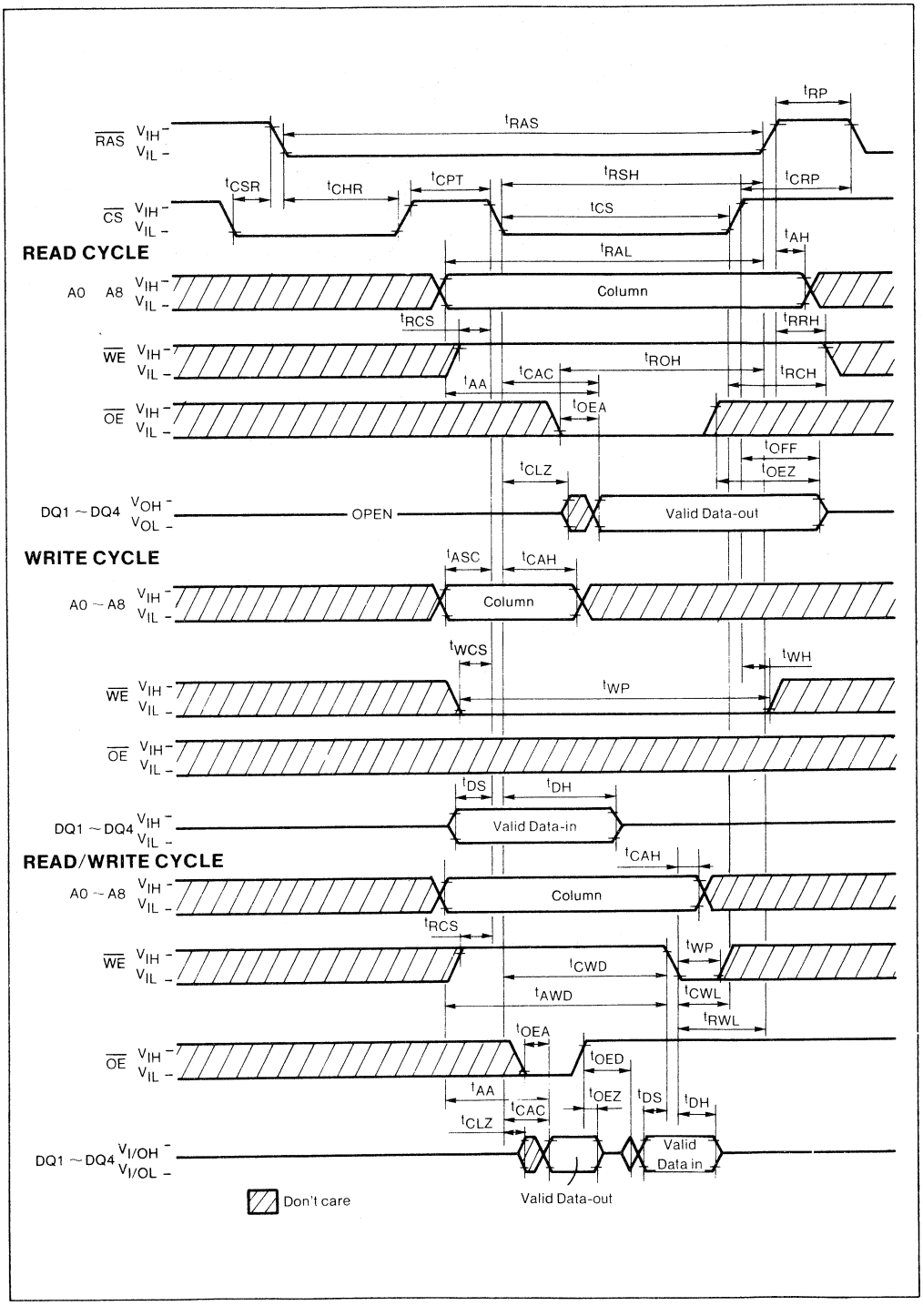
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



MSC2304YS8/KS8

262,144 BY 8 BIT DYNAMIC RAM MODULE <Page Mode Type>

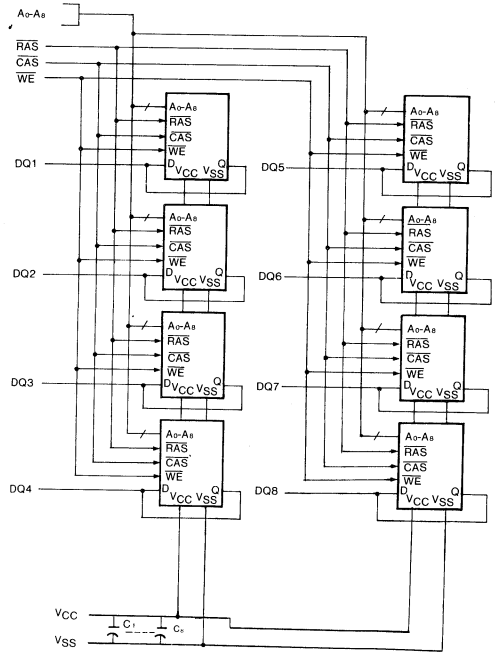
GENERAL DESCRIPTION

The Oki MSC2304YS8/KS8 is a fully decoded, 262,144 words × 8 bit NMOS dynamic random access memory composed of eight 256K DRAMs in plastic leaded chip carrie (MSM41256AJS). The mounting of eight PLCCs together with eight 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS8/KS8 are quite same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

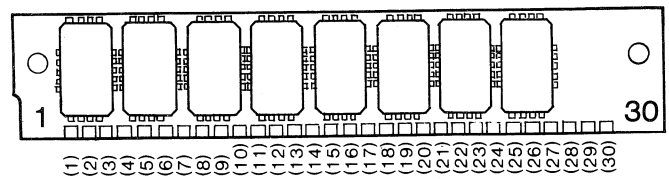
- 262,144 word × 8 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Row Access Time;
  - 100ns max. (MSC2304-10YS8/KS8)
  - 120ns max. (MSC2304-12YS8/KS8)
  - 150ns max. (MSC2304-15YS8/KS8)
- Low Power Dissipation;
  - 2640mW max. (MSC2304-10YS8/KS8)
  - 2420mW max. (MSC2304-12YS8/KS8)
  - 2200mW max. (MSC2304-15YS8/KS8)
- Operating Temperature ... 0°C to 70°C
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- "Page Mode" capability

FUNCTIONAL BLOCK DIAGRAM

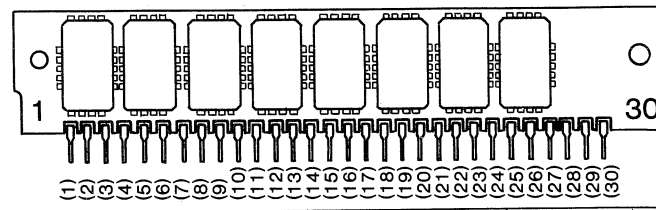


PIN ASSIGNMENT

MSC2304YS8



MSC2304KS8



PIN No.	PIN NAME	PIN No.	PIN NAME
1	$\overline{CAS}$	16	DQ5
2	DQ1	17	A8
3	A0	18	NC
4	A1	19	NC
5	DQ2	20	$\overline{DQ6}$
6	A2	21	$\overline{WE}$
7	A3	22	VSS
8	VSS	23	DQ7
9	DQ3	24	NC
10	A4	25	DQ8
11	A5	26	$\overline{NC}$
12	DQ4	27	$\overline{RAS}$
13	A6	28	NC
14	A7	29	NC
15	V_{CC}	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		480		440		400	mA
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		40		40		40	mA
Refresh Current 1 Average power supply current (RAS cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		440		400		360	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, CAS cycling; t_{PC} = min.)	I_{CC4}		320		280		240	mA
Refresh Current 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		440		400		360	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−80	80	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	37	60	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Note 1, 2, 3

Parameter	Symbol	Unit	MSC2304-10 YS8/KS8		MSC2304-12 YS8/KS8		MSC2304-15 YS8/KS8		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		

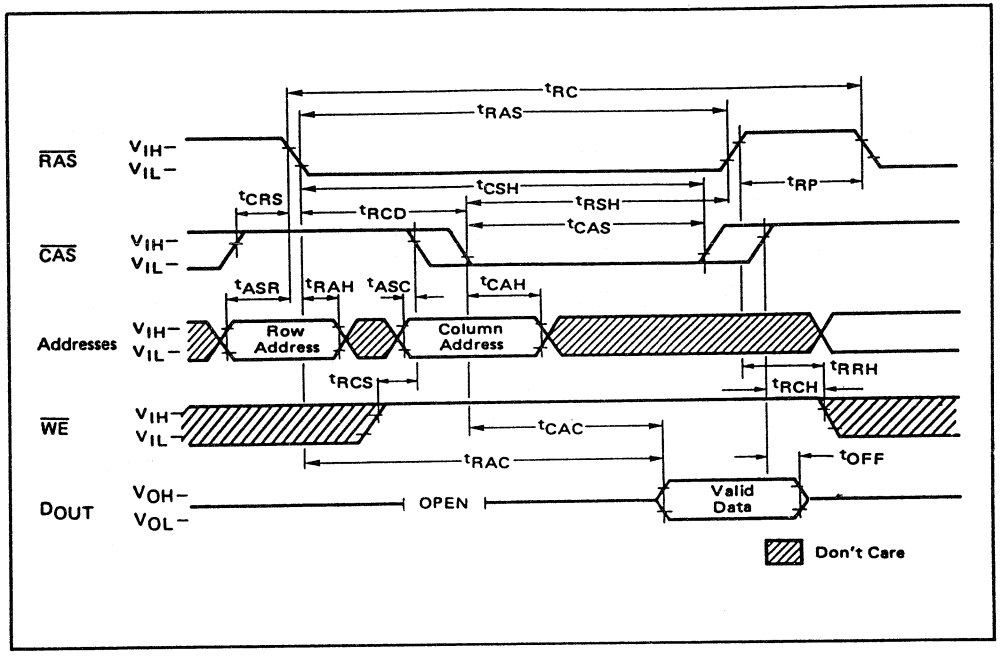
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSC2304-10 YS8/KS8		MSC2304-12 YS8/KS8		MSC2304-15 YS8/KS8		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		8
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		8

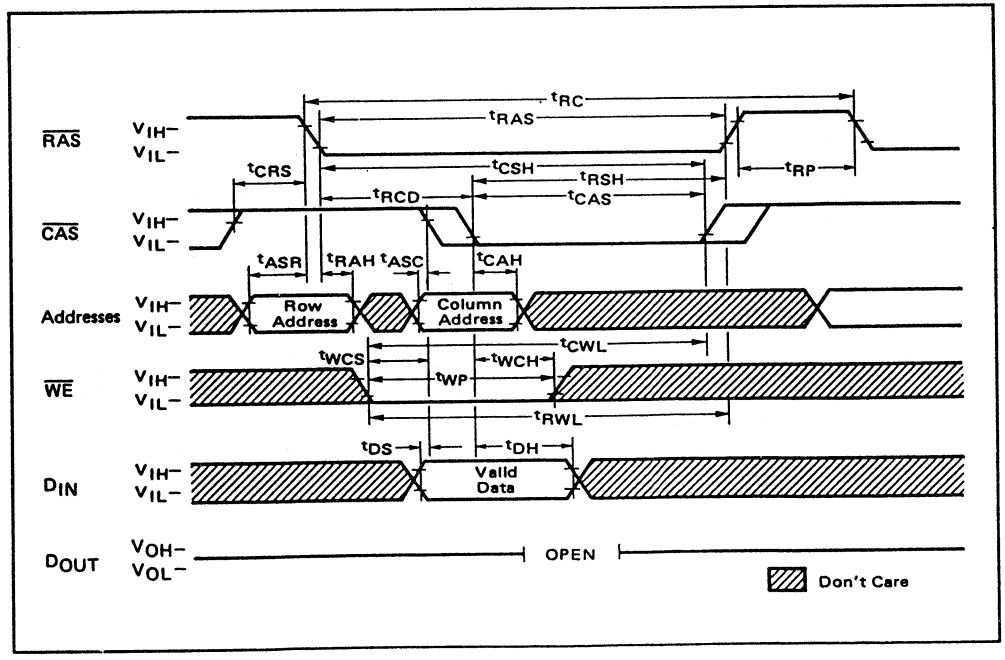
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Page mode cycle.

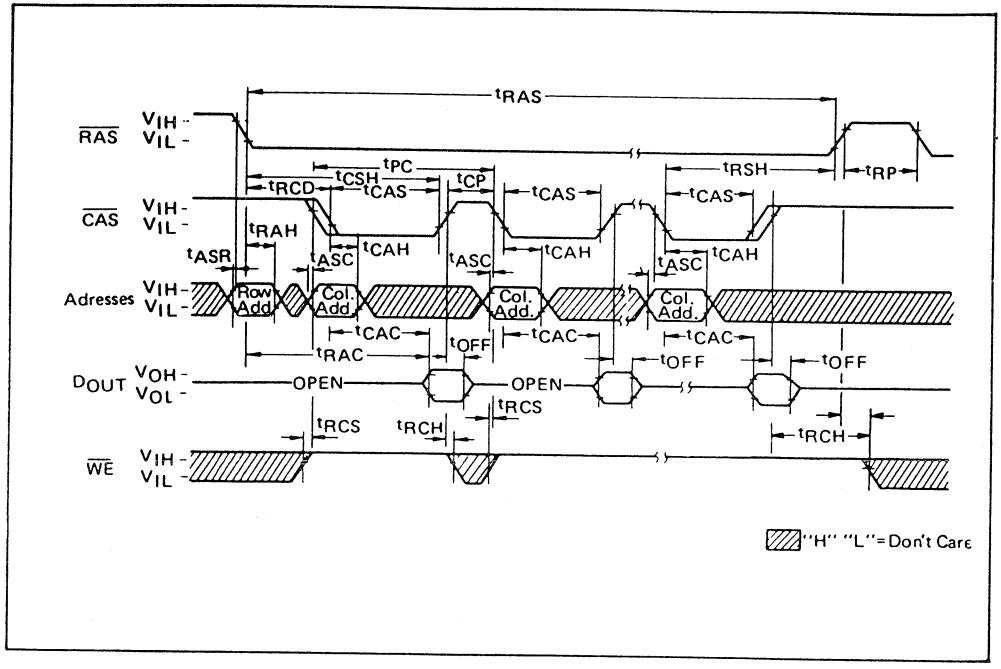
READ CYCLE



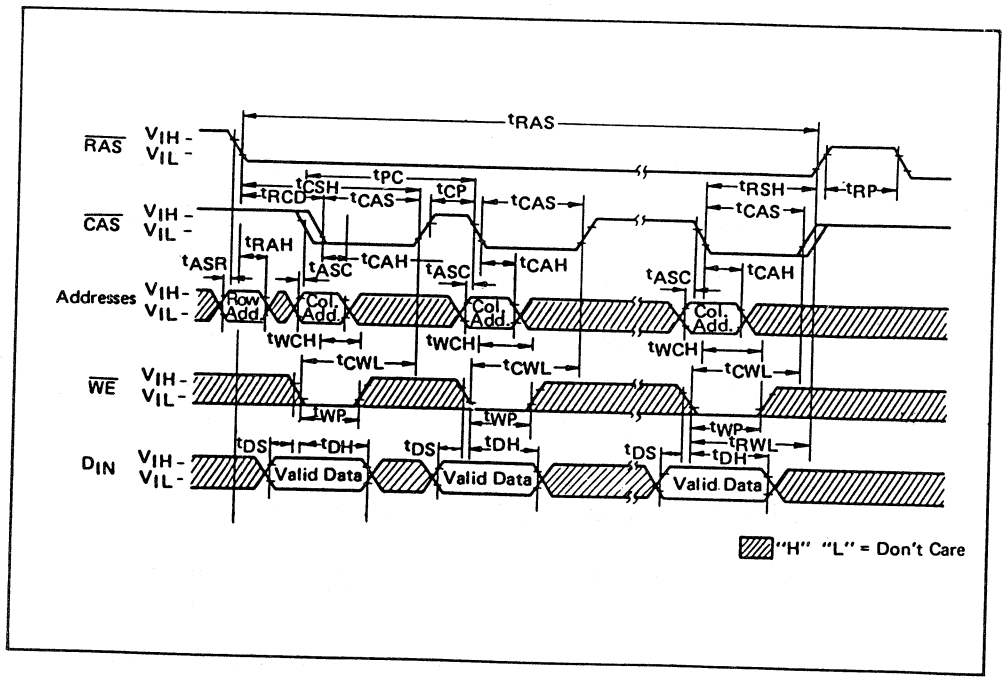
WRITE CYCLE



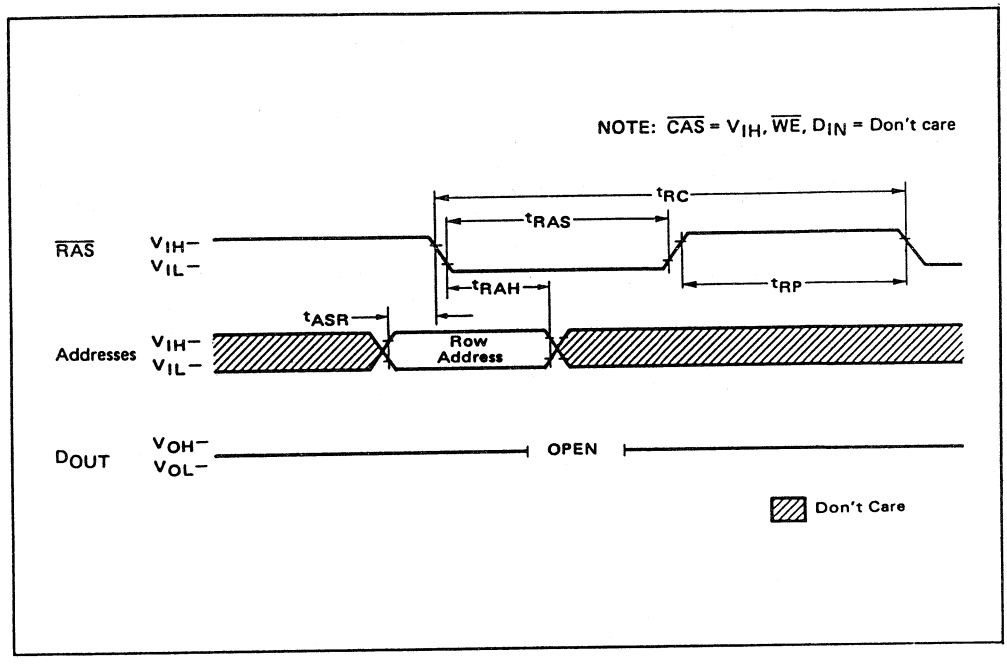
PAGE MODE READ CYCLE



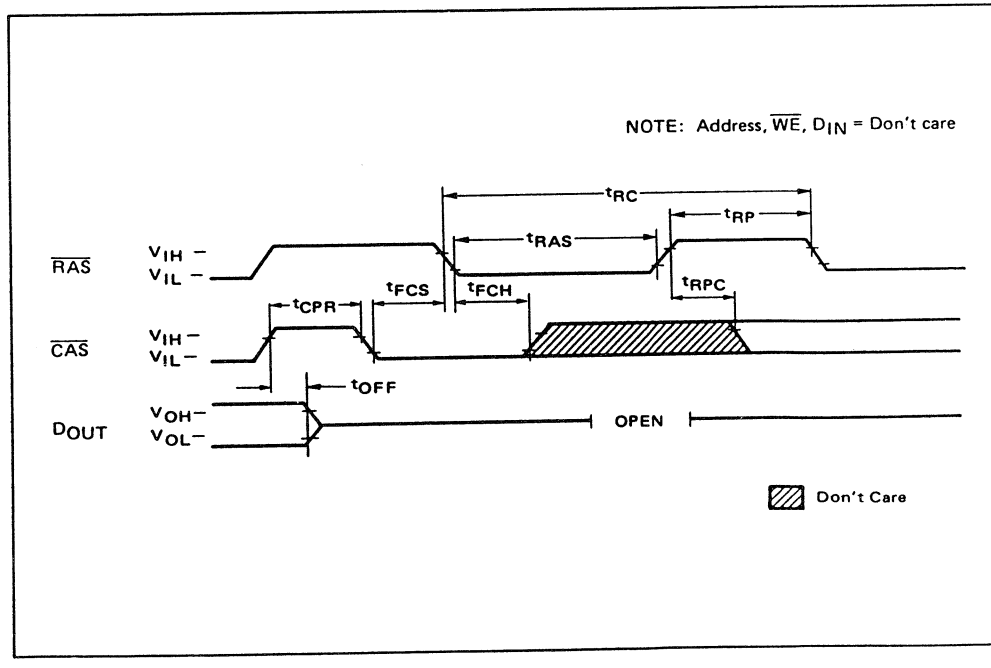
PAGE MODE WRITE CYCLE



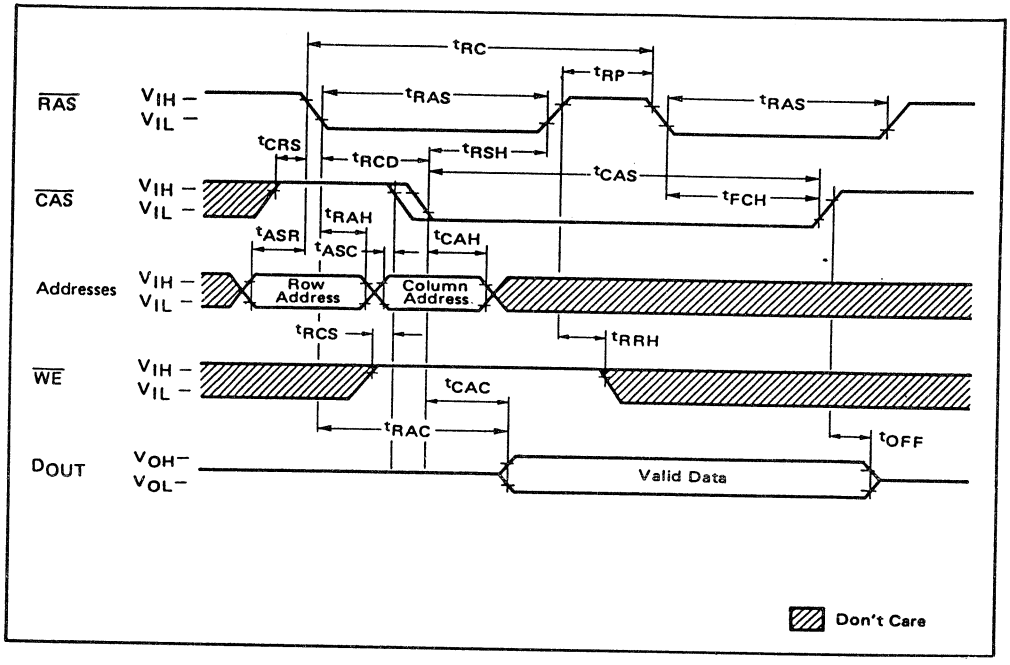
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2304 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2304 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition the MSC2304 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSC2304 can commit better memory system through-put during operations in an interleaved system.

leaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSC2304. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

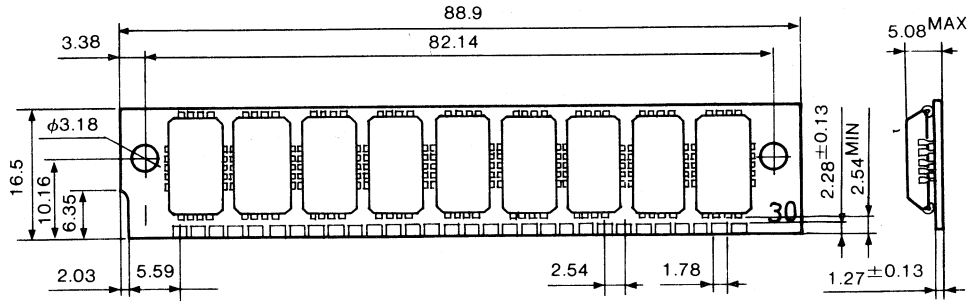
$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

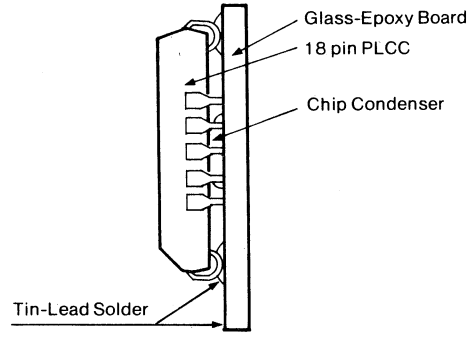
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSC2304 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSC2304 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

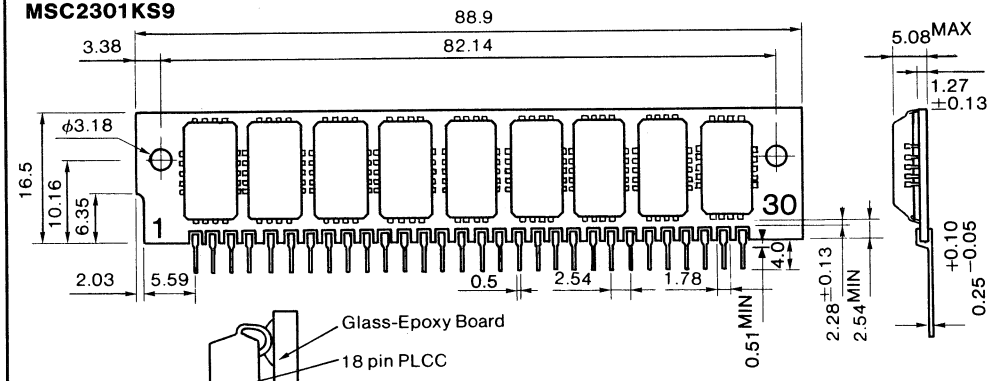
MSC2301YS9

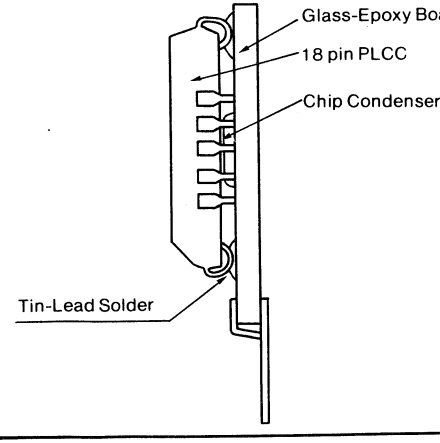




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

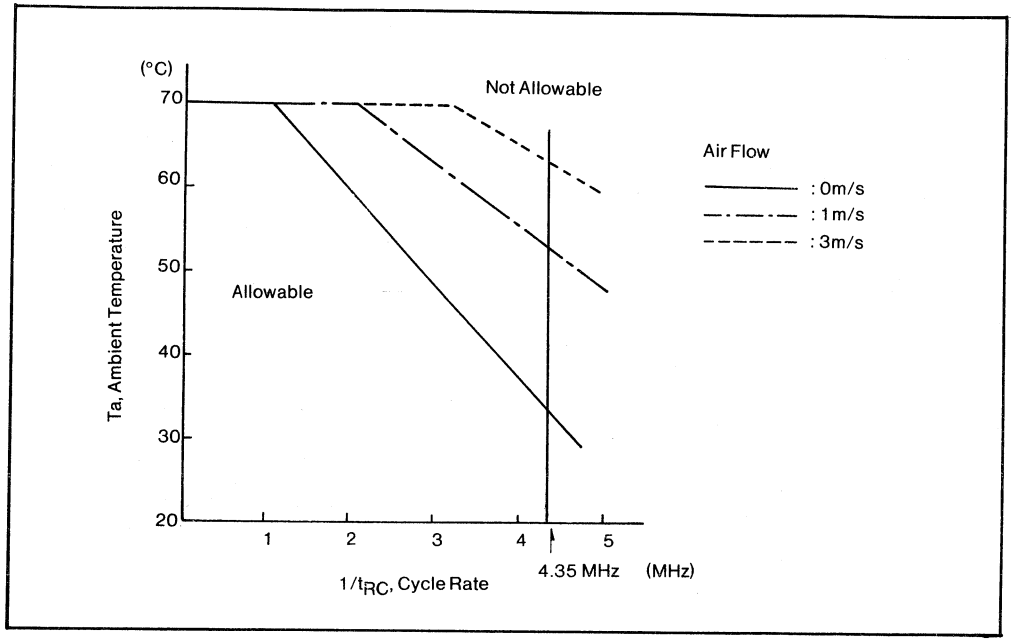
MSC2301KS9





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304YS8/KS8 (SIP/SIM) DERATING CURVE



MSC2304YS9/KS9

262,144 BY 9 BIT DYNAMIC RAM MODULE <Page Mode Type>

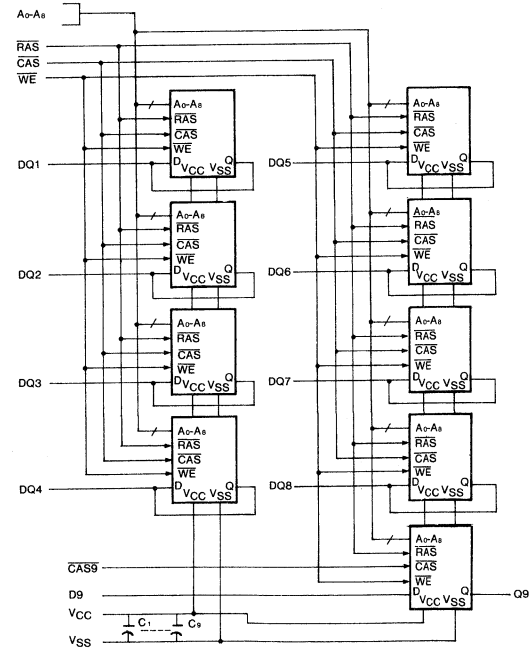
GENERAL DESCRIPTION

The Oki MSC2304YS9/KS9 is a fully decoded, 262,144 words × 9 bit NMOS dynamic random access memory composed of nine 256K DRAMs in plastic leaded chip carrier (MSM41256AJS). The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS9/KS9 are quite same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

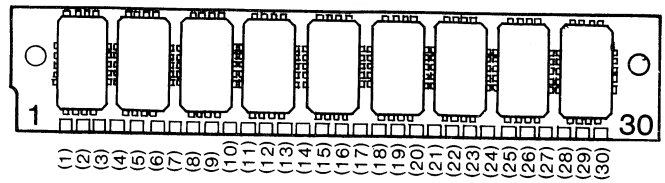
- 262,144 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
  100ns max. (MSC2304-10YS9/KS9)
  120ns max. (MSC2304-12YS9/KS9)
  150ns max. (MSC2304-15YS9/KS9)
- Low Power Dissipation;
  2970mW max. (MSC2304-10YS9/KS9)
  2723mW max. (MSC2304-12YS9/KS9)
  2475mW max. (MSC2304-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

FUNCTIONAL BLOCK DIAGRAM

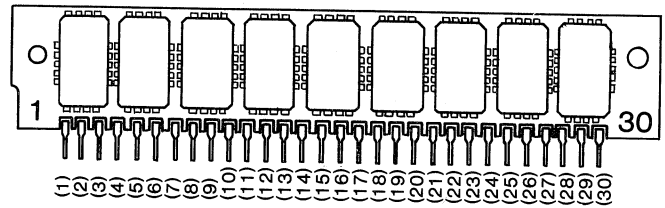


PIN ASSIGNMENT

MSC2304YS9



MSC2304KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		540		495		450	mA
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		45		45		45	mA
Refresh Current 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		495		450		405	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		360		315		270	mA
Refresh Current 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		495		450		405	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−90	90	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSC2304-10 YS9/KS9		MSC2304-12 YS9/KS9		MSC2304-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		8

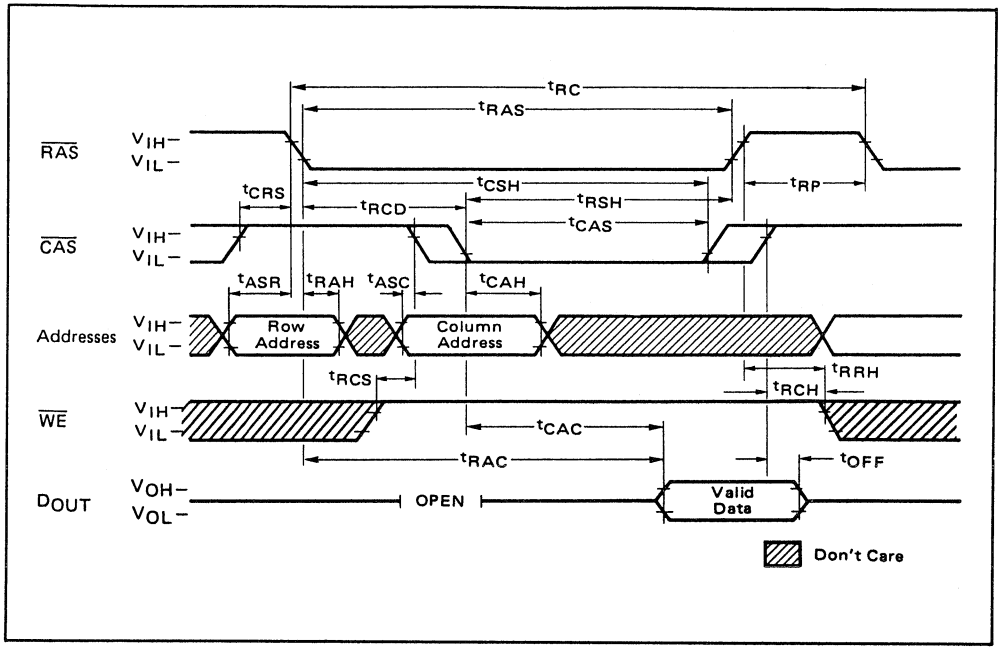
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSC2304-10 YS9/KS9		MSC2304-12 YS9/KS9		MSC2304-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		8
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		8

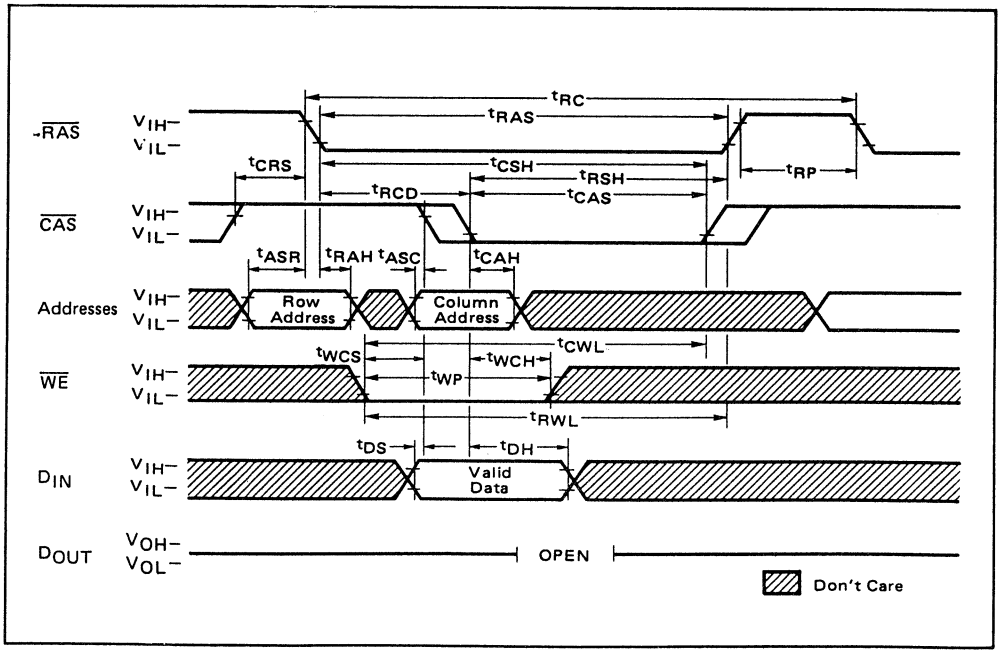
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Page mode cycle.

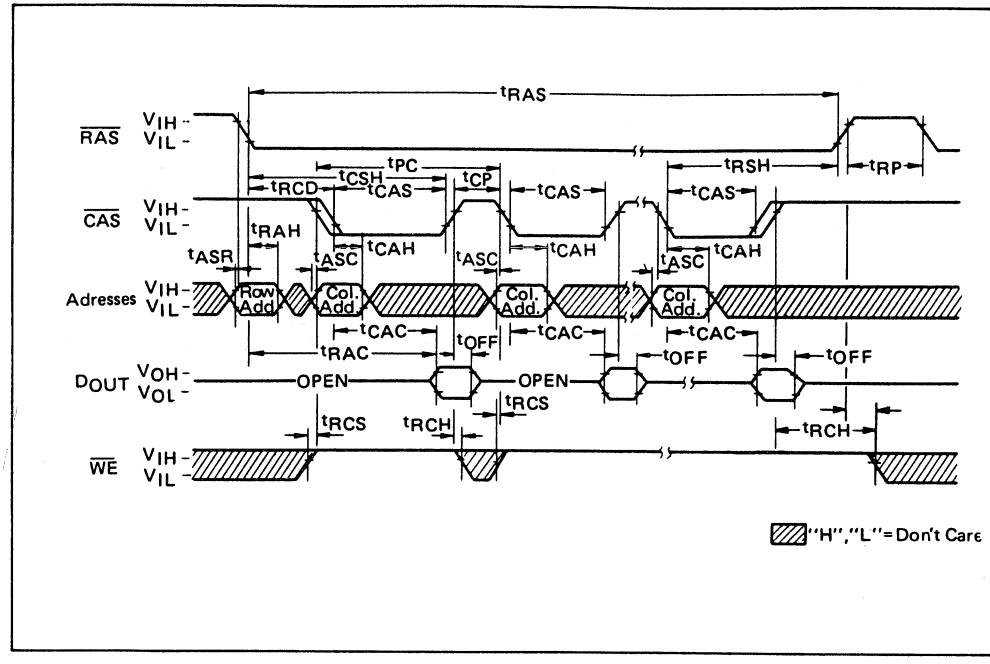
READ CYCLE



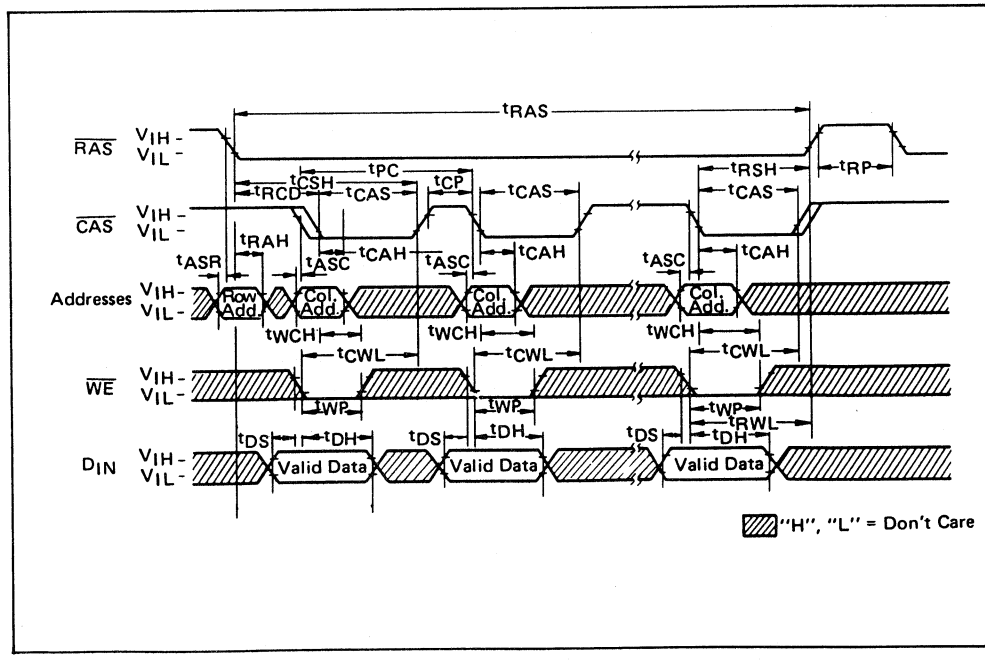
WRITE CYCLE



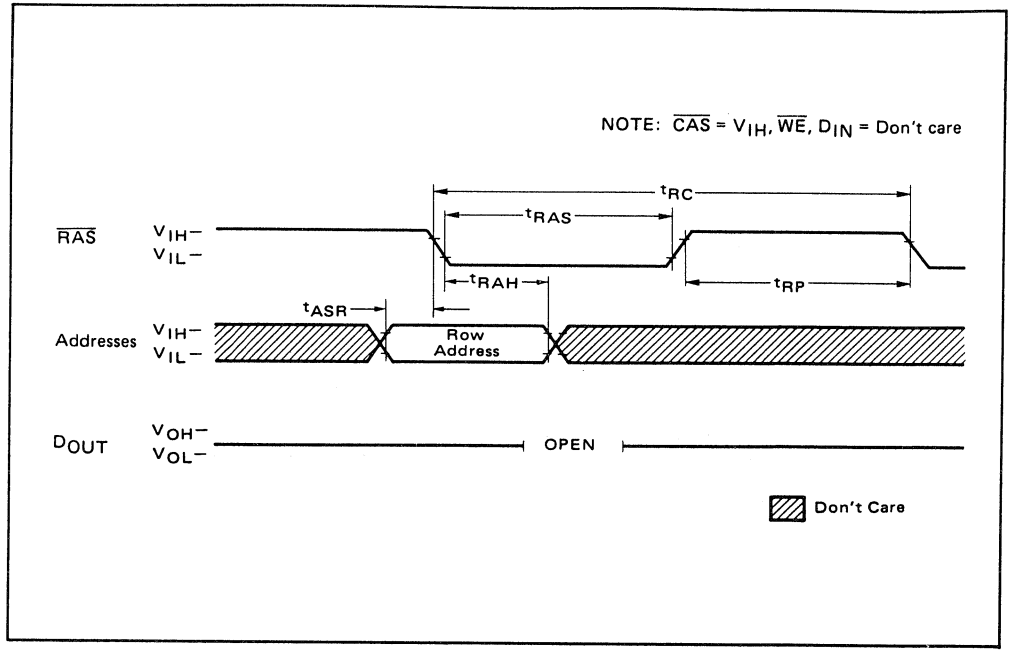
PAGE MODE READ CYCLE



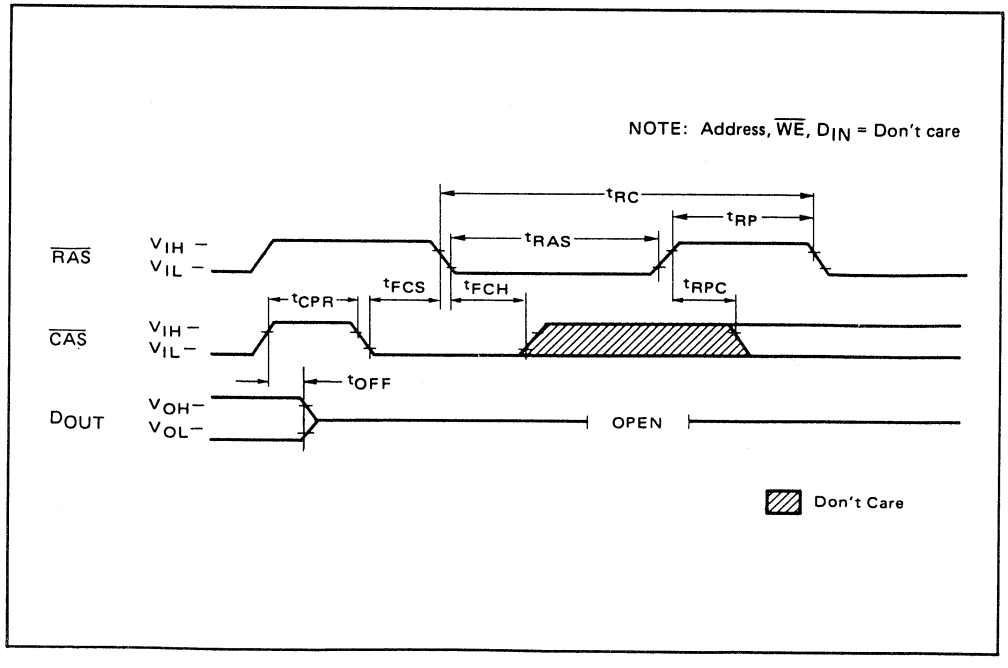
PAGE MODE WRITE CYCLE



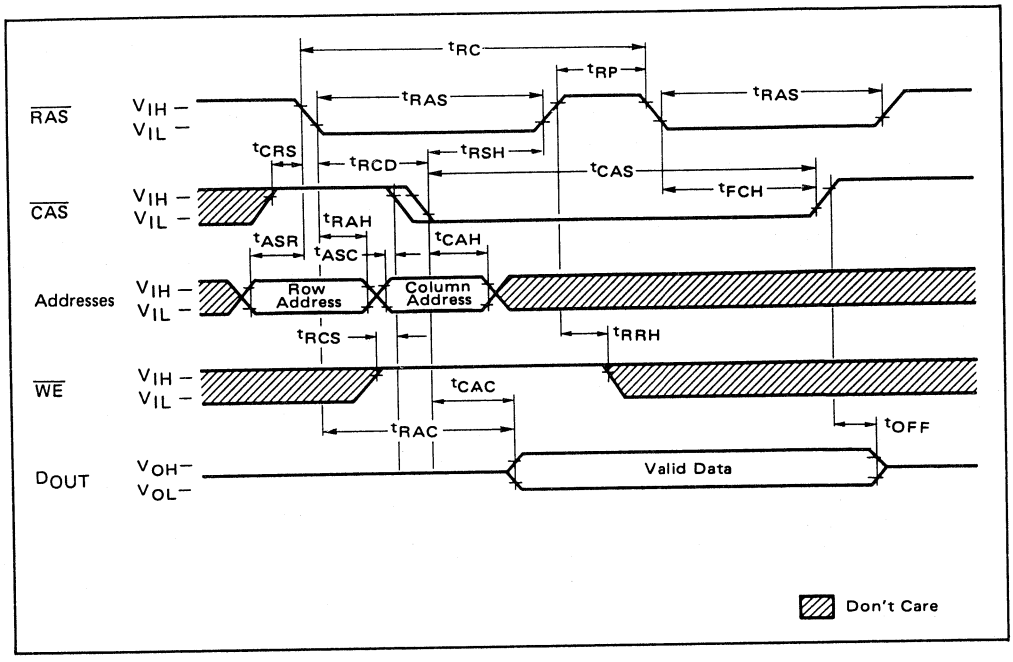
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2304 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2304 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSC2304 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSC2304 can commit better memory system through-put during operations in an interleaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSC2304. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input address must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

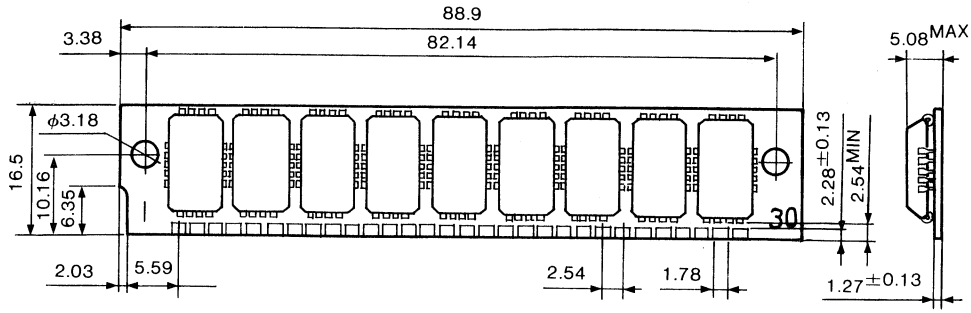
$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

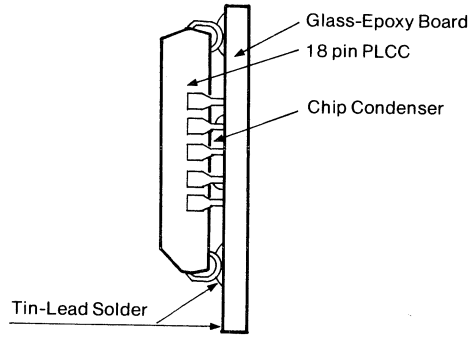
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSC2304 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSC2304 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

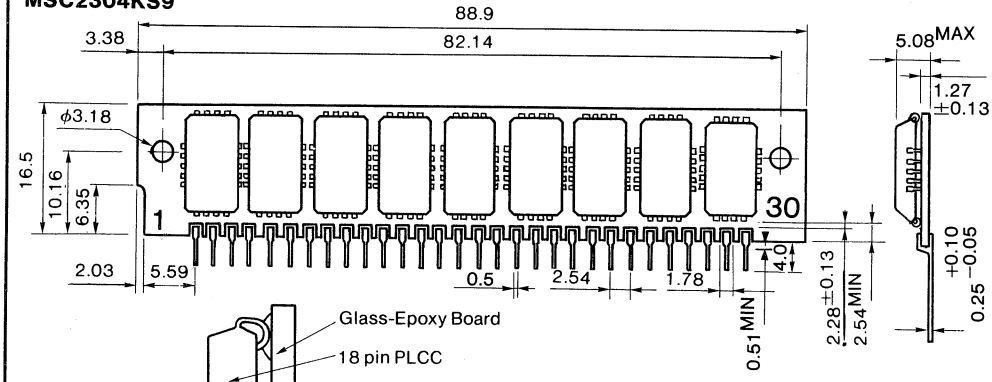
MSC2304YS9

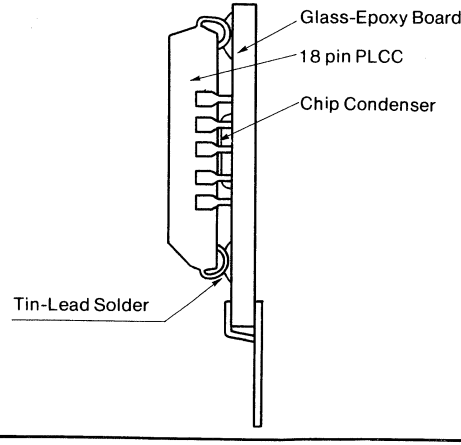




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

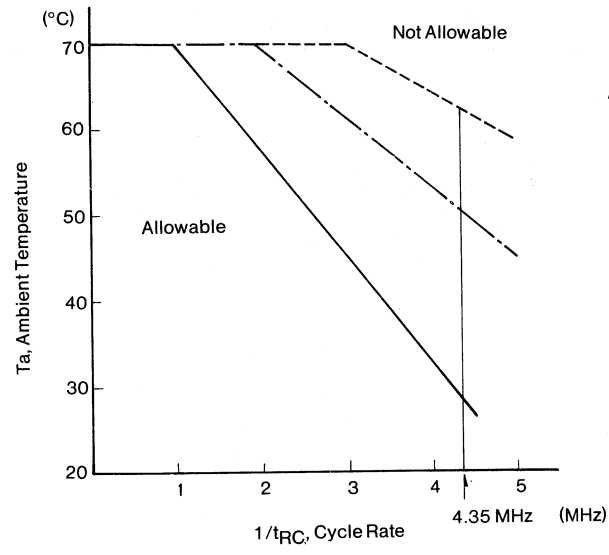
MSC2304KS9





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304YS9/KS9 (SIP/SIM) DERATING CURVE



MSC2307YS9/KS9

262,144 BY 9 BIT DYNAMIC RAM MODULE <Nibble Mode Type>

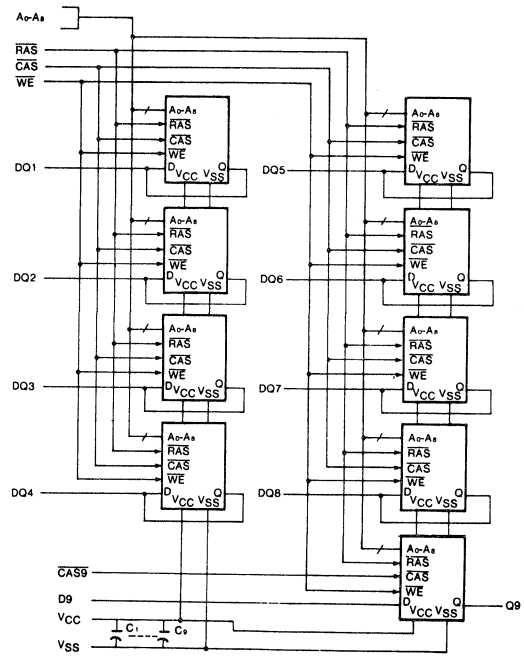
GENERAL DESCRIPTION

The Oki MSC2307YS9/KS9 is a fully decoded, 262,144 words x 9 bit NMOS dynamic random access memory composed of nine 256K DRAMs in plastic leaded chip carrier (MSM41257AJS). The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2307YS9/KS9 are quite same as the original MSM41257AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

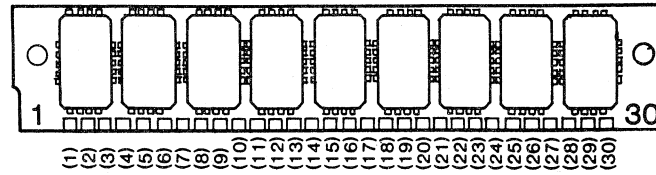
- 262,144 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
  100ns max. (MSC2307-10YS9/KS9)
  120ns max. (MSC2307-12YS9/KS9)
  150ns max. (MSC2307-15YS9/KS9)
- Low Power Dissipation;
  2970mW max. (MSC2307-10YS9/KS9)
  2723mW max. (MSC2307-12YS9/KS9)
  2475mW max. (MSC2307-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability

FUNCTIONAL BLOCK DIAGRAM

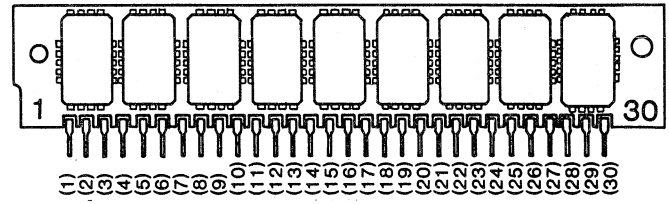


PIN ASSIGNMENT

MSC2307YS9



MSC2307KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; t_{RC} = min.)	I_{CC1}		540		495		450	mA
Standby Current Power supply current (RAS = CAS = V_{IH})	I_{CC2}		45		45		45	mA
Refresh Current 1 Average power supply current (RAS cycling, CAS = V_{IH}; t_{RC} = min.)	I_{CC3}		495		450		405	mA
Page Mode Current* Average power supply current (RAS = V_{IL}; CAS cycling; t_{PC} = min.)	I_{CC4}		360		315		270	mA
Refresh Current 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		495		450		405	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−90	90	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSC2307-10 YS9/KS9		MSC2307-12 YS9/KS9		MSC2307-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		

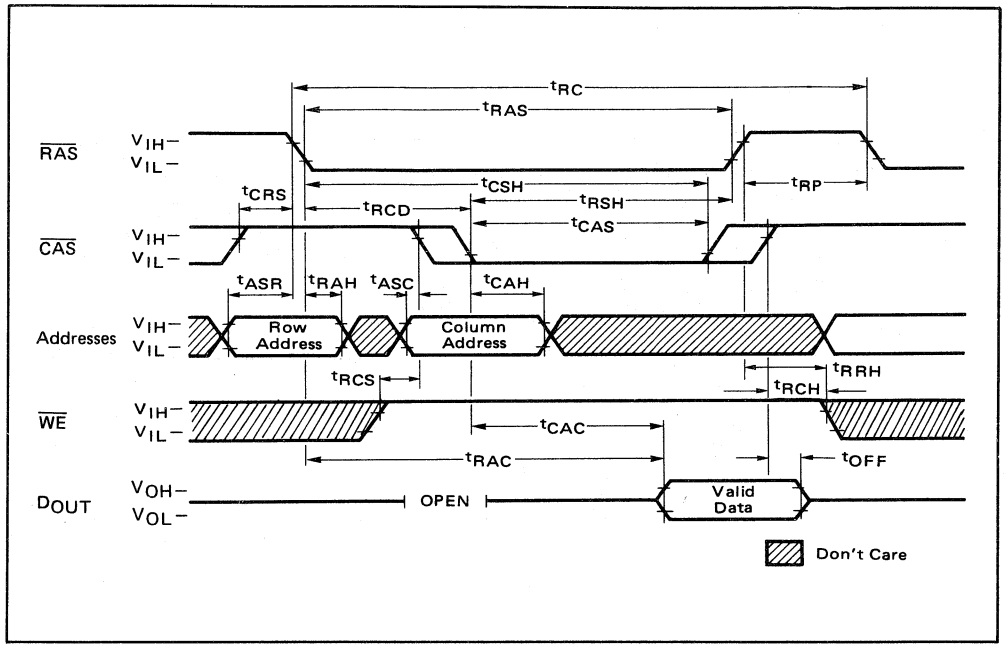
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSC2307-10 YS9/KS9		MSC2307-12 YS9/KS9		MSC2307-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Nibble mode read/write cycle time	t_{NC}	ns	60		70		80		8
Nibble mode access time	t_{NCAC}	ns		25		30		35	8
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	25		30		35		8
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	ns	25		30		35		8
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	ns	25		30		35		8
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	ns	45		50		60		8
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	25		30		35		8

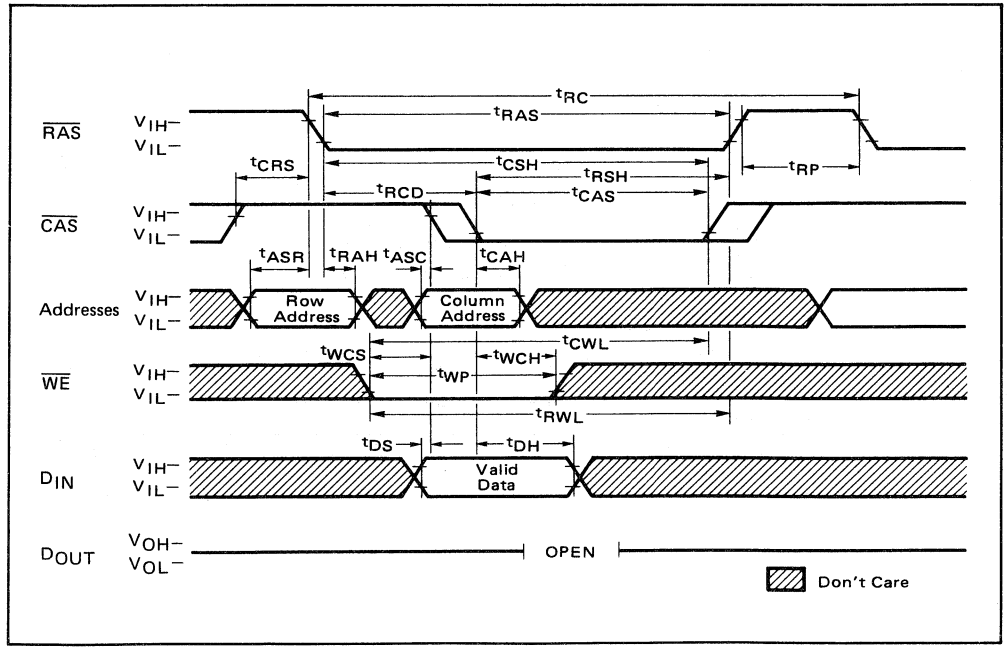
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Nibble mode cycle.

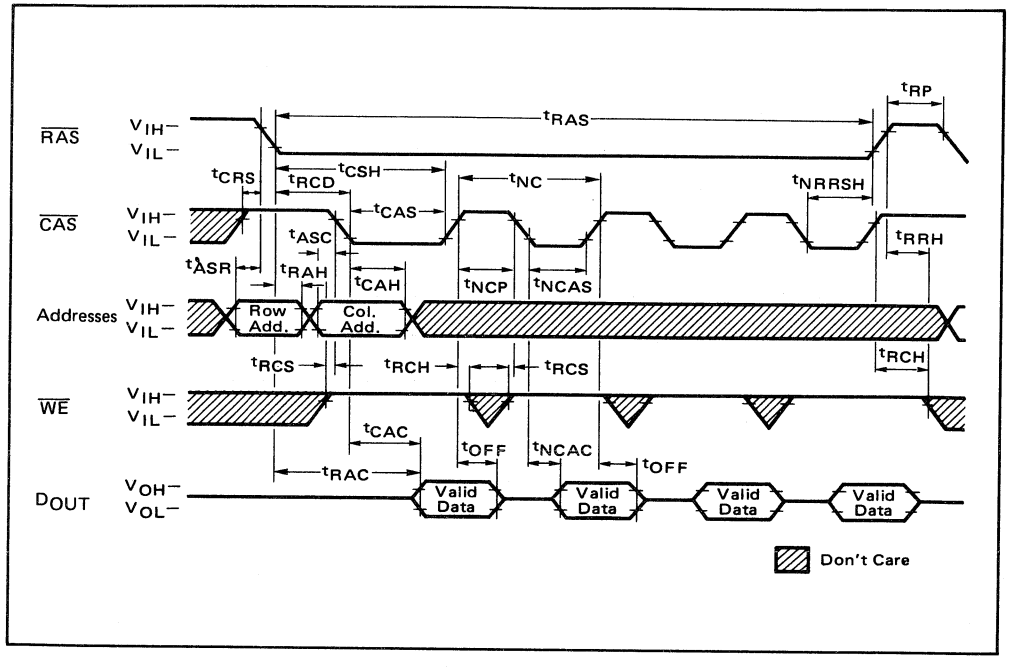
READ CYCLE



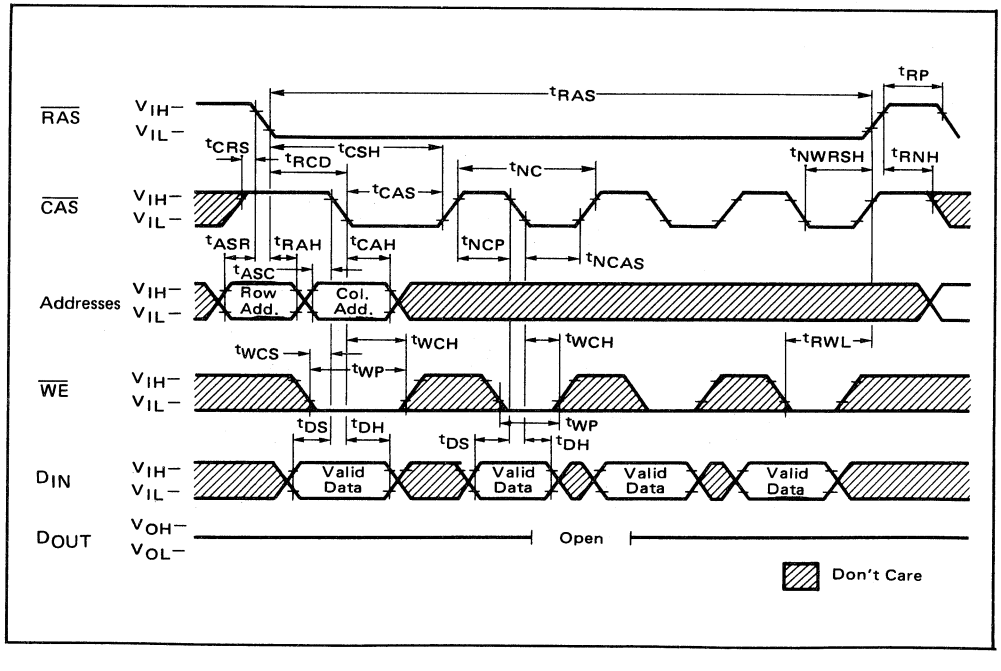
WRITE CYCLE



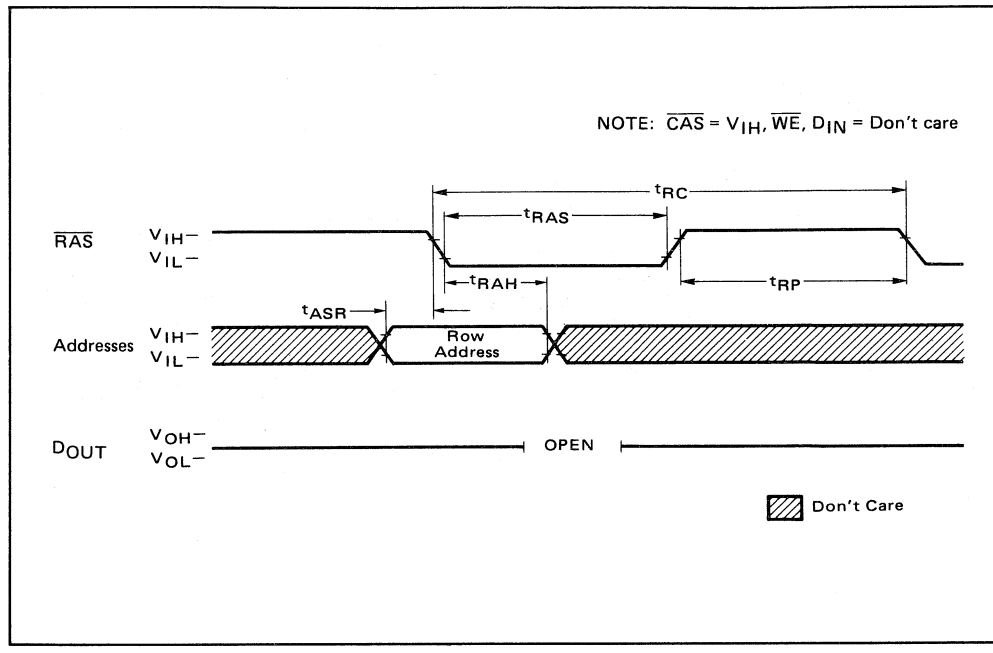
NIBBLE MODE READ CYCLE



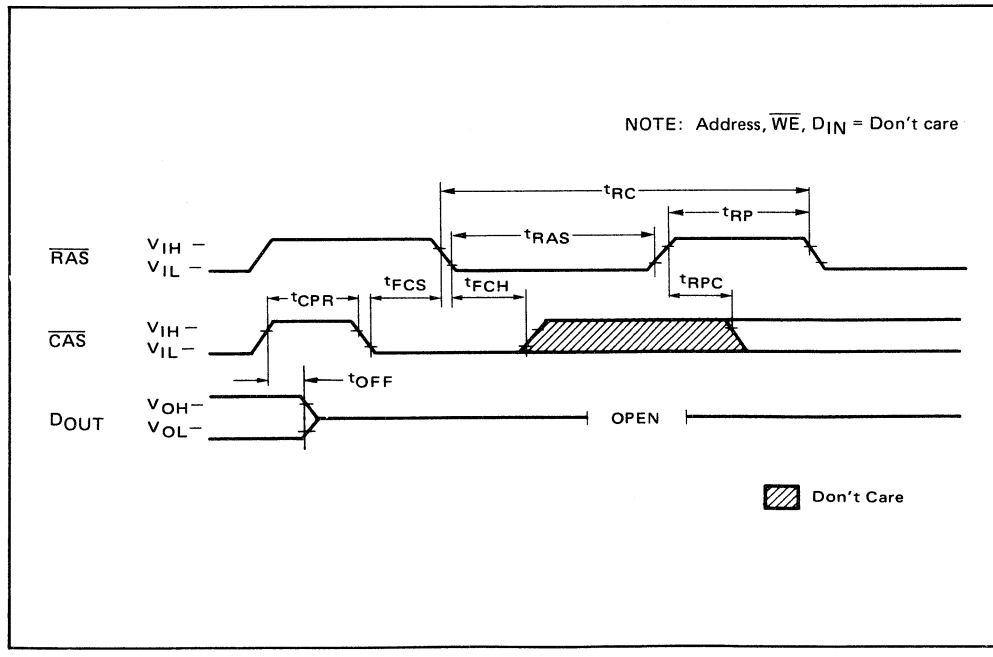
NIBBLE MODE WRITE CYCLE



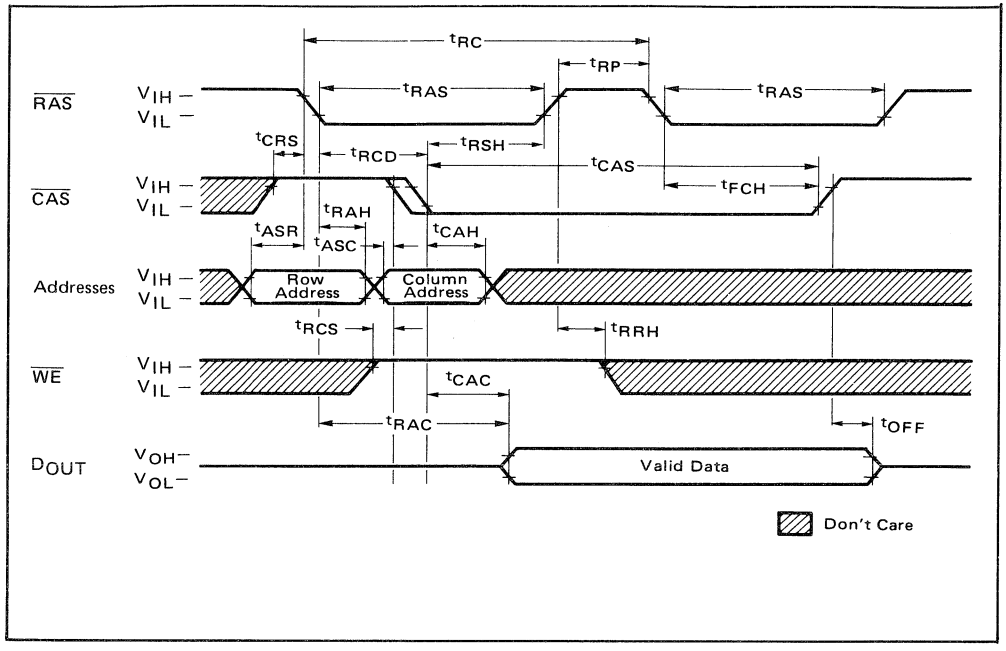
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2307 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2307 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSC2307 has the minimal hold time of Address (t_{CAH}), WE (t_{WCH}) and D_{IN} (t_{DH}). And the MSC2307 can commit better memory system through-put during operations in an interleaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSC2307. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe (RAS). Then nine column address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the WE input. A logic "high" on WE dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2307 during a write. The last falling edge of WE or CAS is a strobe for the Data in (D_{IN}) register. In a write cycle, if WE is brought low (write mode) before CAS, D_{IN} is strobed by CAS, and the set-up and hold times are referenced to CAS.

Data Input:

Data is written into the MSM41257A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode:

Nibble mode allows high speed serial read, write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8 RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling CAS causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	... input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	generated internally sequence repeats
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

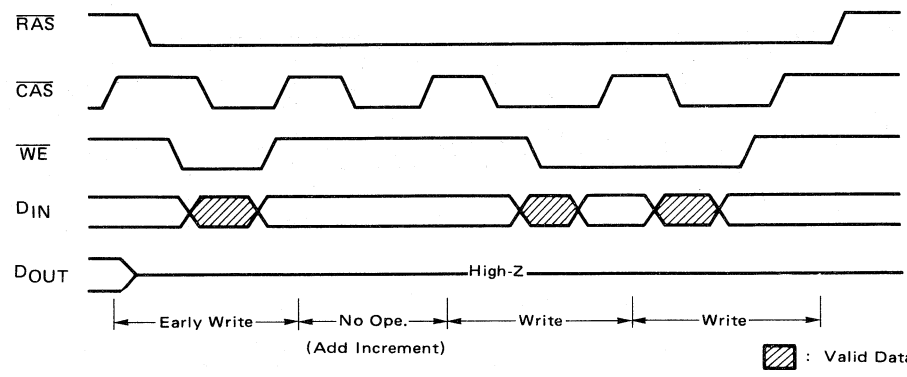
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSC2307 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

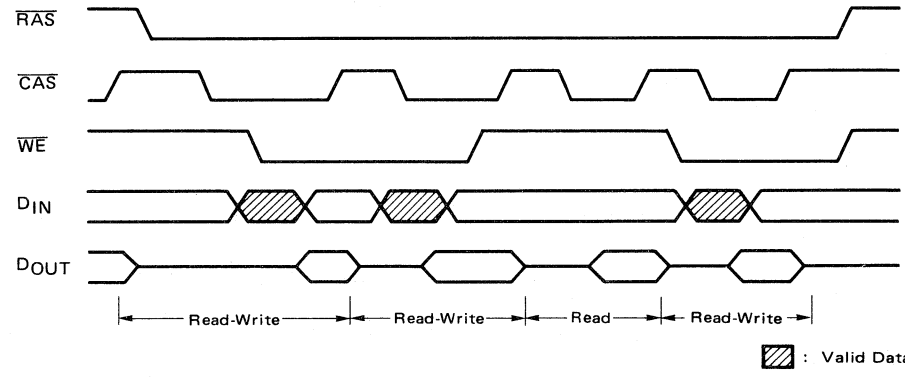
Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSC2307 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

NIBBLE MODE

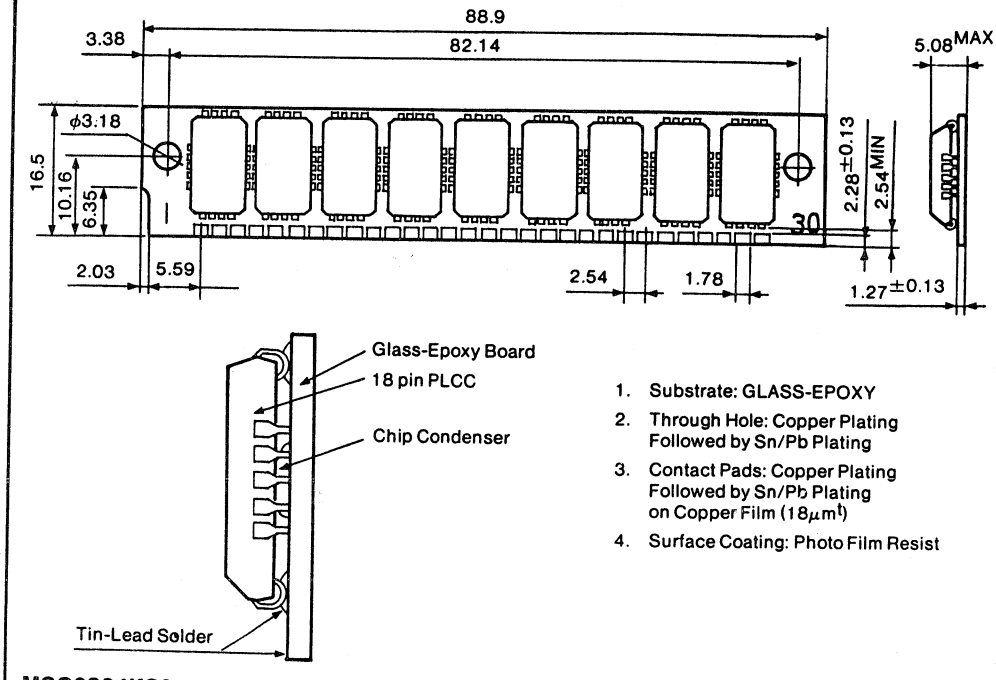
1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

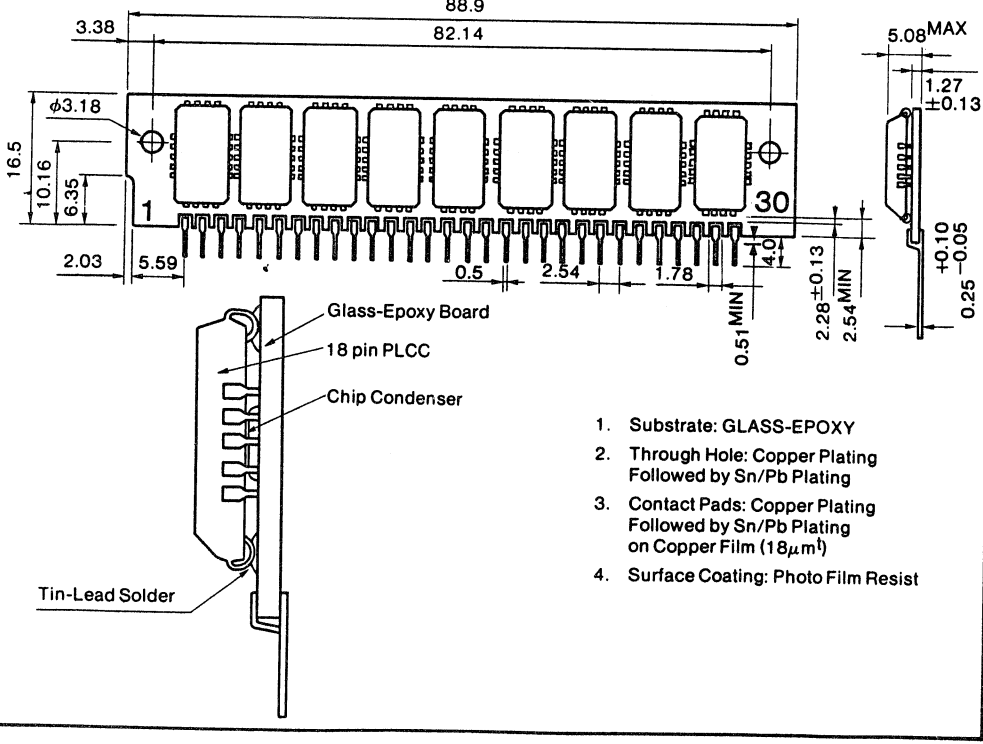


MSC2304YS9



1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304KS9



1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

OKI semiconductor

MSC2305YS18A

524,288 BY 9 BIT DYNAMIC RAM MODULE < Page Mode Type >

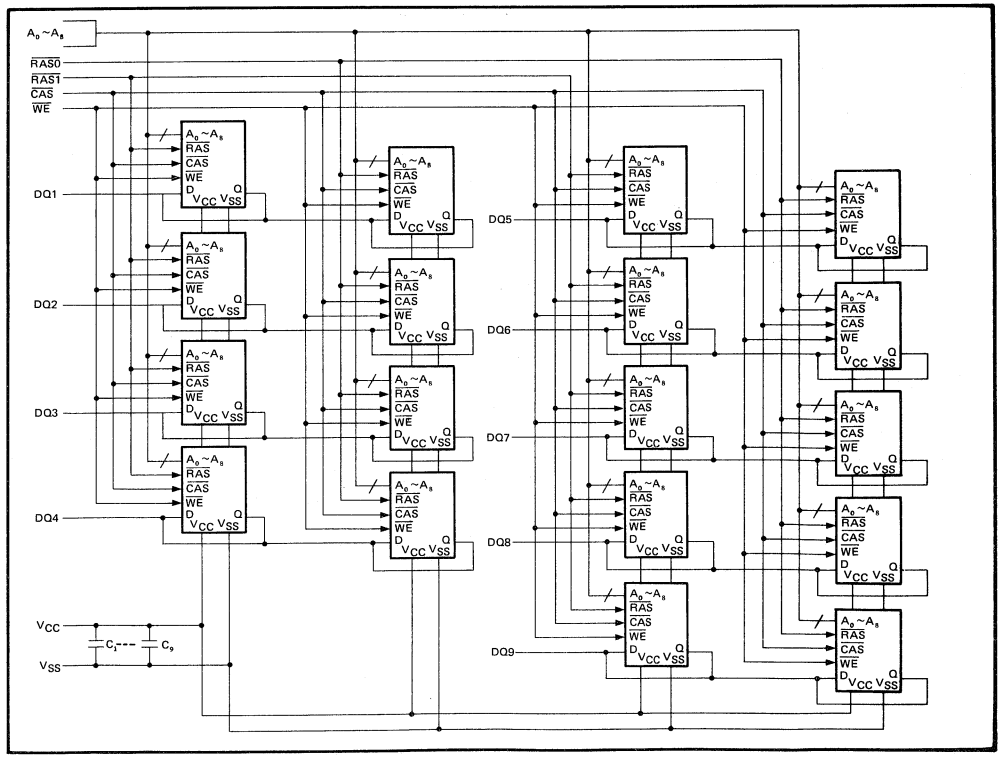
GENERAL DESCRIPTION

The Oki MSC2305YS18A is a fully decoded, 524,288 words × 9 bit NMOS dynamic random access memory composed of eighteen 256K DRAMs in plastic leaded chip carrier (MSM41256AJS). The mounting of eighteen PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2305YS18A are quite same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

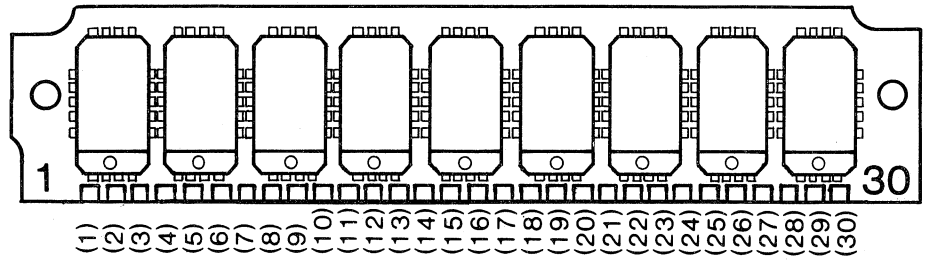
- 524,288 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines
- Row Access Time;
  - 100ns max. (MSC2305-10YS18A)
  - 120ns max. (MSC2305-12YS18A)
  - 150ns max. (MSC2305-15YS18A)
- Low Power Dissipation;
  - 2970mW max. (MSC2305-10YS18A)
  - 2723mW max. (MSC2305-12YS18A)
  - 2475mW max. (MSC2305-15YS18A)
- Operating Temperature ... 0°C to 70°C
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT

MSC2305YS18A



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	$\overline{VSS}$
7	A2	17	A8	27	$\overline{RAS0}$
8	A3	18	NC	28	NC
9	VSS	19	$\overline{RAS1}$	29	DQ9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	18	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; t_{RC}=min.)	I_{CC1}		540		495		450	mA
Standby Current Power supply current (RAS=CAS=V_{IH})	I_{CC2}		90		90		90	mA
Refresh Current-One Module Selected Average power supply current (RAS cycling, CAS=V_{IH}; t_{RC}=min.)	I_{CC3}		495		450		405	mA
Page Mode Current* Average power supply current (RAS=V_{IL}, CAS cycling; t_{PC}=min.)	I_{CC4}		360		315		270	mA
Refresh Current-Two Module Selected Average power supply current (RAS cycling CAS=V_{IH}, t_{RC}=min.)	I_{CC5}		900		810		720	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test= 0V)	I_{LI}	−90	90	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−20	20	−20	20	−20	20	μA
Output Levels Output high voltage (I_{OH}=−5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL}=4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	60	140	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{WE}$)	C_{IN2}	50	140	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	12	20	pF
Input Capacitance ($\overline{CAS}$)	C_{IN3}	85	170	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSC2305-10 YS18A		MSC2305-12 YS18A		MSC2305-15 YS18A		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns	100			120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns	50			60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10,000	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10,000	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		

AC CHARACTERISTICS (CONT.)

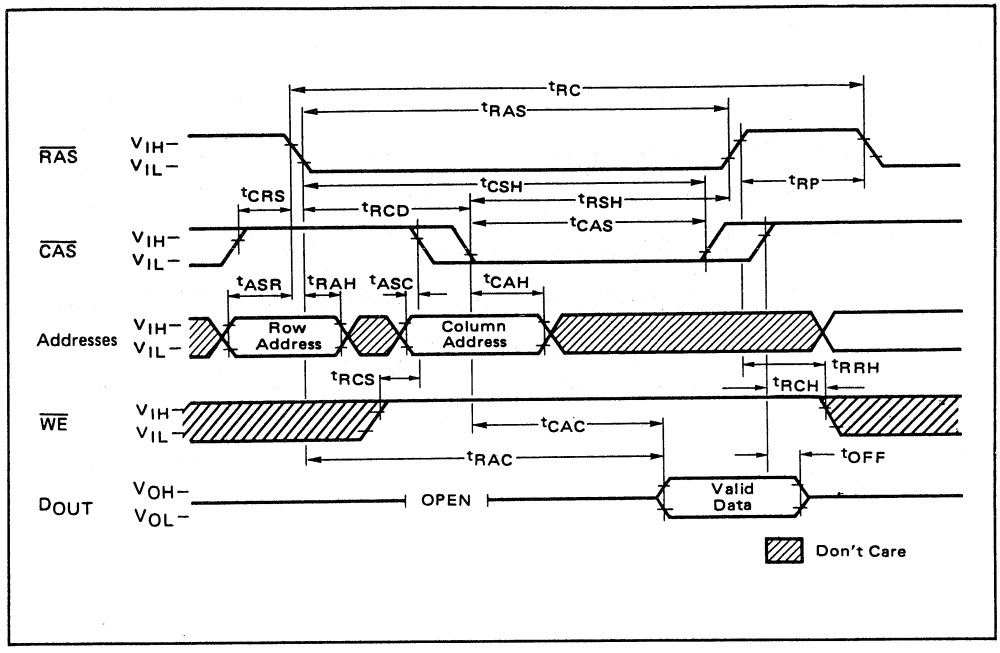
Parameter	Symbol	Units	MSC2305-10 YS18A		MSC2305-12 YS18A		MSC2305-15 YS18A		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		8

AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

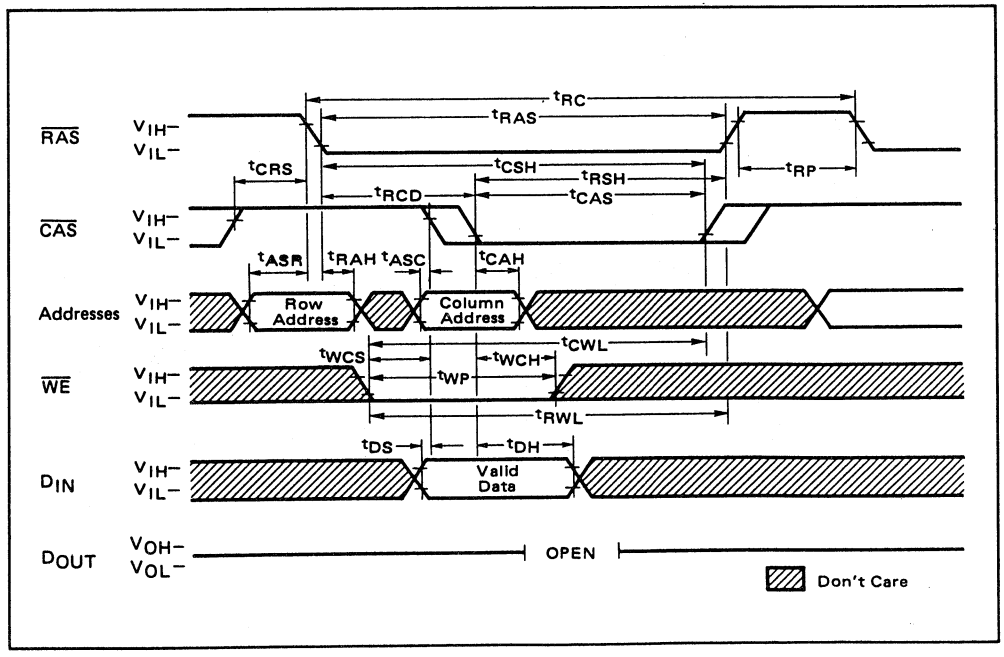
Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		8

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) Page mode cycle.

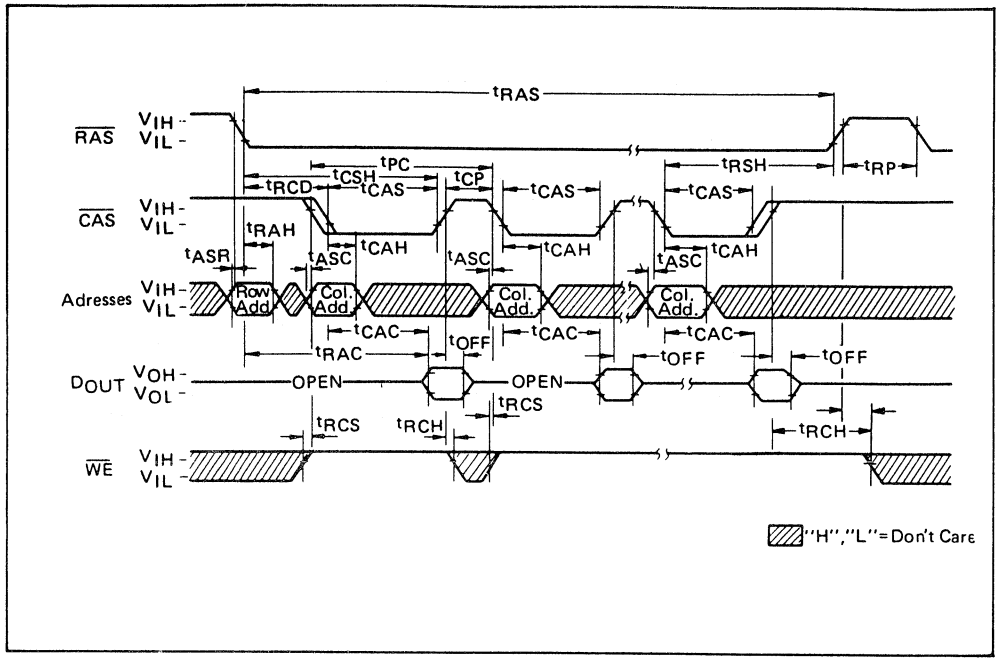
READ CYCLE



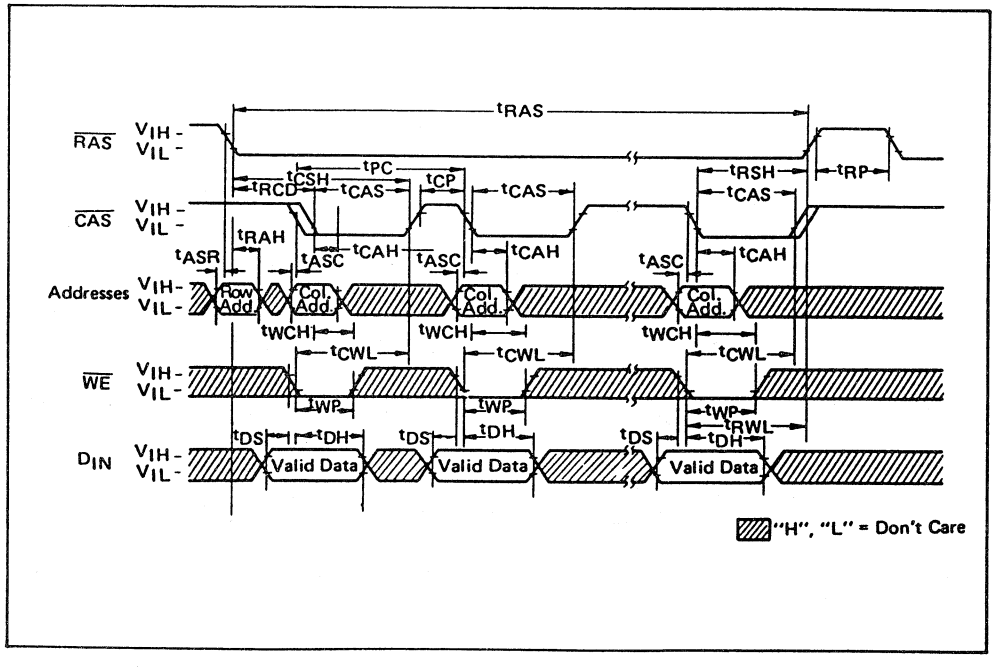
WRITE CYCLE



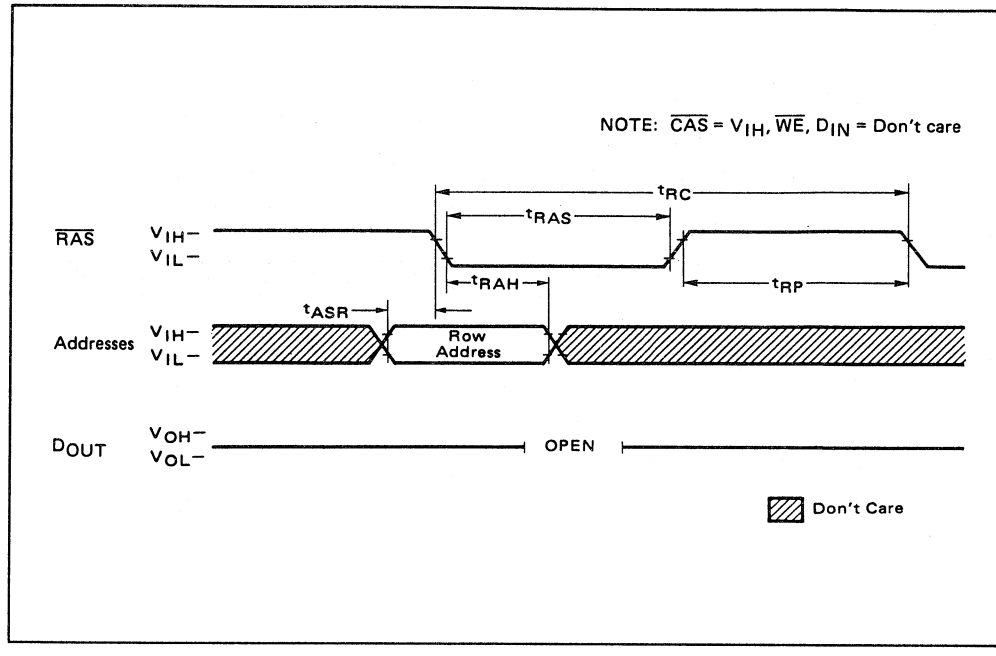
PAGE MODE READ CYCLE



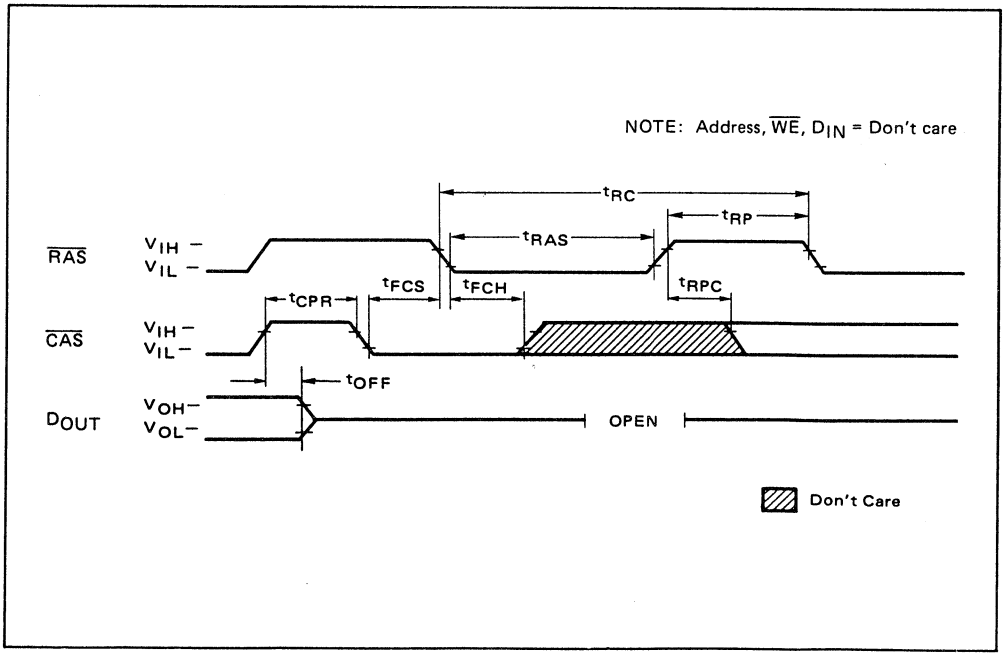
PAGE MODE WRITE CYCLE



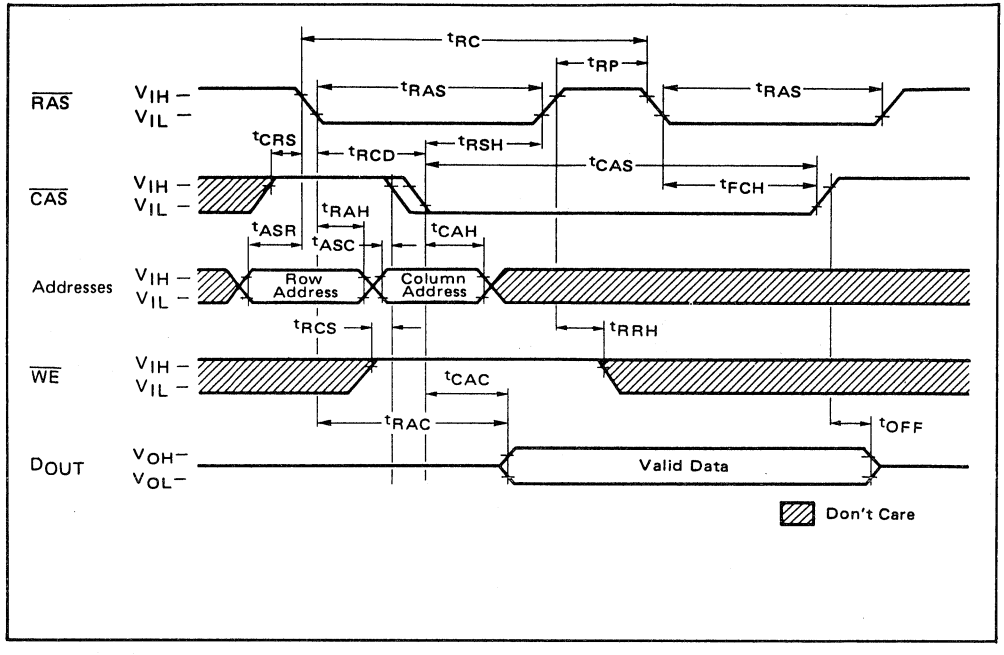
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2305 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2305 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSC2305 has the minimal hold time of Address (t_{CAH}), WE (t_{WCH}) and D_{IN} (t_{CH}). And the MSC2305 can commit better memory system through-put during operations in an interleaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 524,288 storage cell location within the MSC2305. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe (RAS). Then nine column address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2305 during a write. The last falling edge of WE or CAS is a strobe for the Data in (D_{IN}) register. In a write cycle, if WE is brought "low" (write mode) before CAS, D_{IN} is strobed by CAS, and the set-up and hold times are referenced to CAS.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

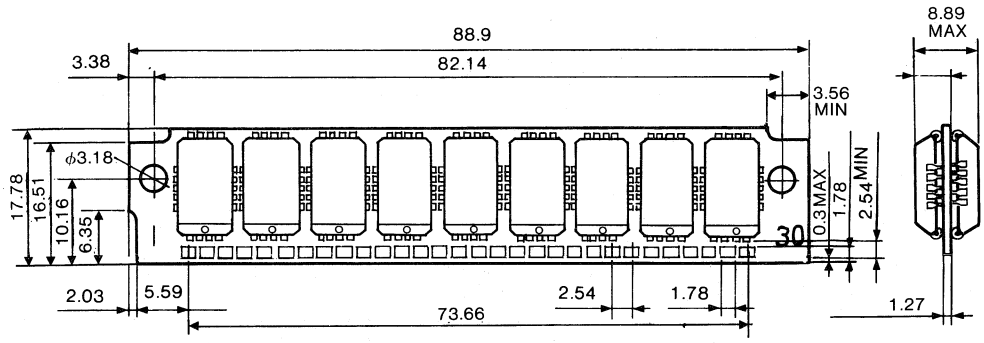
$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

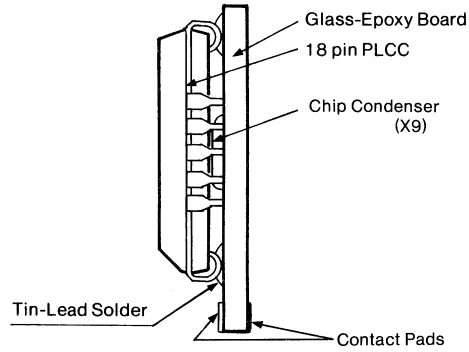
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41256A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

MSC2305YS18A





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2310YS9/KS9

1,048,576 BY 9 BIT DYNAMIC RAM MODULE

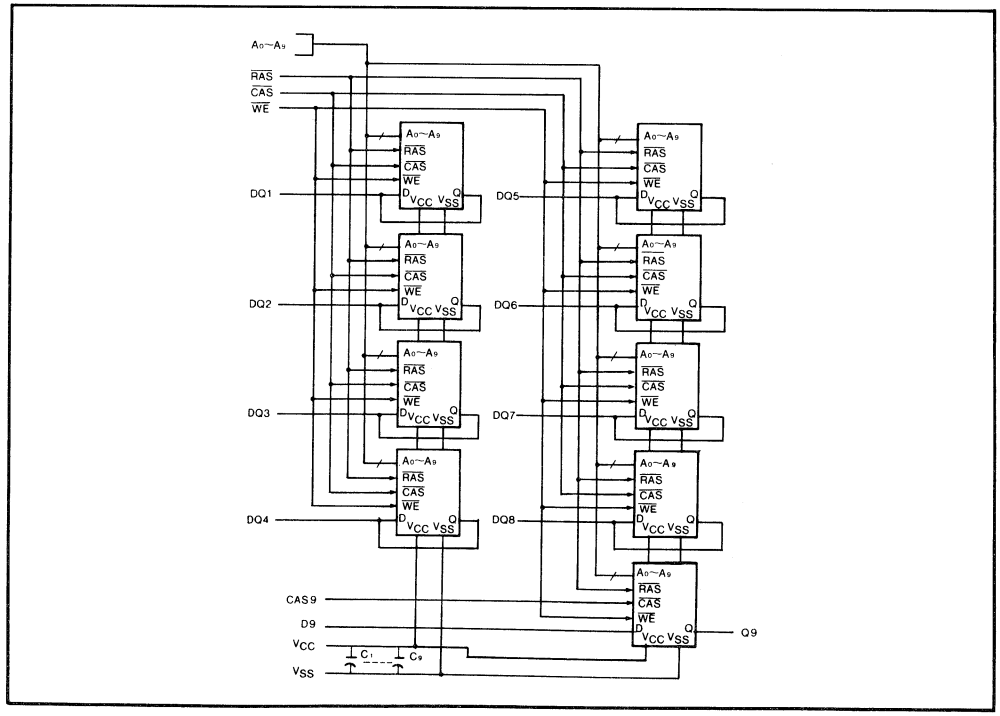
GENERAL DESCRIPTION

The Oki MSC2310YS9/KS9 is a fully decoded, 1,048,576 words × 9 bit NMOS dynamic random access memory composed of nine 1 Mb DRAMs in SOJ (MSM411000JS). The mounting of nine SOJs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2310YS9/KS9 are quite same as the original MSM411000JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

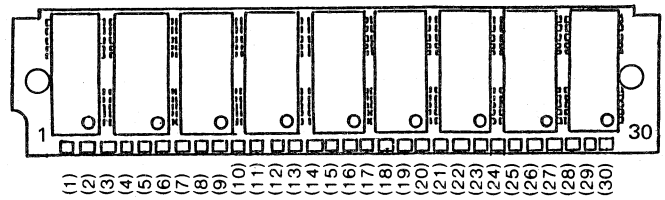
- 1,048,576 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Linens
- Access Time;
  100ns max. (MSC2310-10YS9/KS9)
  120ns max. (MSC2310-12YS9/KS9)
- Low Power Dissipation;
  3713mW max. (MSC2310-10YS9/KS9)
  3465mW max. (MSC2310-12YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

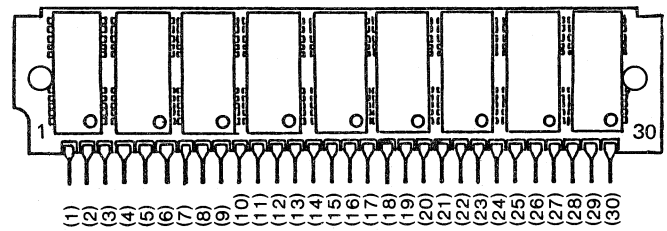


PIN ASSIGNMENT

MSC2310YS9



MSC2310KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		675		630	mA
Standby Current* Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		45		45	mA
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} =min.)	I_{CC3}		585		540	mA
Page Mode Current* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		495		450	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	70	–	85	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	20	–	25	–	ns	

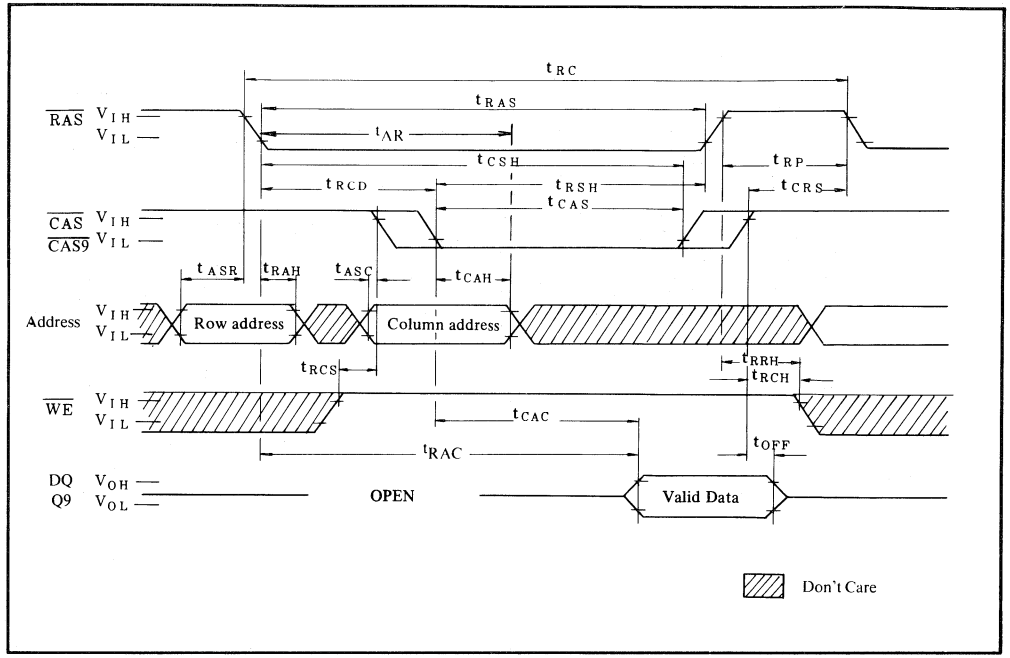
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	70	–	85	–	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	9
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	

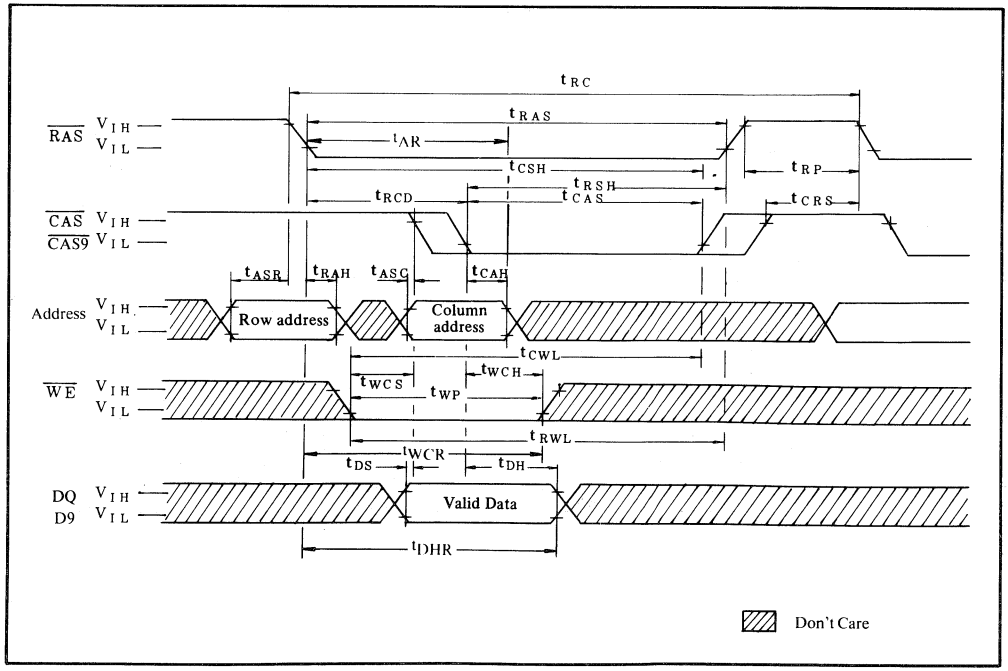
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

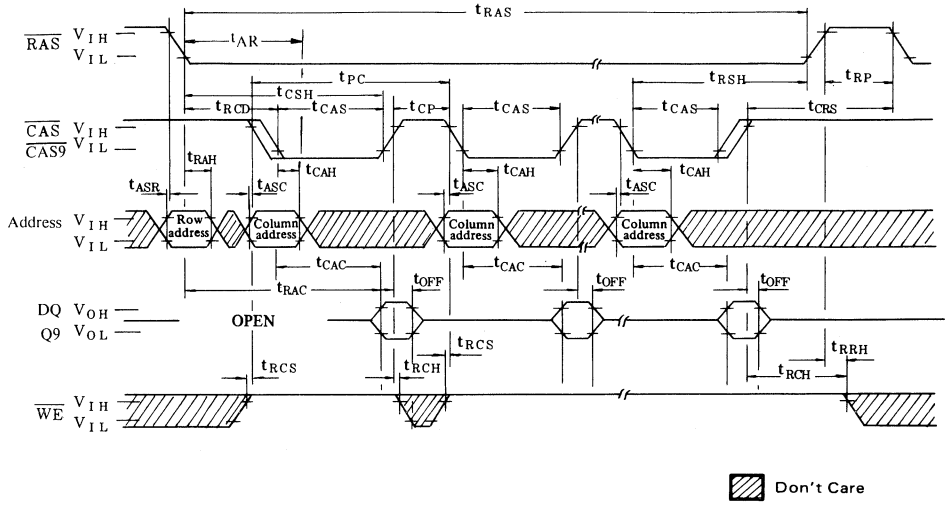
READ CYCLE



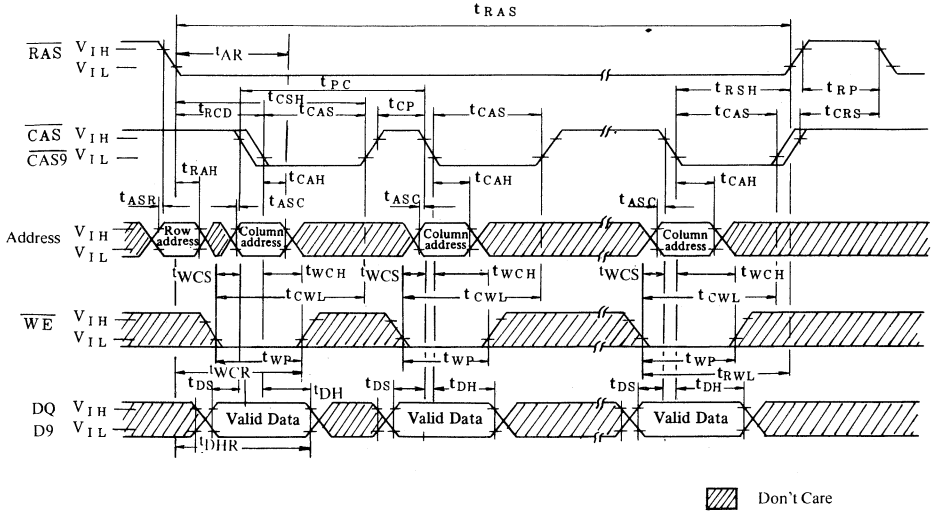
WRITE CYCLE (EARLY WRITE)



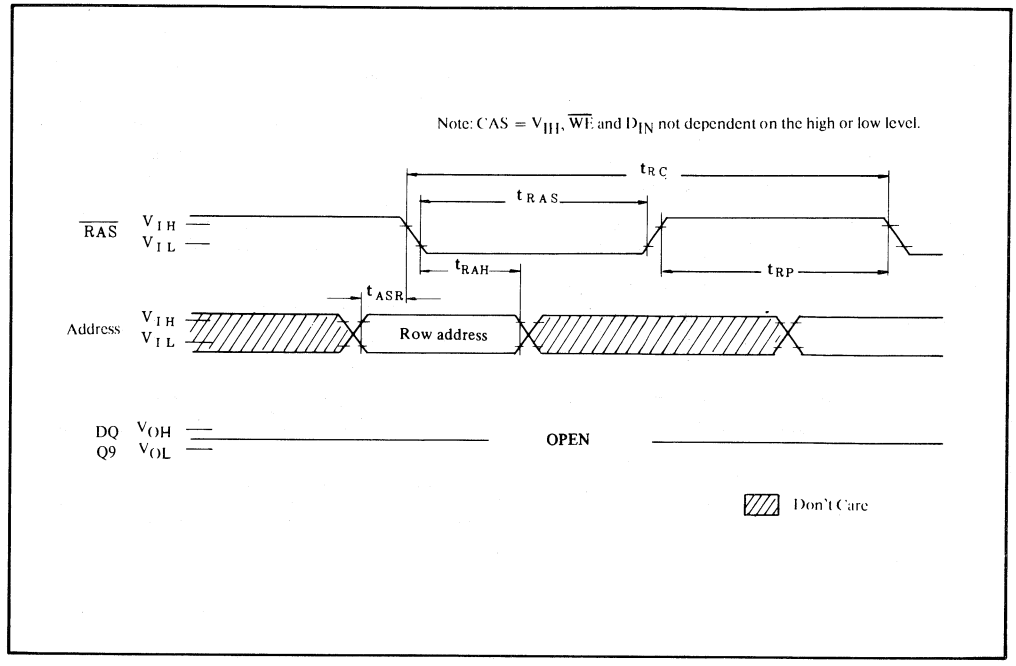
PAGE MODE READ CYCLE



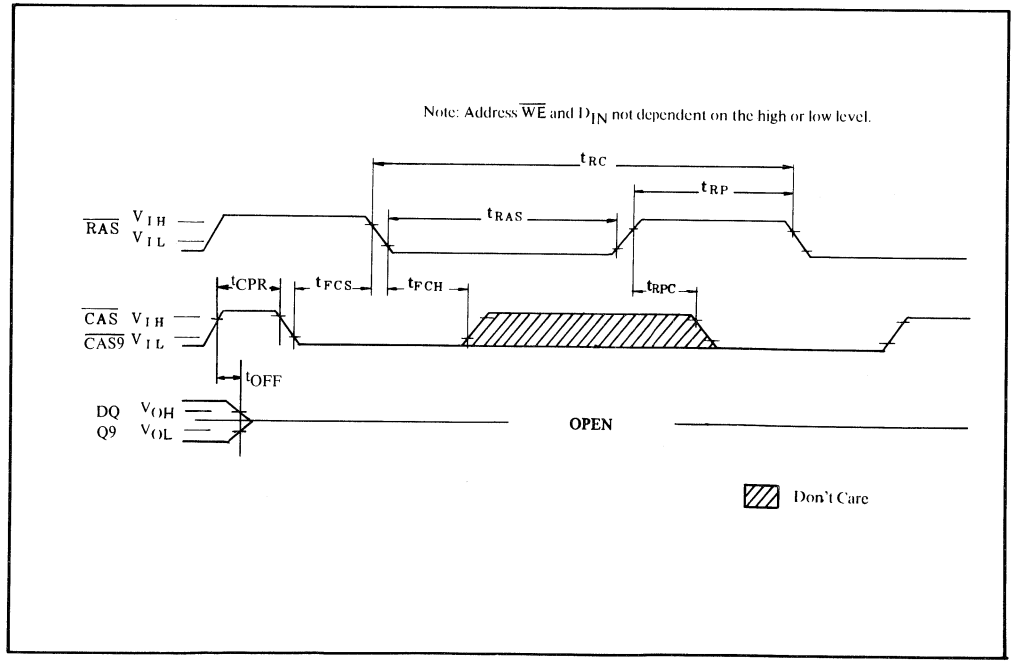
PAGE MODE WRITE CYCLE (EARLY WRITE)



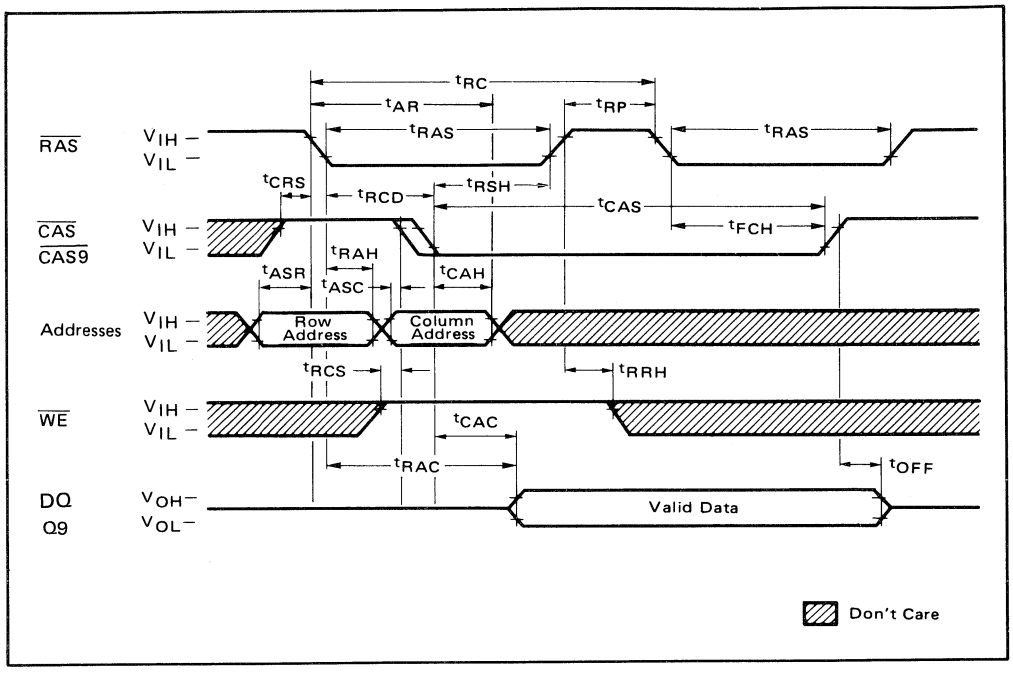
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

20 bits of binary address input are required to decode any one of the 1,048,576 words by 1 bit storage cell locations.

10 row-address bits are set up on address input pins A0 through A9 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 10 column-address bits are set up on pins A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In a write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every 8 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

MSC2311YS8/KS8

1,048,576 BY 8 BIT DYNAMIC RAM MODULE

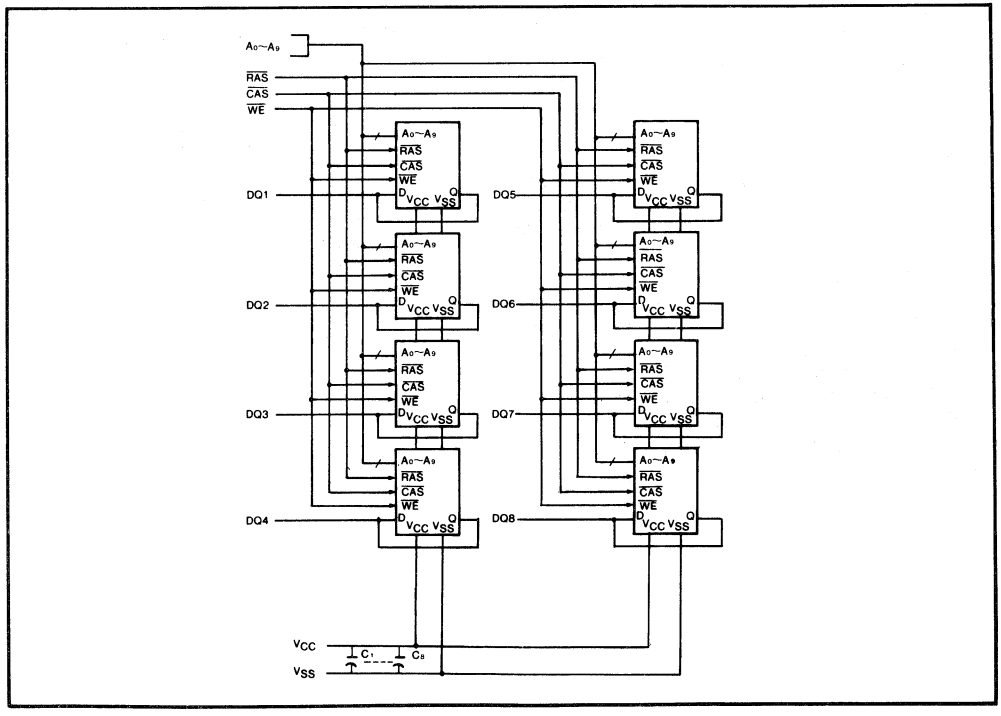
GENERAL DESCRIPTION

The Oki MSC2311YS8/KS8 is a fully decoded, 1,048,576 words × 8 bit NMOS dynamic random access memory composed of nine 1Mb DRAMs in SOJ (MSM411000JS). The mounting of nine SOJs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2311YS8/KS8 are quite same as the original MSM411000JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

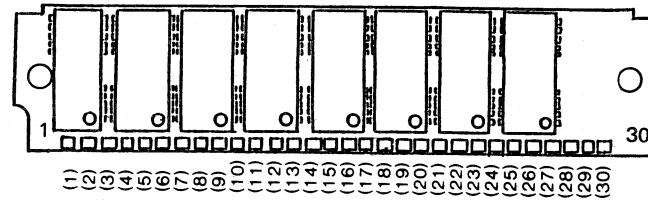
- 1,048,576 word × 8 bit Organization
- Single =5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Linens
- Row Access Time;
  100ns max. (MSC2311-10YS8/KS8)
  120ns max. (MSC2311-12YS8/KS8)
- Low Power Dissipation;
  3300mW max. (MSC2311-10YS8/KS8)
  3080mW max. (MSC2311-12YS8/KS8)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

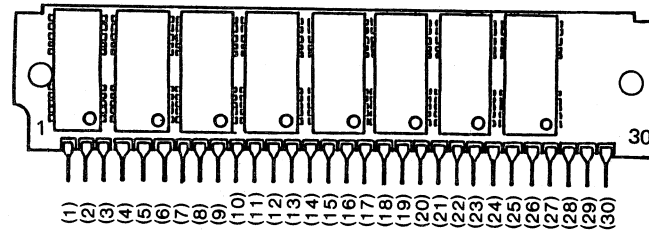


PIN ASSIGNMENT

MSC2311YS8



MSC2311KS8



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	NC
9	VSS	19	NC	29	NC
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2311-10YS8/KS8		MSC2311-12YS8/KS8		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		600		560	mA
Standby Current* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		40		40	mA
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}		520		480	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		440		400	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	37	60	pF
Input Capacitance (RAS, CAS, WE)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSC2311-10YS8/KS8		MSC2311-12YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	70	–	85	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	20	–	25	–	ns	

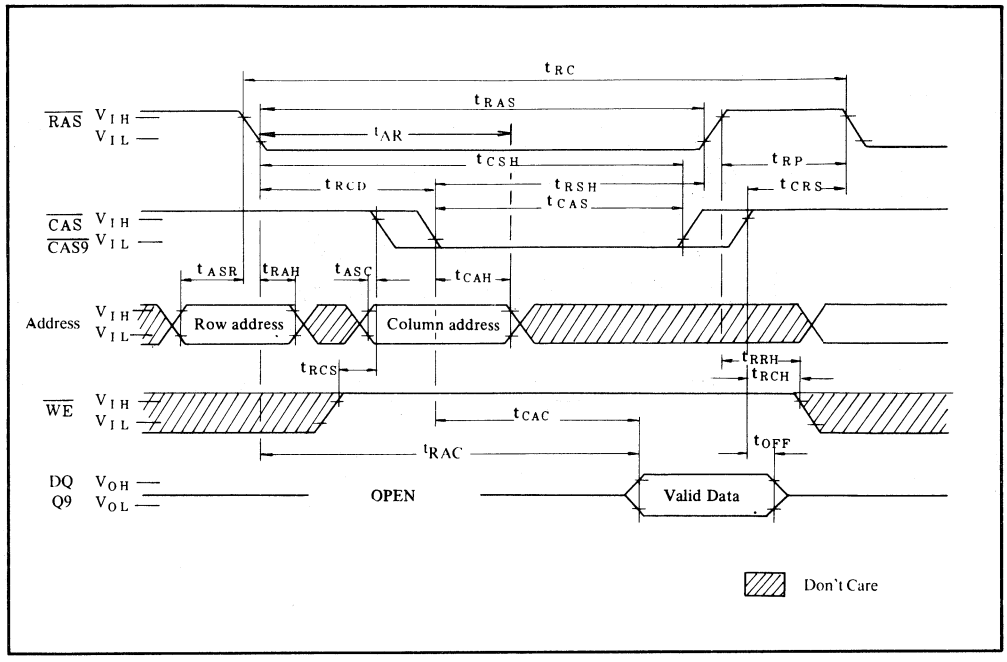
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2311-10YS8/KS8		MSC2311-12YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	70	–	85	–	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	9
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	

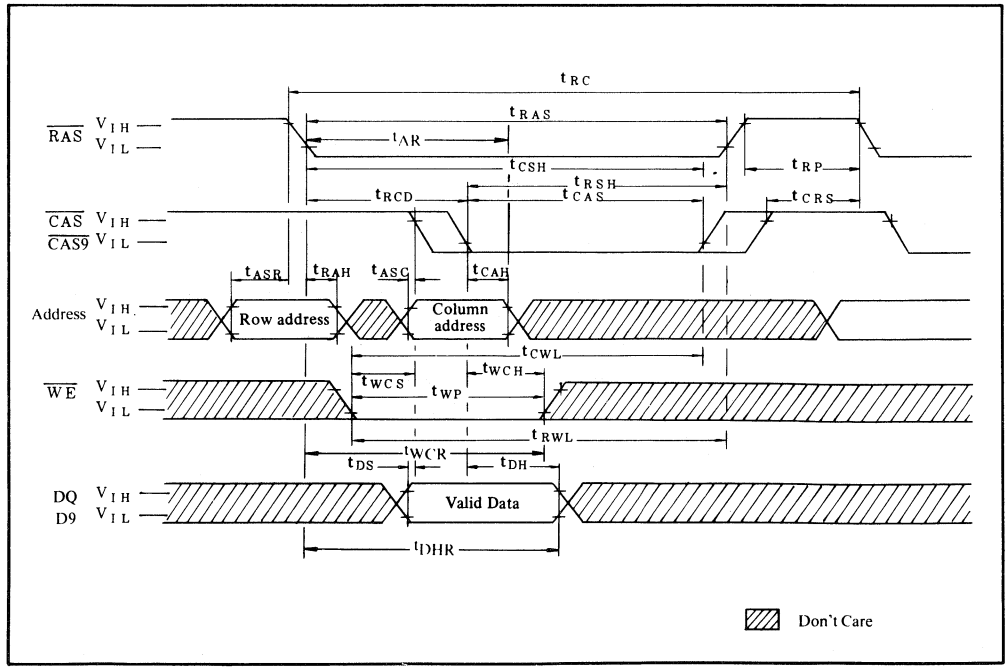
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

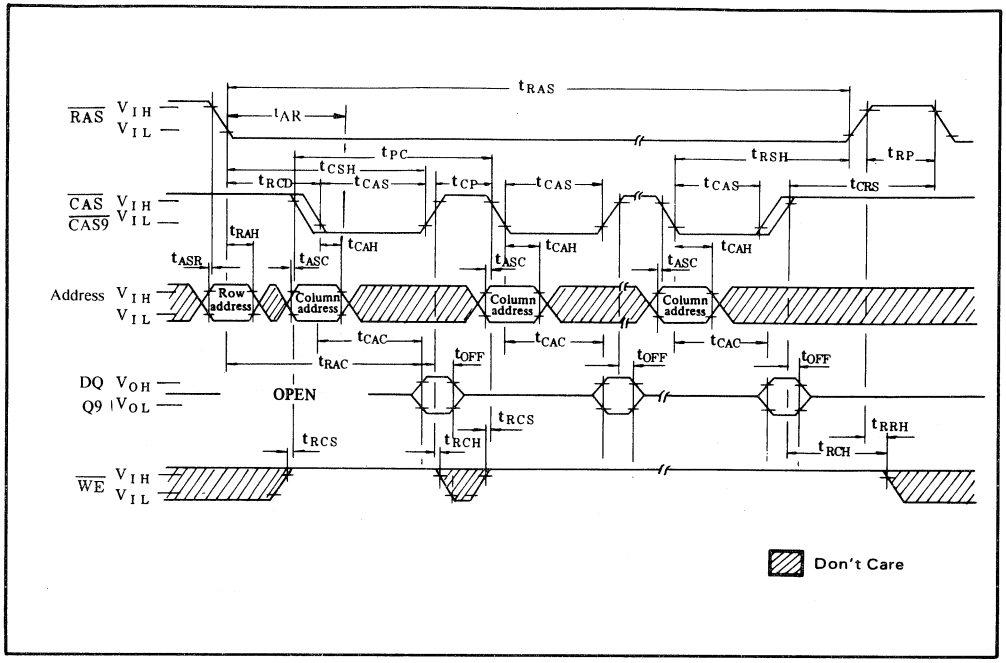
READ CYCLE



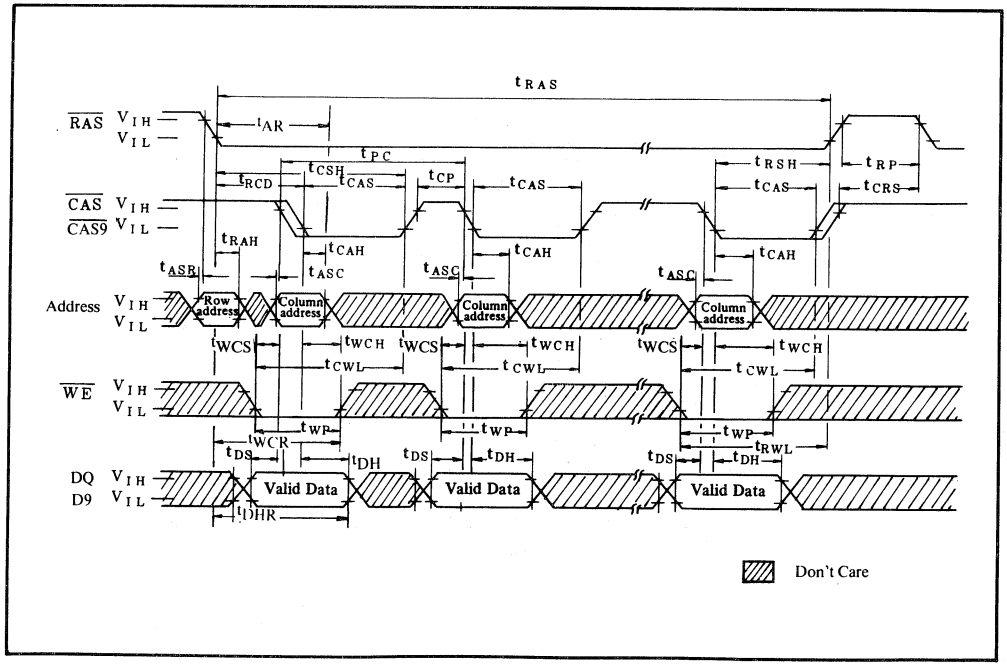
WRITE CYCLE (EARLY WRITE)



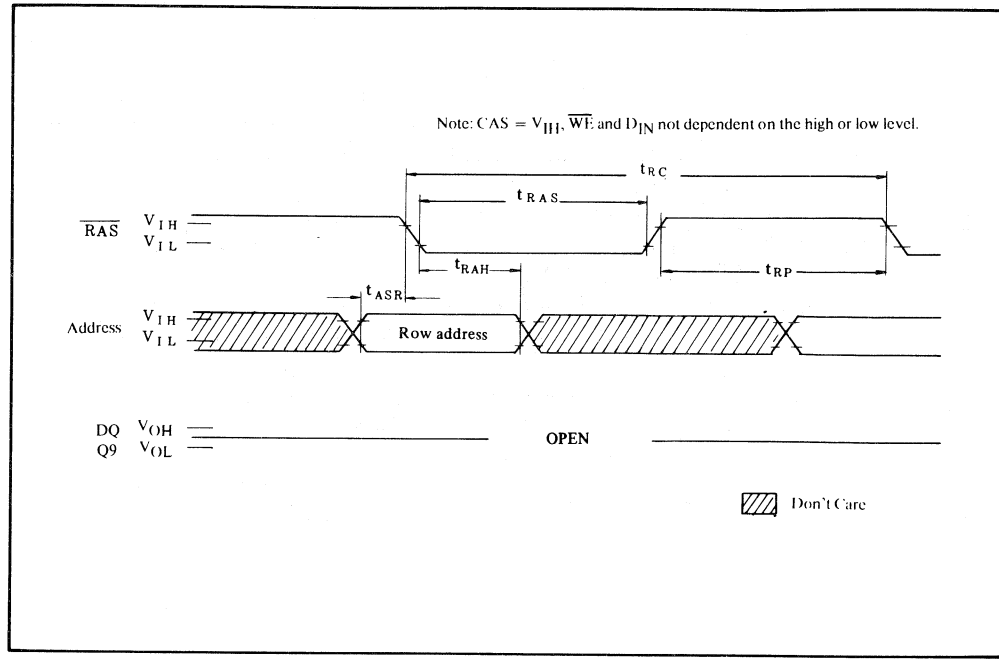
PAGE MODE READ CYCLE



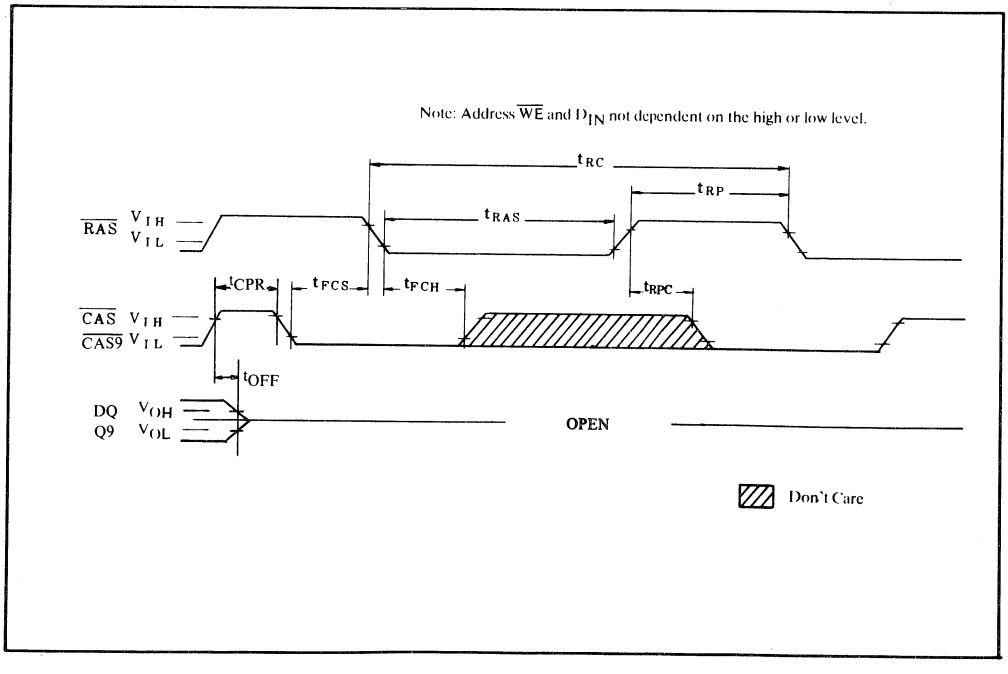
PAGE MODE WRITE CYCLE (EARLY WRITE)



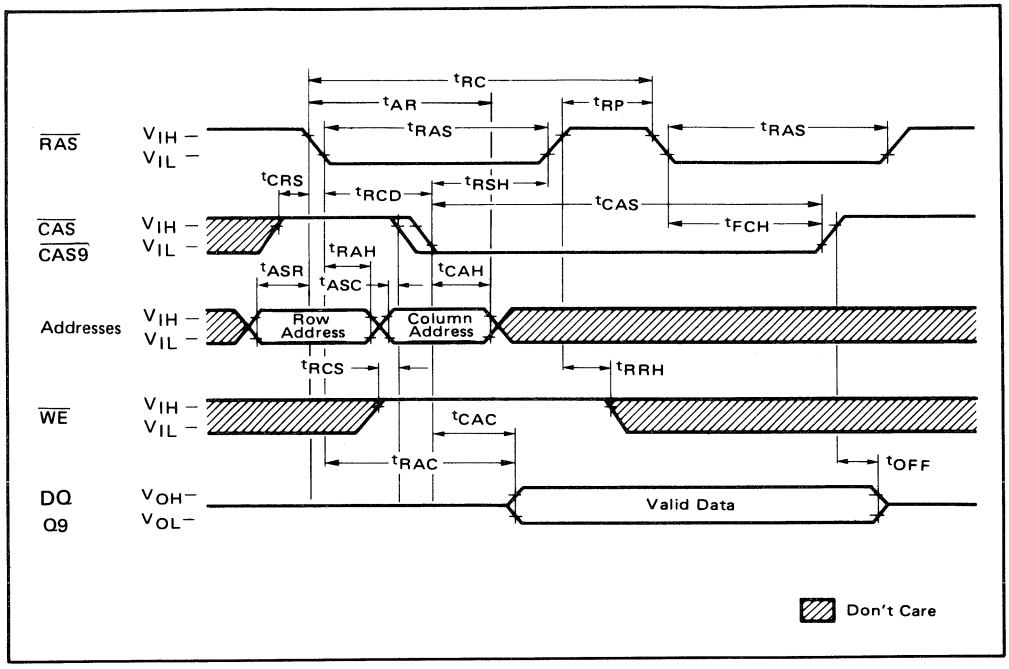
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

20 bits of binary address input are required to decode any one of the 1,048,576 words by 1 bit storage cell locations.

10 row-address bits are set up on address input pins A0 through A9 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 10 column-address bits are set up on pins A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In a write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every 8 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

MOS STATIC RAMS

5 MOS STATIC RAMS

MSM5165RS/JS	8,192-Word x 8-Bit RAM (CMOS)	337
MSM5165LRS/JS	8,192-Word x 8-Bit RAM (CMOS).....	343
MSM5188RS	16,384-Word x 4-Bit RAM (CMOS)	350
MSM51257RS/JS	32,768-Word x 8-Bit RAM (CMOS)	355
MSM51257LRS/JS	32,768-Word x 8-Bit RAM (CMOS)	361

OKI semiconductor

MSM5165RS/JS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

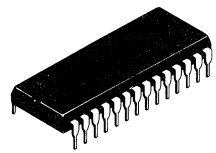
GENERAL DESCRIPTION

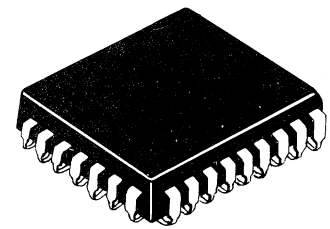
The MSM5165RS/JS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165RS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.
A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CE}_1$, CE_2 and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 5.5 mW MAX
  Operation; 248 mW MAX
- High Speed (Equal Access and Cycle Time)
  120 – 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  64K EPROM (MSM2764)
- 28-pin DIP PKG
- 32-pin PLCC

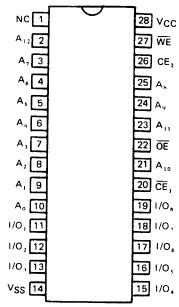
5





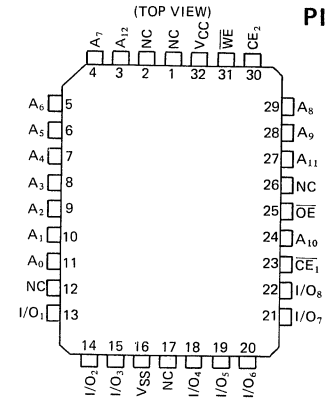
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION



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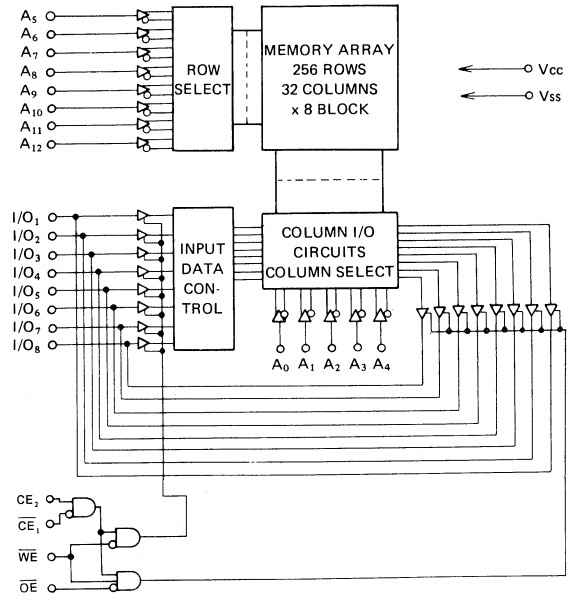
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Wreite	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165 Min.	MSM5165 Typ.	MSM5165 Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		0.02	1	mA	$\overline{CE}_1 \geqq V_{CC} - 0.2V$, $CE_2 \geqq V_{CC} - 0.2V$ V_{IN} = 0 to V_{CC}
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL} t_{cyc} = Min. cycle
Operating Supply Current	I_{CCA}			①	mA	T_{CYC} = Min. cycle
				15		T_{CYC} = 1 μs

① 5165-12 55 mA 5165-15 50 mA 5165-20 45 mA

AC CHARACTERISTICS

Test Condition

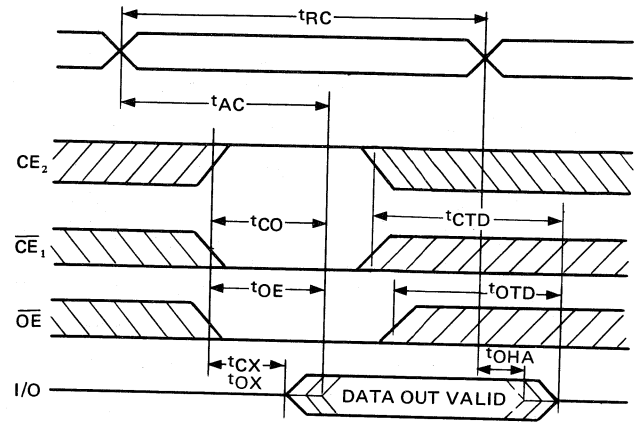
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165-12 Min.	MSM5165-12 Max.	MSM5165-15 Min.	MSM5165-15 Max.	MSM5165-20 Min.	MSM5165-20 Max.	Unit
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Enable Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		70		90	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	40	0	50	0	60	ns
Output 3-state from Chip Deselection	t_{CTD}	0	60	0	70	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low CE_1, a high CE_2, a low OE and a high WE.
2. t_{CX} is specified from CE_1 or CE_2 whichever occurs last.
3. t_{CTD} is specified from CE_1 or CE_2 whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

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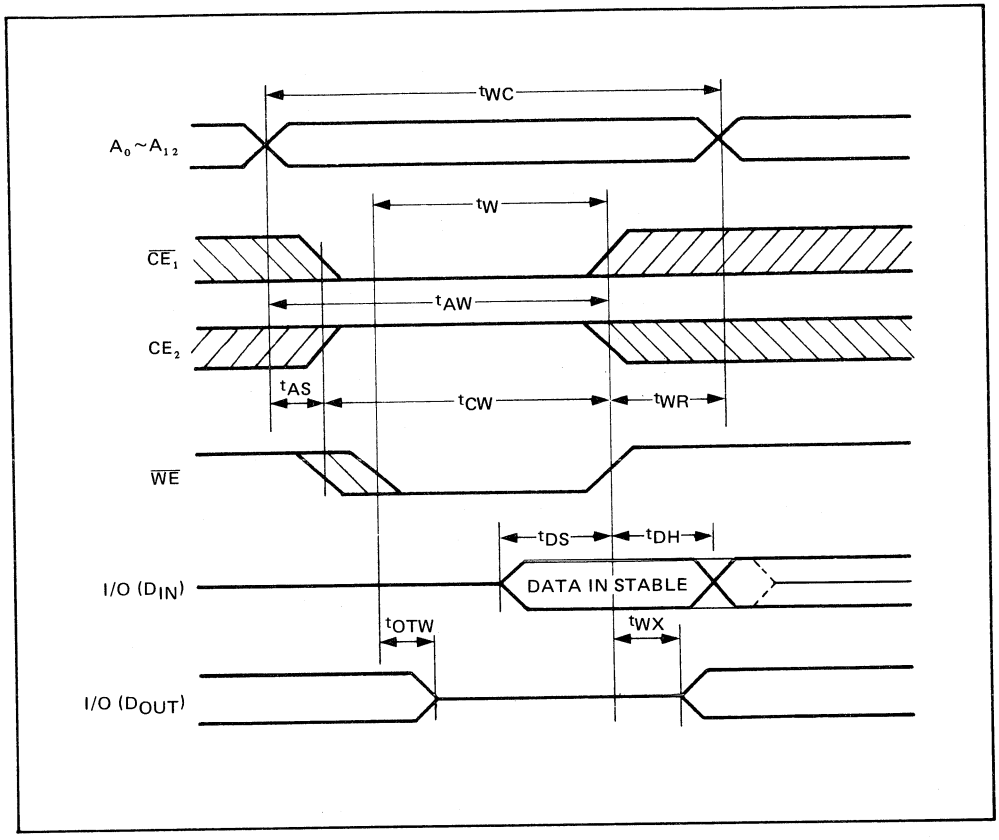
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165-12		MSM5165-15		MSM5165-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	100		120		150		ns
Address Valid to End of Write	t_{AW}	100		120		150		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5165LRS/JS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

GENERAL DESCRIPTION

The MSM5165LRS/JS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165LRS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, CE_1 CE_2 and OE signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 248 mW MAX
- High Speed (Equal Access and Cycle Time)
  120 – 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  64K EPROM (MSM2764)
- 28-pin DIP PKG
- 32-pin PLCC

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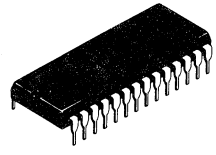
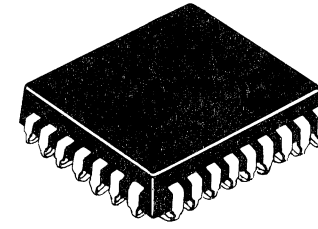
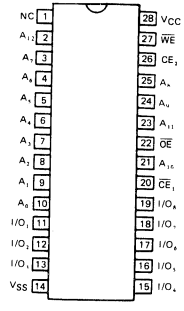




PIN CONFIGURATION

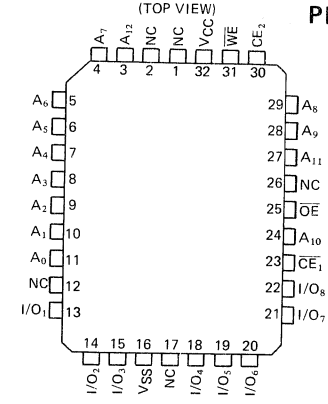
(Top View)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

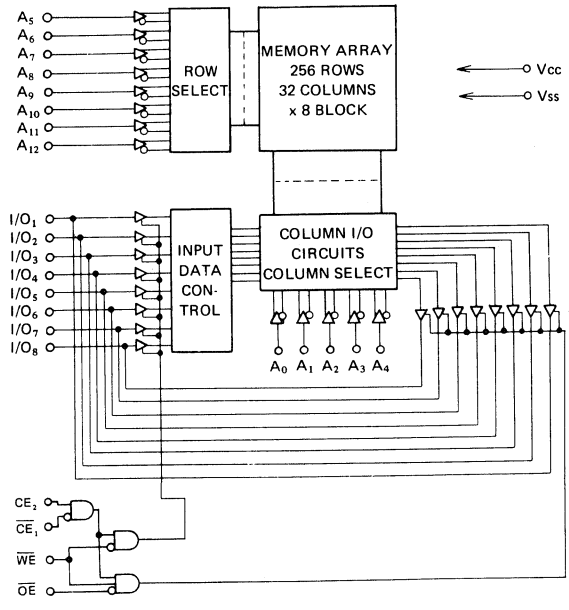
PIN CONFIGURATION

(TOP VIEW)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Wreite	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165L			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CE}_1 \geqq V_{CC}$ − 0.2V, $CE_2 \geqq V_{CC}$ − 0.2V or V_{IN} = 0 to V_{CC}
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL} t_{cyc} = Min, cycle
Operating Supply Current	I_{CCA}			①	mA	T_{CYC} = Min, cycle
				15		T_{CYC} = 1 μs

① 5165L-12 55 mA 5165L-15 50 mA 5165L-20 45 mA

AC CHARACTERISTICS

Test Condition

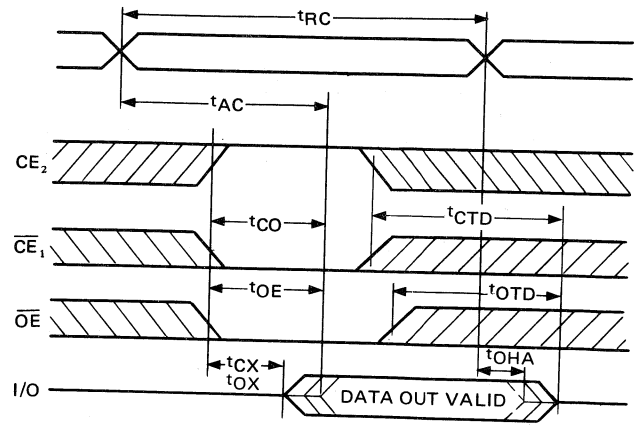
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165L-12		MSM5165L-15		MSM5165L-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Enable Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		70		90	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	40	0	50	0	60	ns
Output 3-state from Chip Deselection	t_{CTD}	0	60	0	70	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE_1}$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE_1}$ or CE_2 whichever occurs last.
3. t_{CXD} is specified from $\overline{CE_1}$ or CE_2 whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

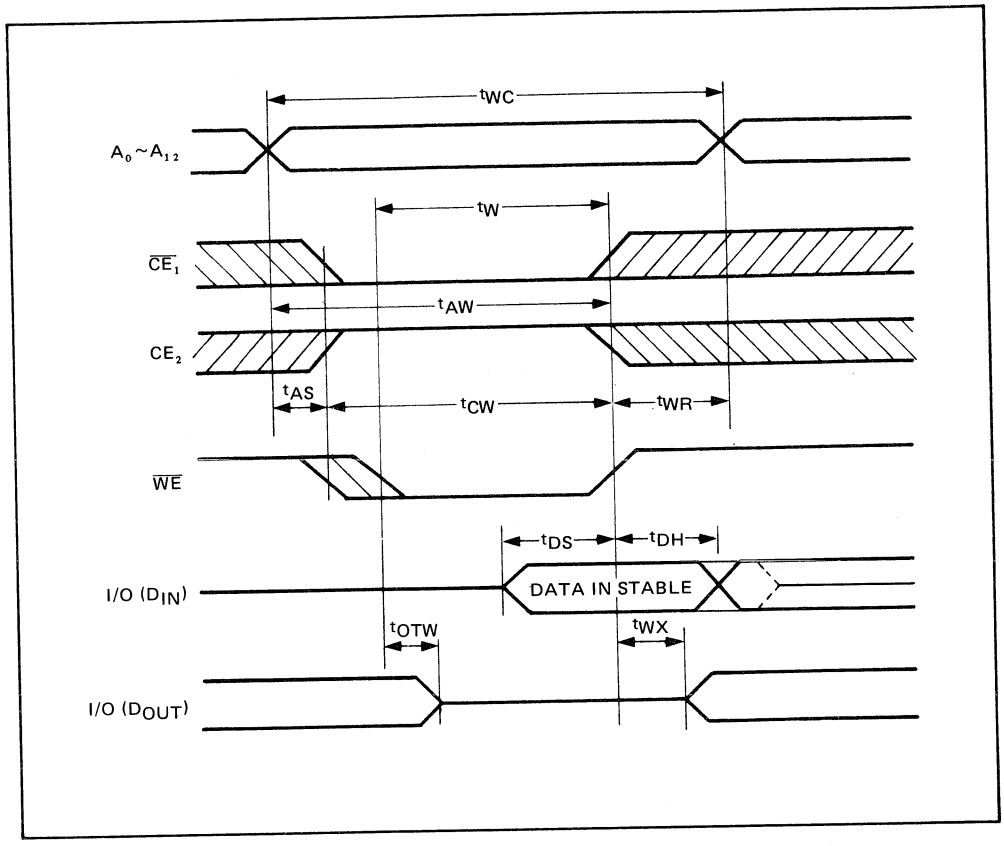
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165L-12		MSM5165L-15		MSM5165L-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	100		120		150		ns
Address Valid to End of Write	t_{AW}	100		120		150		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. OE may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

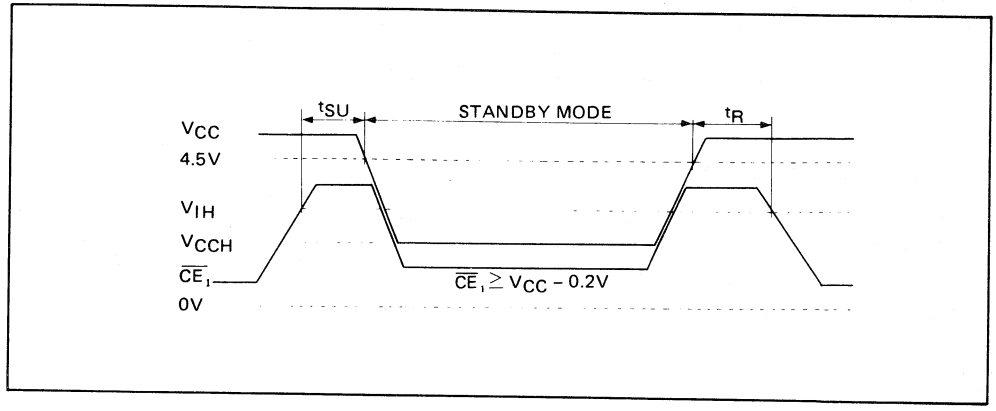


LOW V_{CC} DATA RETENTION CHARACTERISTICS

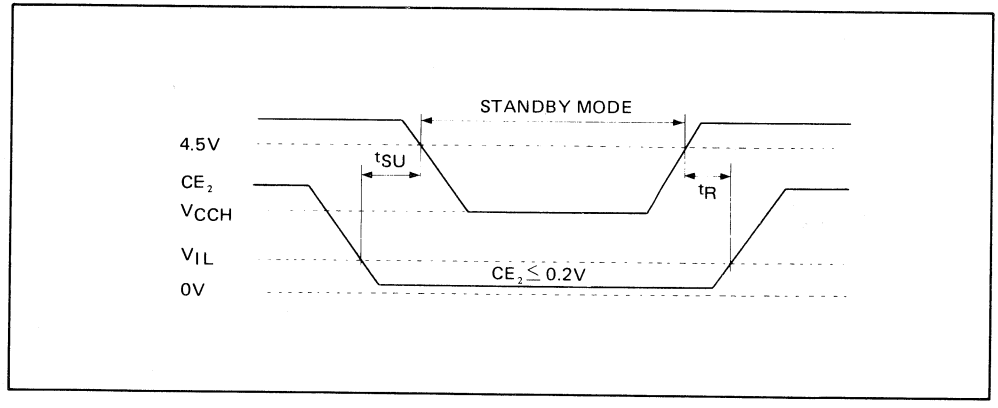
(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$
						$CE_2 \leq 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$
						V_{CC} = 3V, $CE_2 \leq 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CE}_1$ CONTROL



CE_2 CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5188RS

16,384-WORD × 4-BIT HIGH SPEED STATIC CMOS RAM

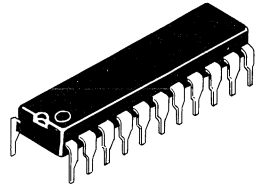
GENERAL DESCRIPTION

The MSM5188 is a static CMOS RAM organized as 16384 words by 4 bits. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary which makes this device very easy to use.

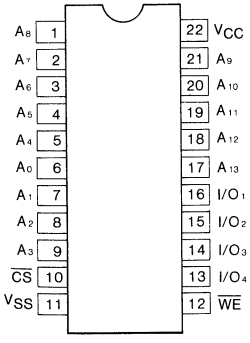
The MSM5188 is offered in a 22-pin slim package.

FEATURES

- Single 5V supply (±10%)
- Completely static operation
- Operating temperature range Ta = 0 to 70°C
- Low power dissipation
  - Standby ..... 11 mW MAX
  - Operation ..... 605 mW MAX
- Access time
  - 45/55/70 ns MAX
- Direct TTL compatible (Input and output)
- 3-State output
- 22 pin DIP PKG (300 mil width)

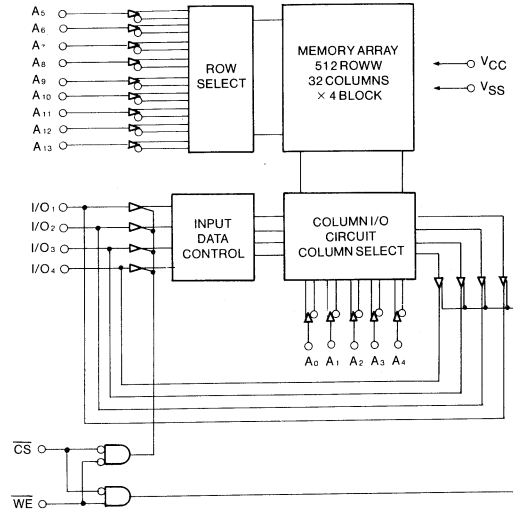


PIN CONFIGURATION



Pin Names	Function
A_0 to A_{13}	Address input
I/O_1 to I/O_4	Data input/output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C Respect to V_{SS}	−0.3 to 7.0	V
Input Voltage	V_{IN}		−0.3 to 7.0	V
Power Dissipation	PD	Ta = 25°C	1.0	W
Operating Temperature	Topr	–	0 to +70	°C
Storage Temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	V_{CC} = 5V ± 10%	2.2	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL}		−0.3	–	0.8	V
Output Load	CL	–	–	–	30	pF
	N	TTL Load	–	–	1	

* When pulse width is equal to or smaller than 20 ns, V_{IH} max = V_{CC} + 1.0V, V_{IL} min = −1.0V.

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	VI = 0 to V_{CC}	−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} VI/O = 0 to V_{CC}	−1		1	μA
"H" Output Voltage	V_{OH}	I_{OH} = −4 mA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC}$ − 0.2V VIN ≦ 0.2V OR VIN ≧ V_{CC} − 0.2V			2	mA
	I_{CCS_1}	$\overline{CS}$ = V_{IH} T_{CYC} = min cycle			30	mA
Operating Supply Current	I_{CCA}	Min cycle			110	mA

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	$V_I = 0V$		6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0V$		8	pF

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Conditions
Input Pulse Level	$V_{IH} = 3.0V$, $V_{IL} = 0V$
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, 1TTL GATE

READ CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}		45		55		70	ns
Address Access Time	T_{AC}		45		55		70	ns
Chip Select Access Time	T_{CO}		45		55		70	ns
Chip Selection to Output Active	T_{CX}	5		5		5		ns
Output Hold Time from Address Change	T_{OHA}	5		5		5		ns
Output 3-state from Deselection	T_{OTD}	0	25	0	25	0	30	ns
Chip Selection to Power up Time	T_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	T_{PD}	0	45	0	55	0	70	ns

Notes: 1. Read Condition: During the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. T_{CX} and T_{OTD} are measured ±200 mV from steady state voltage with specified loading in Figure 2. .

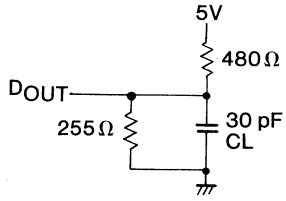


Figure 1 Output Load

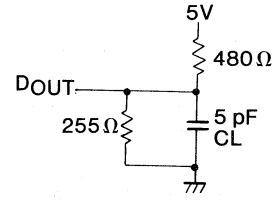


Figure 2 Output Load

Note: CL includes scope and jig.

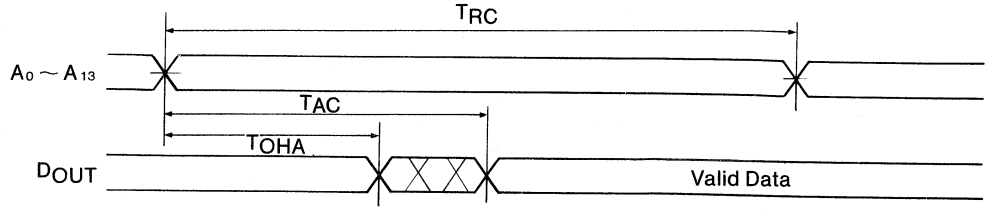
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

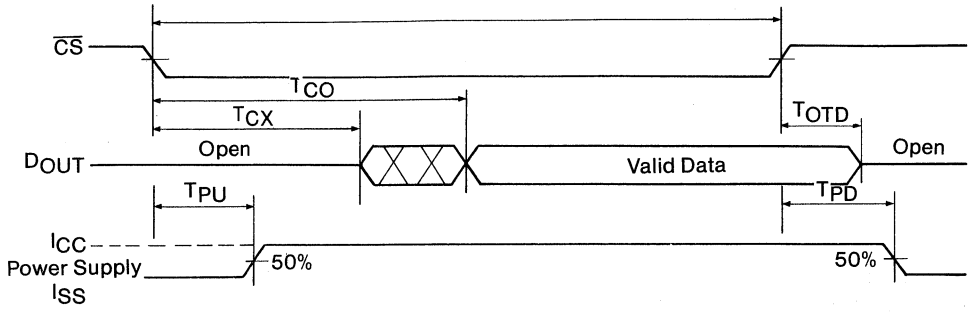
Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	45		55		70		ns
Chip Selection to End of Write	T_{CW}	40		45		55		ns
Address Valid to End of Write	T_{AW}	40		45		55		ns
Address to Write Setup Time	T_{AS}	0		0		0		ns
Write Time	T_W	40		45		55		ns
Write Recovery Time	T_{WR}	5		5		5		ns
Data Setup Time	T_{DS}	25		25		30		ns
Data Hold from Write Time	T_{DH}	0		0		0		ns
Output 3-state from Write	T_{OTW}	0	20	0	25	0	30	ns
Output Active from End of Write	T_{OW}	0		0		0		ns

Notes:
1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. T_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
3. T_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
4. T_{WR}, T_{DS} and T_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
5. T_{OTW} and T_{OW} are measured ±200 mV from steady state voltage with specified loading in Figure 2.
6. When I/O pins are Data output mode, don't force inverse input signals to those pins.

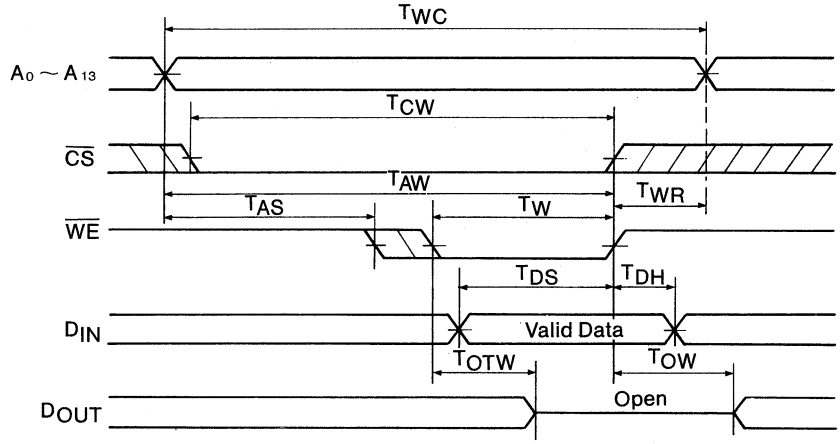
READ CYCLE TIMING 1



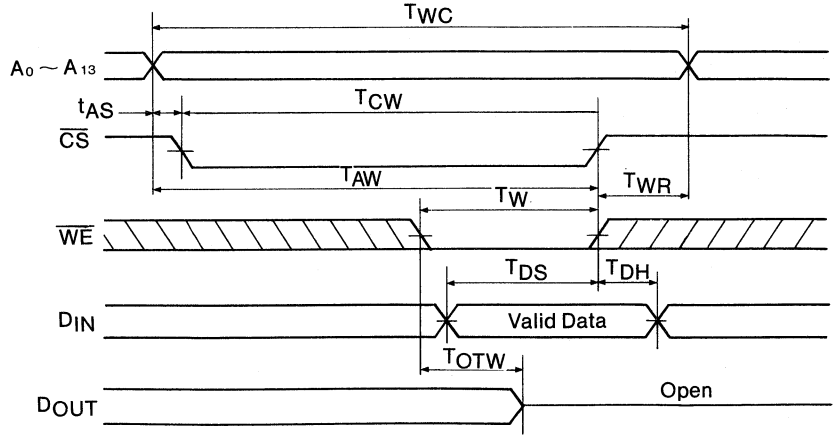
READ CYCLE TIMING 2



WRITE CYCLE TIMING 1
($\overline{WE}$ Control)



WRITE CYCLE TIMING 2
($\overline{CS}$ Control)



OKI semiconductor

MSM51257RS/JS

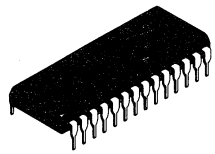
32,768-WORD x 8-BIT CMOS STATIC RAM

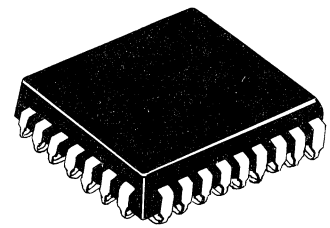
GENERAL DESCRIPTION

The MSM51257RS/JS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257RS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

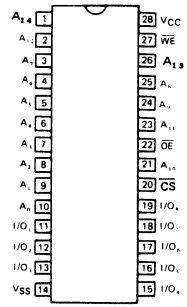
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 5.5 mW MAX
  Operation; 385mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 32-pin PLCC





PIN CONFIGURATION

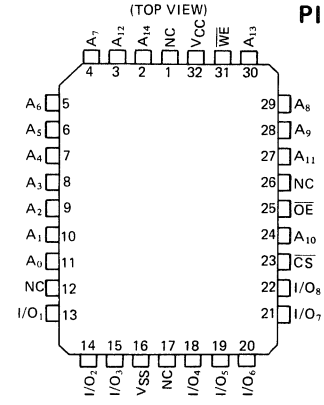
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

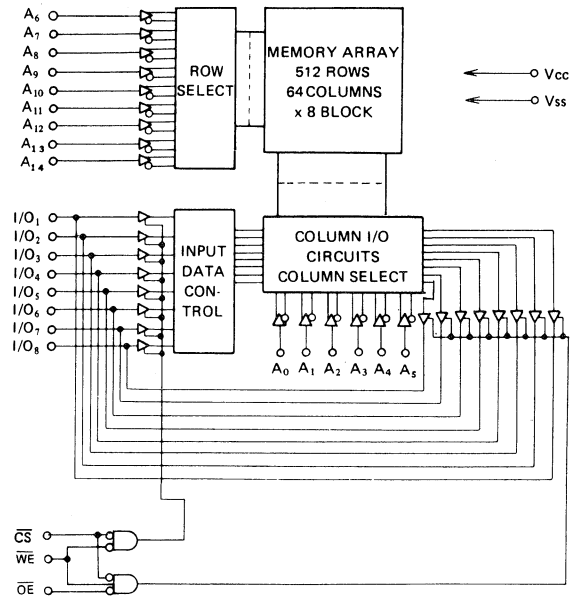
PIN CONFIGURATION

(TOP VIEW)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Wreite	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		0.02	1	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH}
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE

AC CHARACTERISTICS

Test Condition

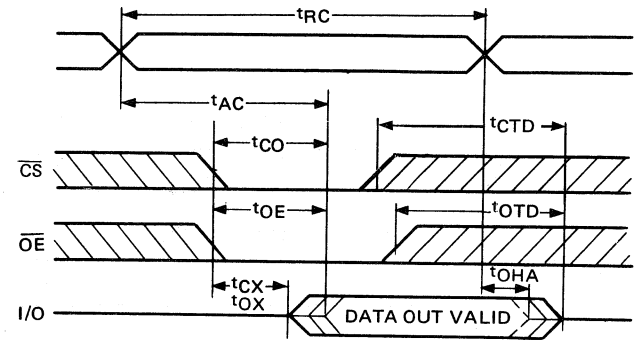
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Output Disable	t_{OTD}	−	30	−	50	−	60	ns
Output 3-state from Chip Deselection	t_{CTD}	−	30	−	40	−	50	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

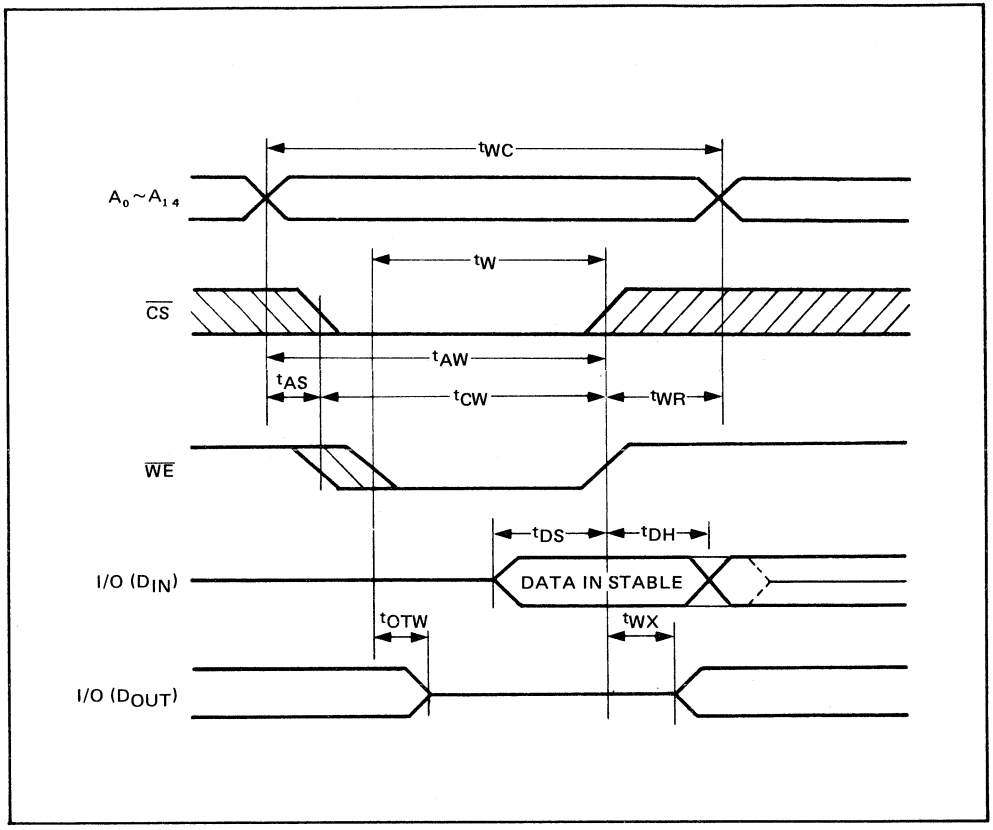
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			10	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM51257LRS/JS

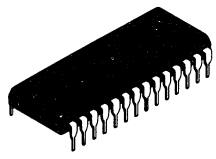
32,768-WORD x 8-BIT CMOS STATIC RAM

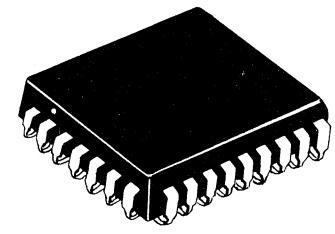
GENERAL DESCRIPTION

The MSM51257LRS/JS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257LRS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

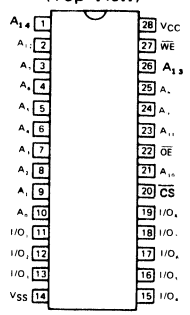
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 385 mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 32-pin PLCC





PIN CONFIGURATION

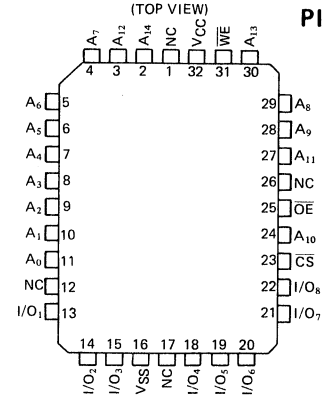
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

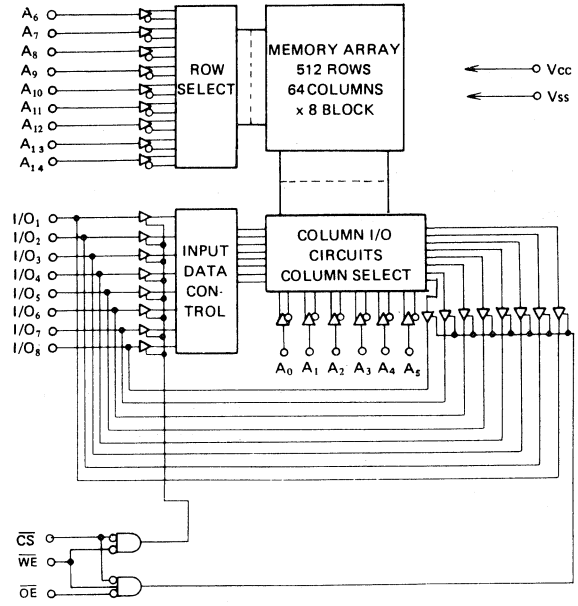
PIN CONFIGURATION

(TOP VIEW)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Wreite	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{ccH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH},
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE

AC CHARACTERISTICS

Test Condition

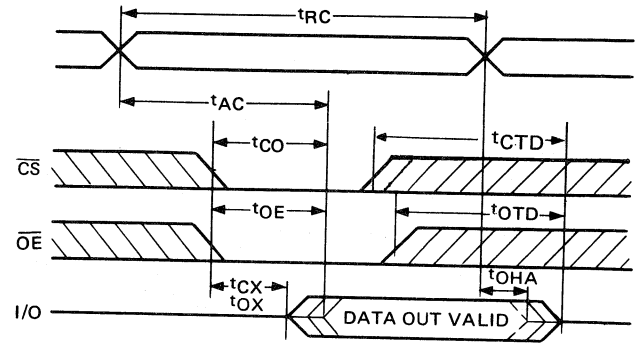
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257L-85		MSM51257L-10		MSM51257L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Output Disable	t_{OTD}	—	30	—	50	—	60	ns
Output 3-state from Chip Deselection	t_{CTD}	—	30	—	40	—	50	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

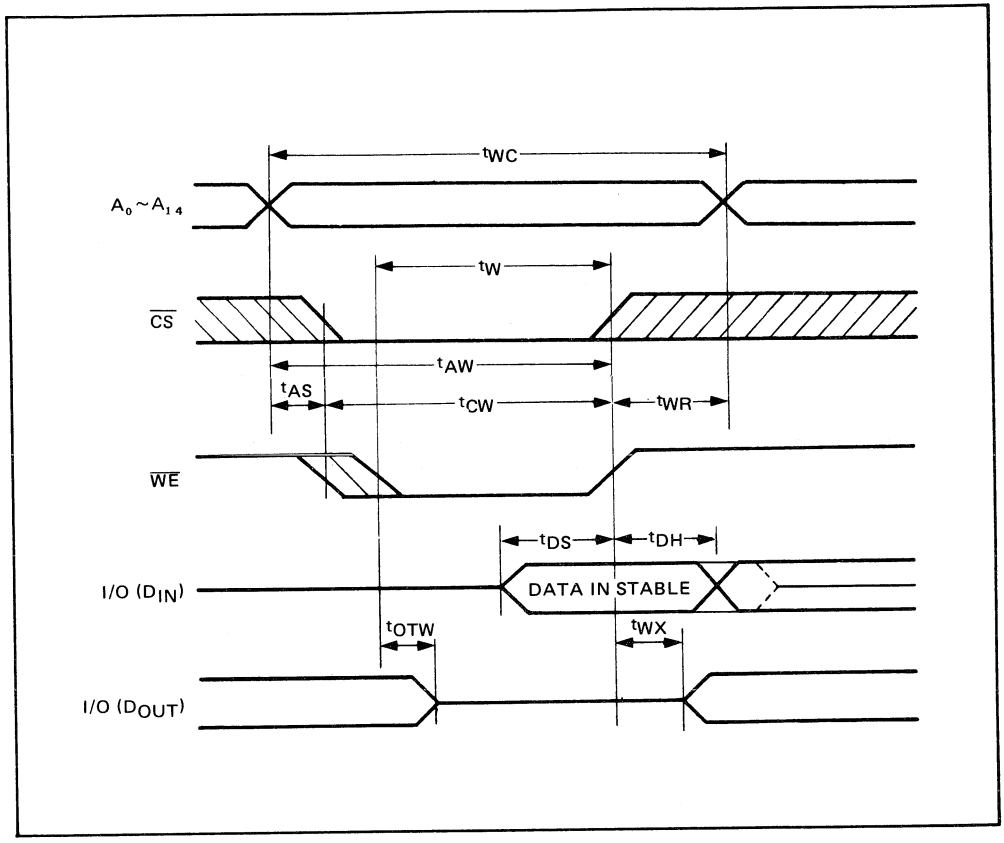
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257L-85		MSM51257L-10		MSM51257L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

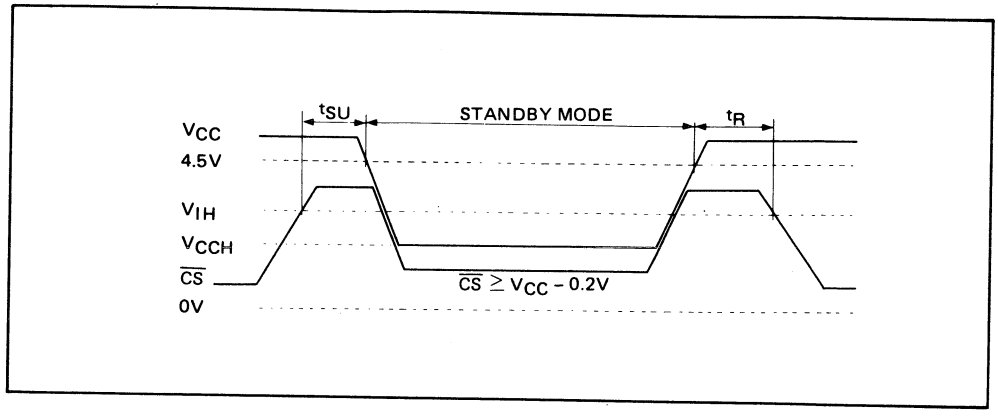


LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CS} \geq V_{CC} - 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CS} \geq V_{CC} - 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CS}$ CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			10	pF

Note: This parameter is periodically sampled and not 100% tested.

MOS MASK ROMS

6 MOS MASK ROMS

MSM3864RS	8,192-Word x 8-Bit MASK ROM (NMOS)	371
MSM38128ARS	16,384-Word x 8-Bit MASK ROM (NMOS)	375
MSM38256RS	32,768-Word x 8-Bit MASK ROM (NMOS)	379
MSM38256ARS	32,768-Word x 8-Bit MASK ROM (NMOS)	383
MSM28101AAS	1M Bit MASK ROM (NMOS)	387
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MSM53256RS	32,768-Word x 8-Bit MASK ROM (CMOS)	397
MSM531000RS	131,072-Word x 8-Bit MASK ROM (CMOS)	401

OKI semiconductor

MSM3864RS

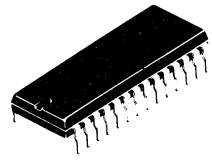
8,192 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM3864RS is an N-channel silicon gate MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expansion of memory and bus line control.

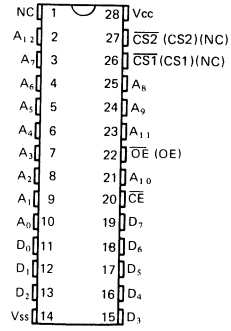
FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

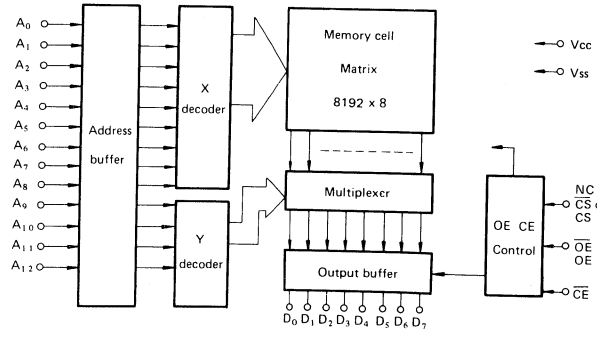
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS1}$, $\overline{CS2}$	:	Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2	5	6	V
	V_{IL}	—	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	—	—	100	mA
	Iccs	Vcc = Max. CE = V_{IH}, I_O = 0 mA	—	—	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	—	—	60	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

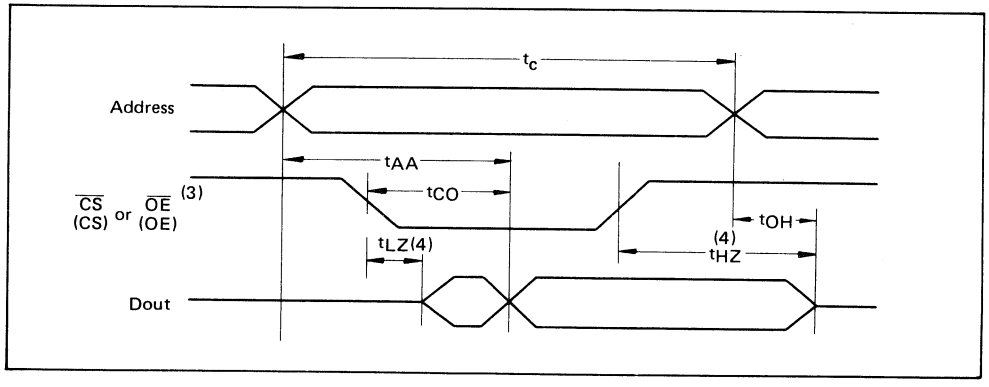
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

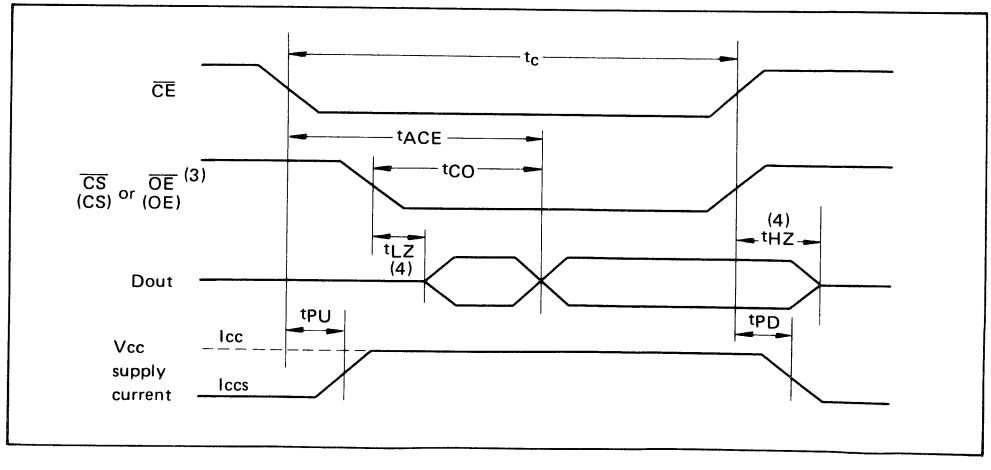
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–		ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–		ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{Lz} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{Hz} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{Hz} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

6

OKI semiconductor

MSM38128ARS

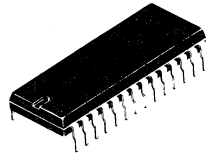
16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

GENERAL DESCRIPTION

The MSM38128ARS is an N-channel silicon gate MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

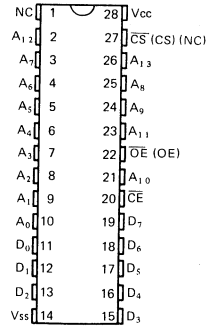
FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

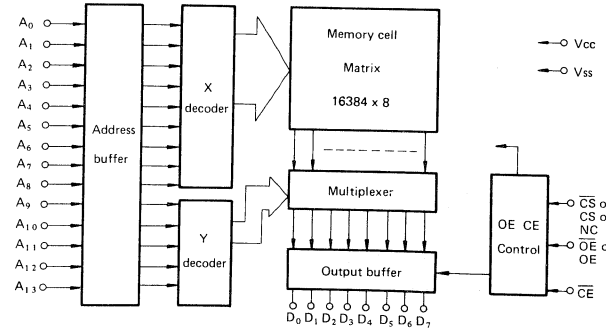
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the $\overline{OE}$ active level and $\overline{CS}$ active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2	5	6	V
	V_{IL}	—	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	—	—	100	mA
	Iccs	Vcc = Max.	—	—	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	—	—	60	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

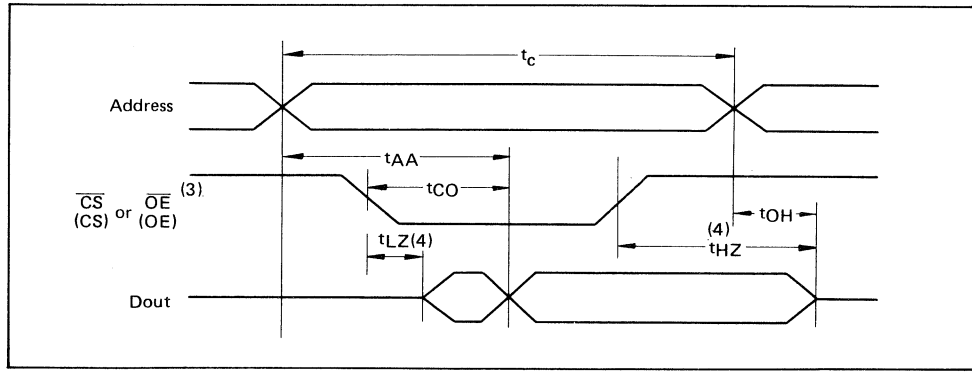
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

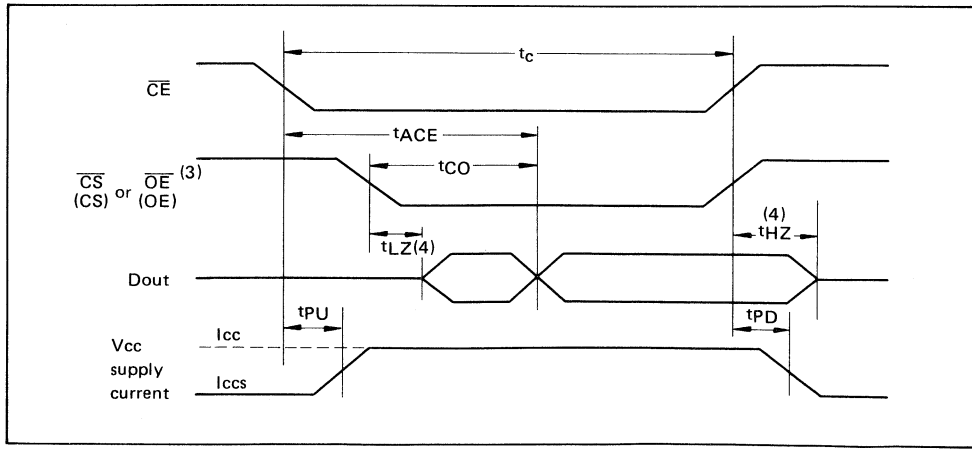
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–		ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–		ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

6

OKI semiconductor

MSM38256RS

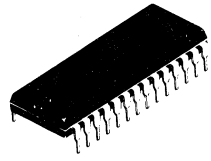
32768 WORD x 8 BIT MASK ROM (E3-S-029-32)

GENERAL DESCRIPTION

The MSM38256RS is an N-channel silicon gate MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides CE, CS and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

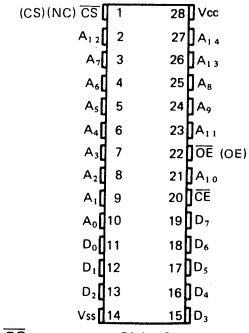
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

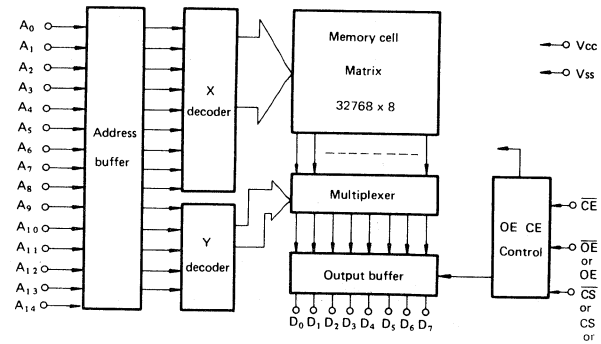
(Top View)



$\overline{CS}$	:	Chip Select
$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable

Note: The $\overline{OE}$ active level and $\overline{CS}$ active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
	V_{SS}		0	0	0	V
Input Signal Level	V_{IH}		2	5	6	V
	V_{IL}		−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		Vcc	V
	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10		10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA			120	mA
	Iccs	Vcc = Max.			30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}			60	mA
Operating Temperature	T_{opr}		0		70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

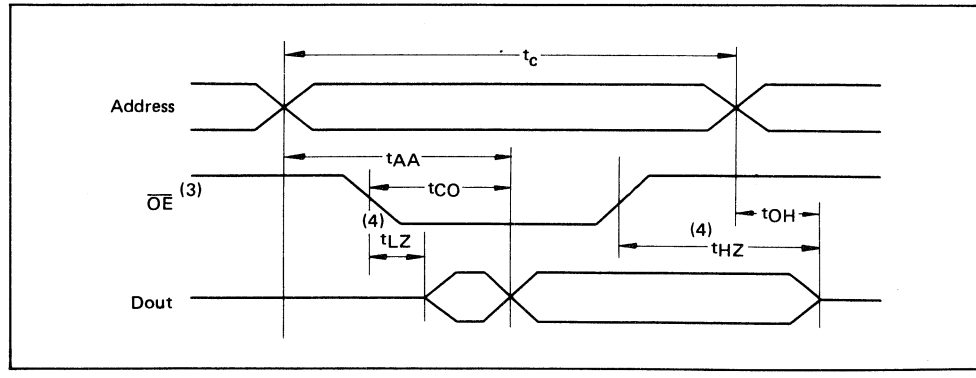
.Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

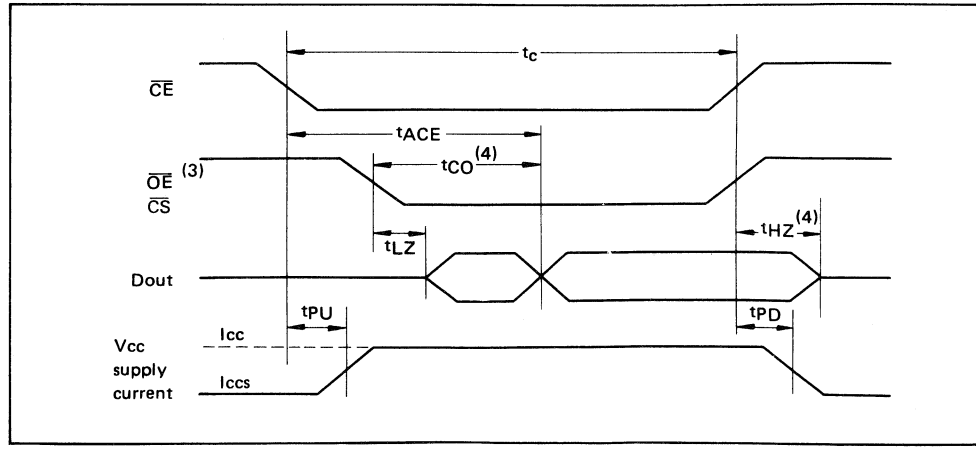
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250			ns	
Address Access Time	t_{AA}			250	ns	
Chip Enable Access Time	t_{ACE}			250	ns	
Output Delay Time	t_{CO}			100	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		100	ns	
Output Retaining Time	t_{OH}	10			ns	
Power Up Time	t_{PU}	0			ns	
Power Down Time	t_{PD}			100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

OKI semiconductor

MSM38256ARS

32768 WORD x 8 BIT MASK ROM (E3-S-030-32)

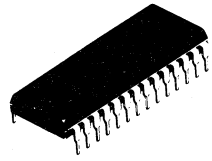
GENERAL DESCRIPTION

The MSM38256ARS is an N-channel silicon gate E/DMOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 6mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides CE, OE, CS signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

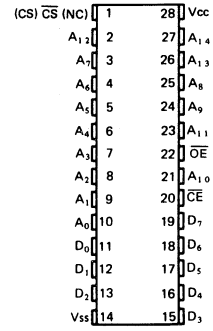
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

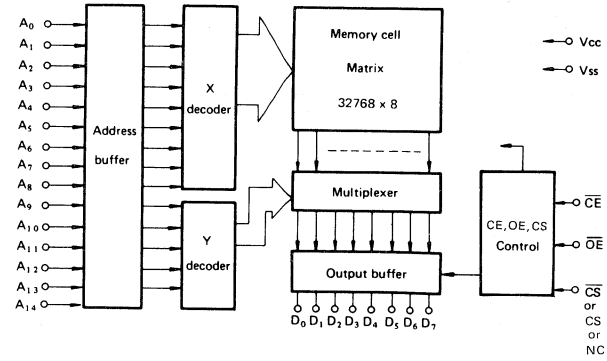
(Top View)



$\overline{CE}$	:	Chip enable
$\overline{OE}$	:	Output enable
(CS) $\overline{CS}$	:	Chip select
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
(NC)	:	No Connection

Note: $\overline{CS}$ active level is specified by customers.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	PD	1.0	W	Per package

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Conditions	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{cc}		4.5	5	5.5	V
	V_{ss}		0	0	0	V
"H" Input Signal Level	V_{IH}		2.2	5	6	V
"L" Input Signal Level	V_{IL}		−0.5	0	0.8	V
"H" Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		V_{cc}	V
"L" Output Signal Level	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{cc}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{cc} Chip not selected	−10		10	μA
Power Supply Current	I_{cc}	V_{cc} = Max. I_O = 0 mA			60	mA
	I_{ccs}	V_{cc} = Max.			6	mA
Peak Power On Current	I_{po}	V_{cc} = GND ~ V_{cc} Min. CE = V_{cc} or V_{IH}			60	mA
Operating Temperature	Topr		0		70	°C
Load Capacitance	C_L				100	pF
Fan Out	N	TTL Load			1	Piece

AC CHARACTERISTICS

TIMING CONDITIONS

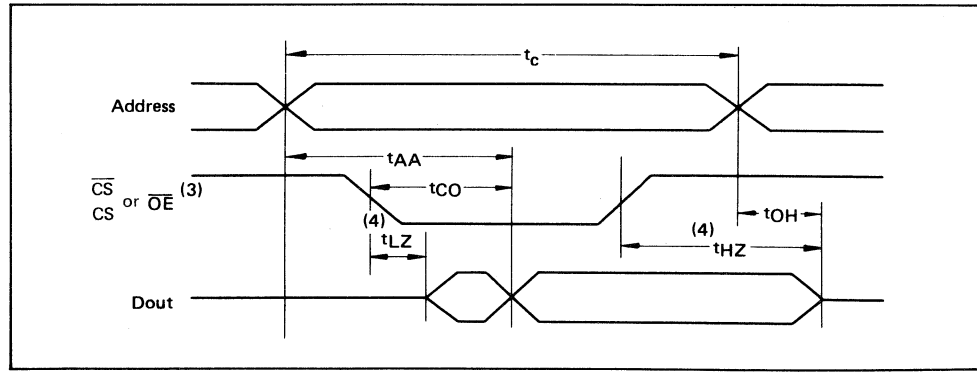
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

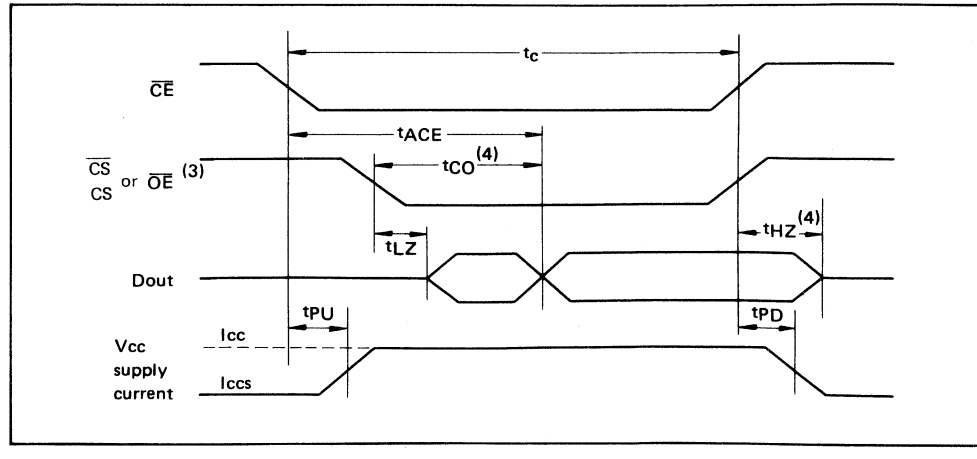
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150			ns	
Address Access Time	t_{AA}			150	ns	
Chip Enable Access Time	t_{ACE}			150	ns	
Output Delay Time	t_{CO}			50	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		50	ns	
Output Retaining Time	t_{OH}	10			ns	
Power Up Time	t_{PU}	0			ns	
Power Down Time	t_{PD}			100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		6	pF	V_O=0V

OKI semiconductor

MSM28101AAS

JAPANESE-CHARACTER GENERATING 1M BIT MASK ROM (E3-S-032-32)

GENERAL DESCRIPTION

The MSM 28101AAS is a 1M Bit Mask ROM using the N-channel silicon gate MOS process which stores 3,760 characters of numeric characters, Japanese cursive and square syllabarys, JIS 1st standard Japanese-characters, etc., in one chip.

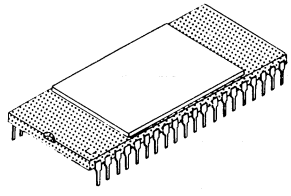
Because of its large capacity, Japanese-character pattern of 3,760 characters can be generated with only one chip. Furthermore, since the dot matrix character form of 18 lines x 16 strings is available from the data out pin by only inputting the JIS Japanese-character code into the address pin, the MSM28101AAS is efficient and optimum for constituting the Japanese-character terminal.

The power supply voltage is of 5 V single power supply, the input level is of TTL compatible, the data output is of 3-state output, the data valid is the output of the open collector and is packaged on the 40-pin DIP.

FEATURES

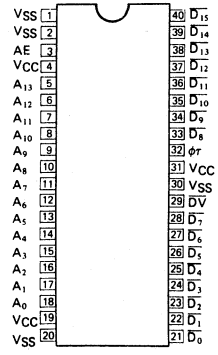
• Function	18 x 16 chinese-character font output
• Configuration	Duplex configuration of cell-array using the defect permissible technique
• Storage capacity	1082880 Bits
• Number of generating characters	3,418 characters
• Storage character range	Partition 0 ~ 7 and partition 16 ~ 47 of Japanese-character code system for JIS information processing
• Address input	14 Bits ($A_0 \sim A_{13}$)
• Data output	16 Bits ($\overline{D_0} \sim \overline{D_{15}}$, 3-state)
• Output mode	16 Bits x 18 times transfer
• Address enable	1 each (AE)
• Data valid	1 each ($\overline{DV}$, open collector output)
• Clock	1 each (ϕT) DC ~ 1.5MHz
• Used temperature	Ta = 0 ~ 70°C
• Access time	10 μs MAX
• Data transfer rate	22 μs/character
• Interface	TTL level
• Power supply voltage	5V single power supply (±5%)
• Power consumption	700 mW TYP
• Package	Side-brazed 40-pin DIP
• Memory cell	Multi-gate ROM

This specification is subject to change without notice



PIN CONFIGURATION

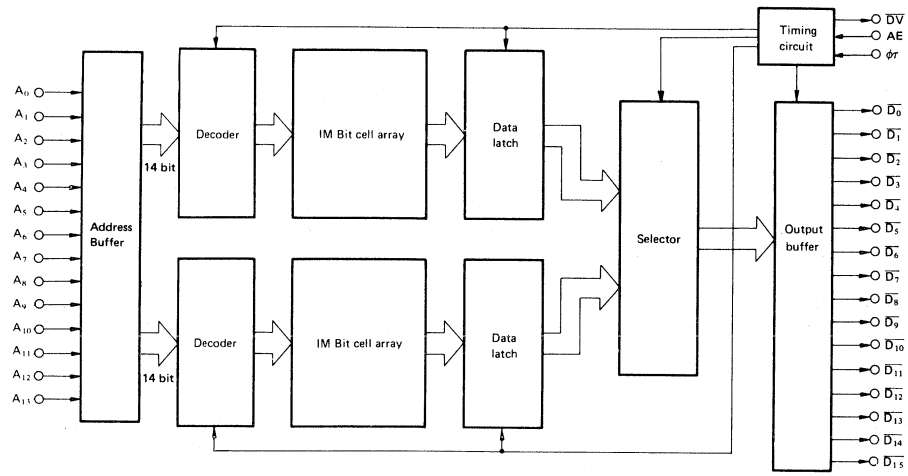
(Top View)



$A_0 \sim A_{13}$: Address input
$\overline{D_0} \sim \overline{D_{15}}$: Data output
AE: Address enable
$\overline{DV}$: Data valid output
ϕT: Clock input
V_{CC}: Power supply voltage (5V)
V_{SS}: GND (OV)

(Note) Connect all V_{CC} and V_{SS} terminals.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5 ~7 •	V
Input Terminal Voltage	V_{IN}	Respect to Vss	−0.5 ~7	V
Output Terminal Voltage	V_{OUT}	Respect to Vss	−0.5 ~7	V
Power Dissipation	P_D		2	W
Operating Temperature	T_{opr}		0 ~70	°C
Storage Temperature	T_{stg}		−35 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vcc	5V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
Input Signal Level	V_{IH}	Respect to Vss	2.0	5	6	V
	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Output Signal Level	V_{OH}	I_{OH}=–0.2 mA	2.4		Vcc	V
	V_{OL}	I_{OL} =1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0 ~Vcc	–10		10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 ~Vcc V_{AE}=0.8V	–10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC}=22μs t_C=650 ms t_{AR}=300 ns			170	mA
Steady State Power Supply Current	I_{CCS}	V_{AE}=0.8V			170	mA

AC CHARACTERISTICS

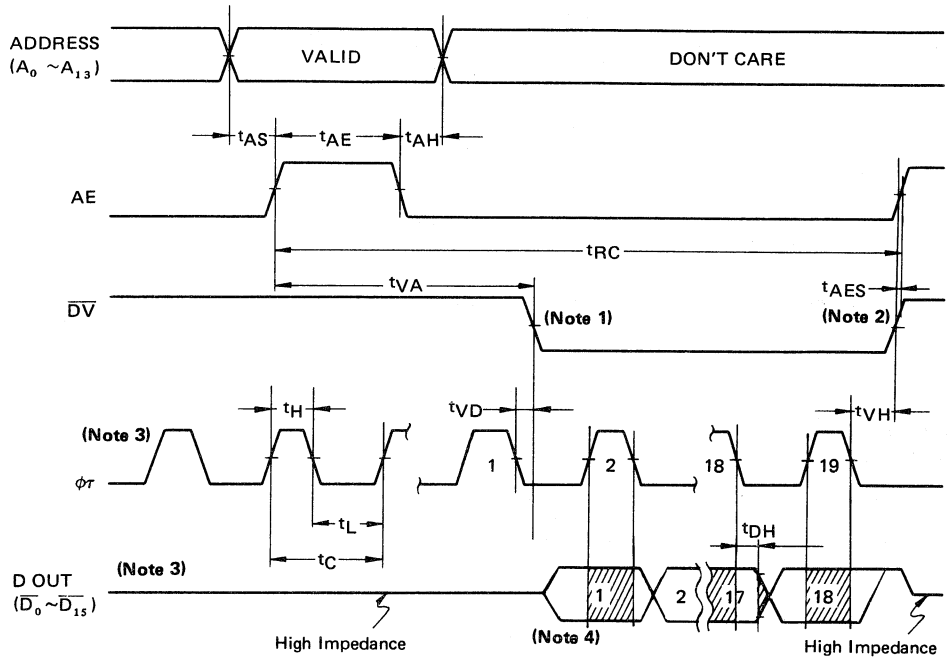
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.0V, V_{IL} = 0.8V
Input Rising, Falling Time	t_r = t_f = 15 ns
Input Timing Level	1.5V
Loading Condition	C_L = 50 pF, 1TTL Gate

READ CYCLE

(Vcc = 5V ±5%, T_a = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



(Note 1) $\overline{DV}$ is determined by the falling of ϕT.
(Note 2) $\overline{DV}$ changes with the falling of ϕT.
(Note 3) ϕT and Dn DATA are repeated 18 times during $\overline{DV}$ is Low.
(Note 4) The $\overline{Dn}$ timing levels are 2.0 V and 0.8 V.
(Note 5) Sometimes it will not normally operate unless input is made at least once with AE as the dummy after input of power supply.
(Note 6) $\overline{DV}$ is an open collector output and $\overline{Dn}$ is a 3-stage output.

INPUT/OUTPUT CAPACITANCE

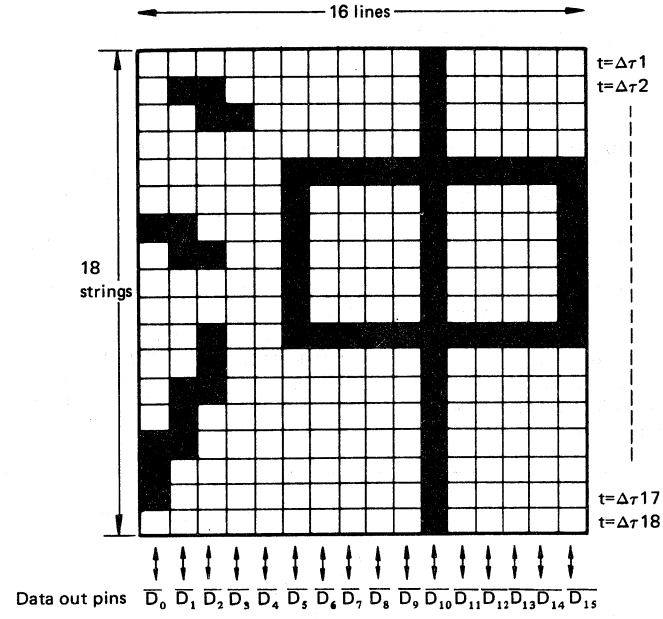
(Ta = 25°C, f = 1 MHz)

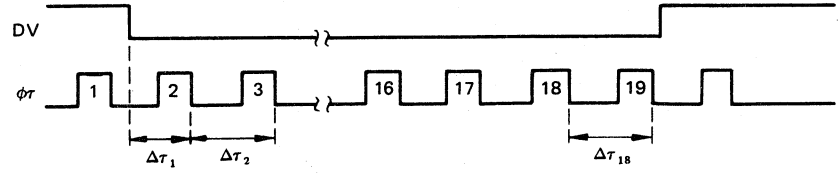
Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_{IN}	V_{IN} = 0V			8	pF
Input Capacitance (AE terminal)	C_{IN}	V_{IN} = 0V			15	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			8	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Specification	Unit	Remarks
Font Type	18 lines x 16 strings dot matrix		
Output Mode	16 bits x 18 times transfer		**(Note 1)**
Number of Generating characters	3418	Word	
Storage Character Range	0 ~ 7 (Non chinese-character area) 16 ~ 47 (JIS 1st standard)	Partition	**(Note 2)**

(Note 1) The correspondence of the 18 lines x 16 strings matrix and the data out pins are as shown in the diagram below.
Output for the character portion will be Low (V_{OL}) and the output for the background portion will be High (V_{OH}).





(Note 2) The correspondence of the 1st and 2nd bytes of JIS C 6226 and the address pins are as shown below.

JIS C 6226	Second byte							First byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

OKI semiconductor

MSM28201AAS

1M BIT MASK ROM FOR JAPANESE-CHARACTER PATTERN (E3-S-033-32)

GENERAL DESCRIPTION

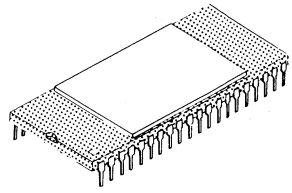
The MSM28201AAS is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 Japanese-characters (kanji conforming with JIS No. 2 standards) incorporated in single chip.

With this large capacity, 3760 Japanese-character patterns can be generated in a single chip. And by only a single input of JIS Japanese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile Japanese-character terminals.

The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

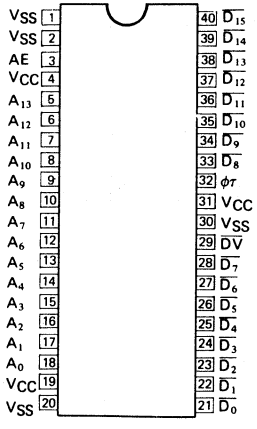
FEATURES

- Function . . . . . 18 x 16 chinese-character font output
- Configuration . . . . Duplex configuration employing defect permissible technique
- Storage capacity . . . 1082880 bits
- Number of generated characters . . . . . 3384 characters
- Accommodation character region . . . Japanese-character encoded partitions 48 to 87 for JIS data processing.
- Address input . . . . 14 bits (A_0 to A_{13})
- Data output . . . . . 16 bits ($\overline{D_0}$ to $\overline{D_{15}}$, tristate)
- Output mode . . . . 16 bit x 18 transfers
- Address enable . . . 1 (AE)
- Data valid . . . . . 1 ($\overline{DV}$, open collector output)
- Clock . . . . . 1 (ϕT) DC to 1.5MHz
- Operating temperature . . . . . Ta=0°C to 70°C
- Access time . . . . . 10 μs MAX.
- Data transfer rate . . 22 μs/character
- Interface . . . . . TTL level
- Power supply voltage 5V single (±5%)
- Power consumption . 700 mW TYP
- Package . . . . . Side-brazed 40-pin DIP
- Memory cell . . . . . Multi-gate ROM



PIN CONFIGURATION

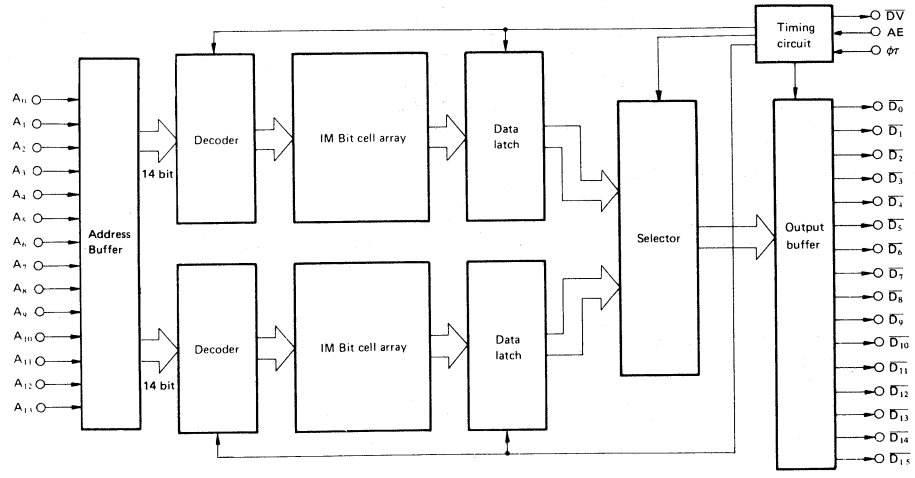
(Top View)



$A_0 \sim A_{13}$: Address inputs
$\overline{D_0} \sim \overline{D_{15}}$: Data outputs
AE : Address enable
$\overline{DV}$: Data valid output
ϕT : Clock input
Vcc : Power supply voltage (5 V)
Vss : GND (0 V)

Note: All Vss pins are to be connected

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5~7	V
Input Voltage	V_I	Respect to Vss	−0.5~7	V
Output Voltage	V_O	Respect to Vss	−0.5~7	V
Power Dissipation	P_D		2	W
Operating Temperature	Topr		0 ~ 70	°C
Storage Temperature	Tstg		−35~125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Range Value			Unit
			Min	Typ	Max	
Power Supply Voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
"H" Input Voltage	V_{IH}	Respect to Vss	2.0	5	6	V
"L" Input Voltage	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
"H" Output Voltage	V_{OH}	I_{OH} = −0.2 mA	2.4		V_{CC}	V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0 ~ V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0 ~ V_{CC} V_{AE} = 0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC} = 22μS, t_C = 650 ns t_{AE} = 300ns			170	mA
Rated Power Supply Current	I_{CCS}	V_{AE} = 0.8V			170	mA

AC CHARACTERISTICS

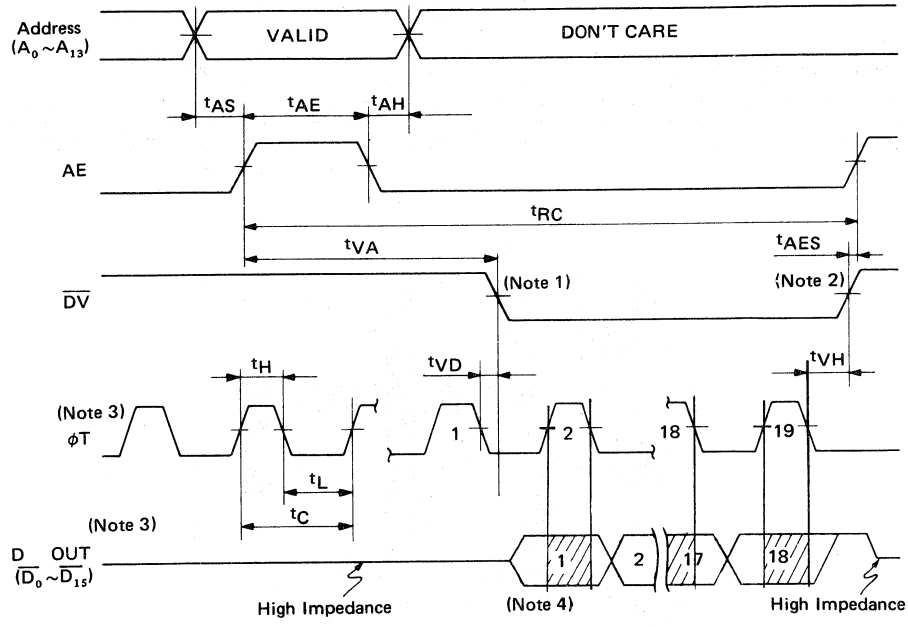
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0 V, V_{IL}=0.8 V
Input Rise/Fall Time	tr=tf=15ns
Input Timing Level	1.5V
Output Load	C_L=50pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



Notes:
1. $\overline{DV}$ is determined by the φT falling edge.
2. $\overline{DV}$ is changed by the φT falling edge.
3. φT and DnDATA are repeated 18 times when $\overline{DV}$ is low.
4. $\overline{Dn}$ timing levels of 2.0V and 0.8V.
5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
6. $\overline{DV}$ denotes open collector output, and $\overline{Dn}$ the tristate output.

INPUT/OUTPUT CAPACITANCE

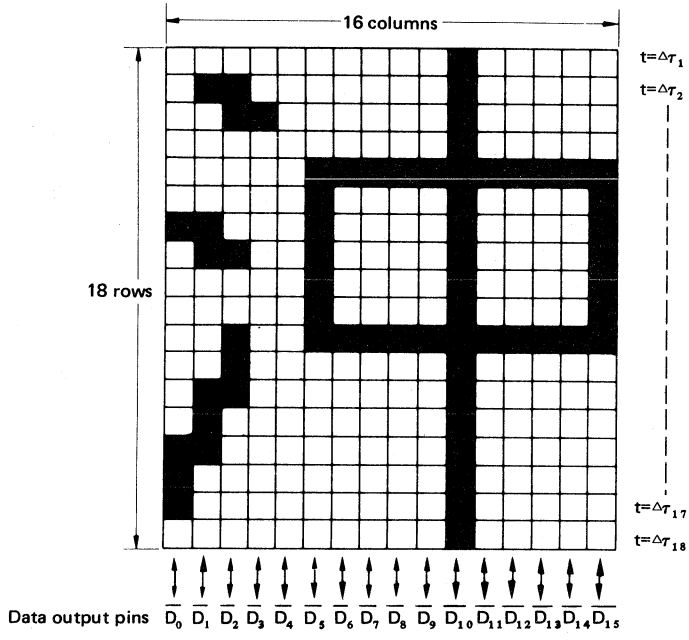
(Ta=25°C, f=1 MHz)

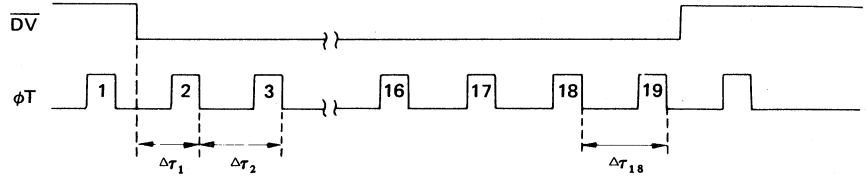
Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_I	V_I=0 V			15	pF
Input Capacitance (AE pin)	C_I	V_I=0 V			35	pF
Output Capacitance	C_O	V_O=0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Range	Unit	Remarks
Font Format	18-row x 16-column dot matrix		
Output Mode	16 bit x 18 transfers		(Note 1)
Number of Characters Generated	3384	Word	
Character Accommodation Region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (V_{OL}) for the character portion, and high (V_{OH}) for the background area.





Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

JIS C 6226	No.2 byte							No.1 byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

OKI semiconductor

MSM53256RS

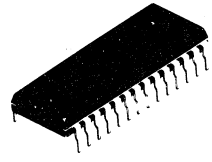
32,768 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM53256RS is a silicon gate CMOS device ROM with 32,768 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

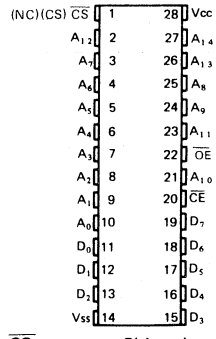
FEATURES

- 256k bits: 32,768 words x 8 bits
- High speed: access time 150 ns max
- Low power: active current 15 mA max
  standby current 0.1 mA max
- Wide tolerance operating: Vcc = 5V ± 10%
- Fully static operating: using no clock
- Fully TTL compatible
- Pin compatible to 256k EPROM
- Packaged to 28 pins plastic
- Fabricated with CMOS silicon gate technology



PIN CONFIGURATION

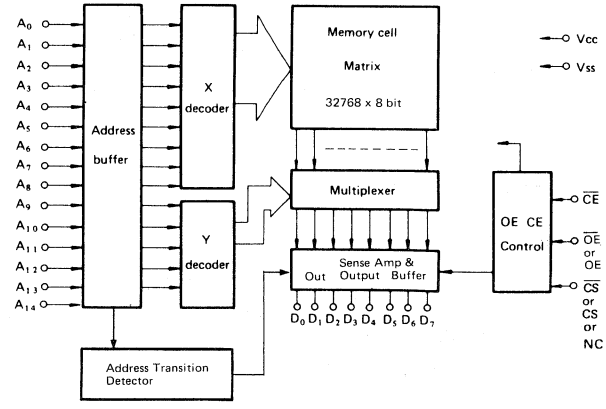
(Top View)



$\overline{CS}$	: Chip select
$\overline{OE}$	: Output enable
Vcc, Vss	: Power supply voltage
$A_0 \sim A_{13}$	: Address input
$D_0 \sim D_7$	: Data output
$\overline{CE}$	: CHip enable

Note: $\overline{CS}$ active level is specified by customer.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 150 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	0.1	mA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	0.5	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

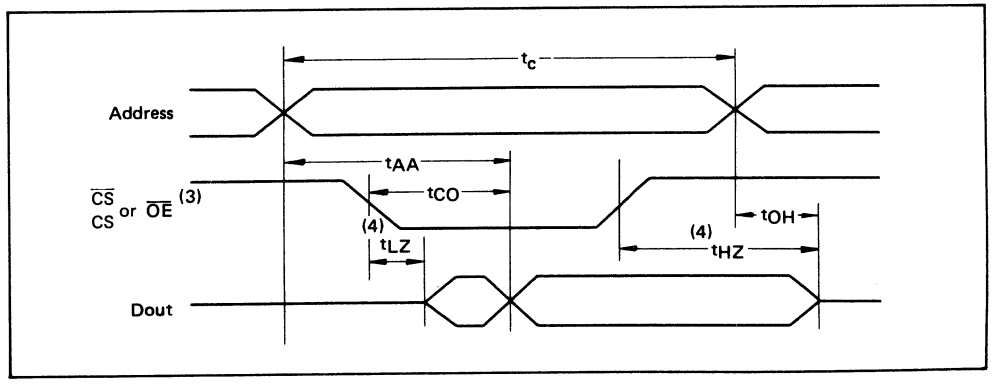
Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

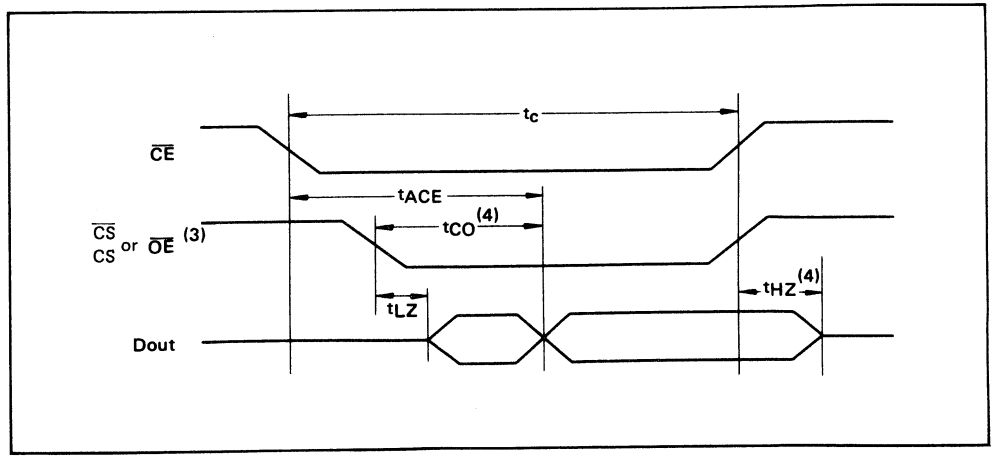
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	150			ns	
Address Access Time	t_{AA}			150	ns	
Chip Enable Access Time	t_{ACE}			150	ns	
Output Delay Time	t_{CO}			50	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		50	ns	
Output Retaining Time	t_{OH}	10			ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		6	pF	V_O=0V

OKI semiconductor

MSM531000RS

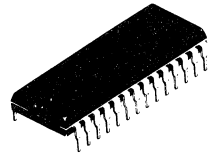
131,072 WORD x 8 BIT MASK ROM (E3-S-031-32)

GENERAL DESCRIPTION

The MSM531000RS is a silicon gate CMOS device ROM with 131,072 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

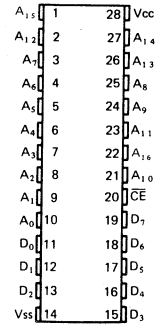
FEATURES

- 131,072 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- 28-pin DIP



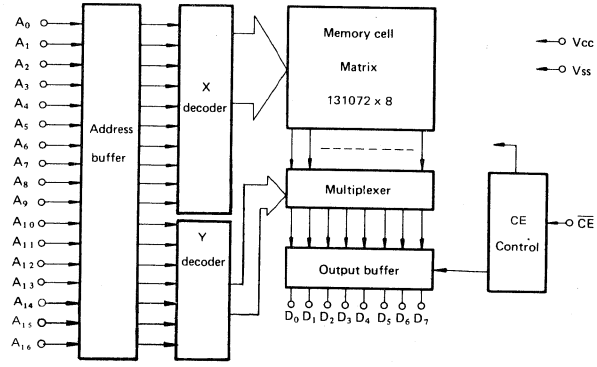
PIN CONFIGURATION

(Top View)



Vcc, Vss : Power supply voltage
$A_0 \sim A_{13}$: Address input
$D_0 \sim D_7$: Data output
$\overline{CE}$: Chip enable

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 250 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	0.1	mA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	0.5	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

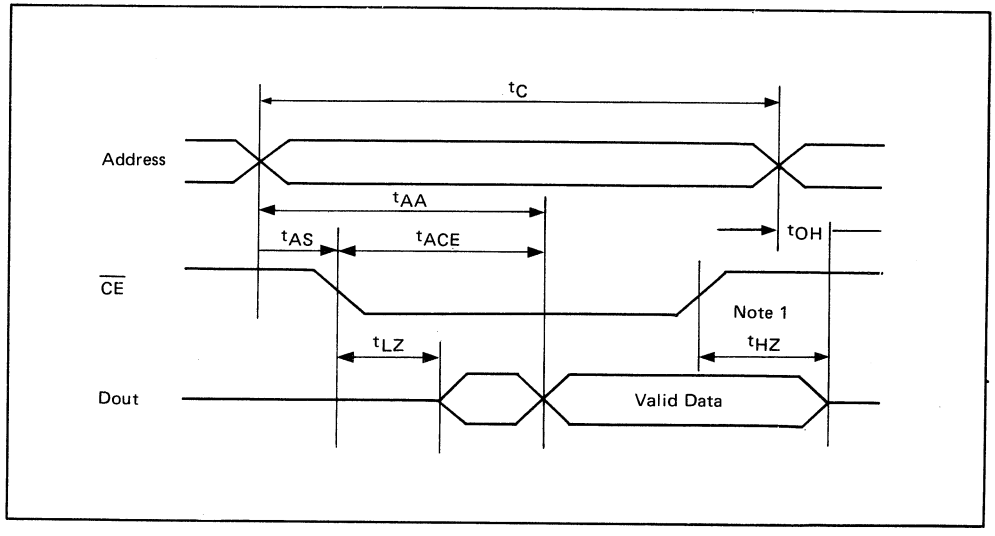
Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–	–	ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Address Setting Time	t_{AS}	0	–	–	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	80	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

READ CYCLE



Note: t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	6	pF	V_O=0V

MOS EPROMS

7 MOS EPROMS

MSM2764A	8,192-Word x 8-Bit EPROM (NMOS)	407
MSM27128A	16,384-Word x 8-Bit EPROM (NMOS)	413
MSM27256	32,768-Word x 8-Bit EPROM (NMOS)	419
MSM27512AS	65,536-Word x 8-Bit EPROM (NMOS)	425
MSM271000	131,072-Word x 8-Bit EPROM (NMOS)	430
MSM271024	65,536-Word x 16-Bit EPROM (NMOS)	436
MSM27C1024	65,536-Word x 16-Bit EPROM (CMOS)	442
MSM2764AZB-RS	8,192-Word x 8-Bit OTP ROM (NMOS)	448
MSM27128AZB-RS	16,384-Word x 8-Bit OTP ROM (NMOS)	453
MSM27256ZB-RS	32,768-Word x 8-Bit OTP ROM (NMOS)	458
MSM27512ZB-RS	65,536-Word x 8-Bit OTP ROM (NMOS)	463

OKI semiconductor

MSM2764A

8192 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

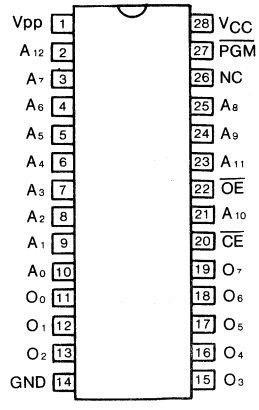
The MSM2764A is a 8192 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM2764A is ideal for microprocessor programs, etc. The MSM2764A is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

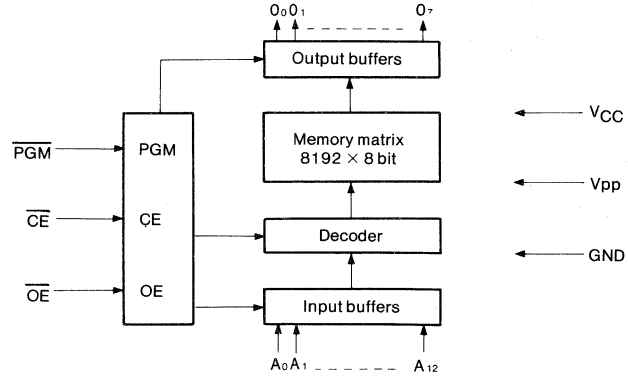
- +5V single power supply
- 8192 words × 8 bit configuration
- Access time:
  - MAX 100 ns (MSM2764A - 10)
  - MAX 120 ns (MSM2764A - 12)
  - MAX 150 ns (MSM2764A - 15)
  - MAX 200 ns (MSM2764A - 20)
  - MAX 250 ns (MSM2764A - 25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	– 0°C ~ 70°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	– 0.6V ~ 7V
Program Voltage	Vpp	–0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V± 5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.0	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

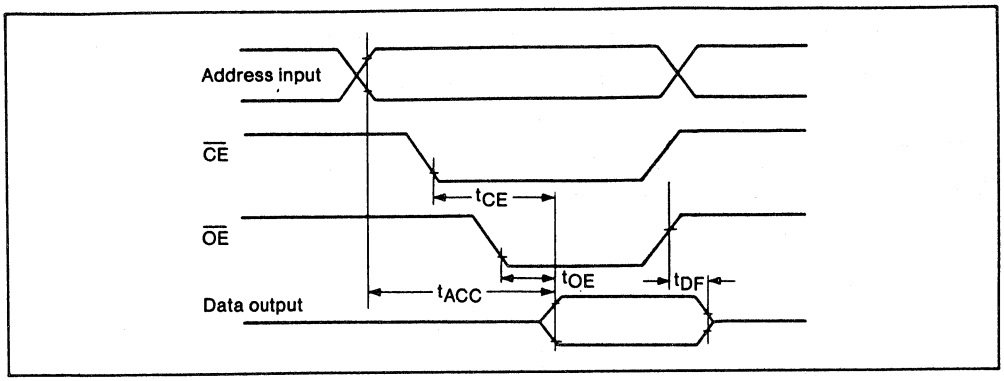
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	2764A-10		2764A-12		2764A-15		2764A-20		2764A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	50	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	40	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ±0.5V, Ta = 25°C±5°C)

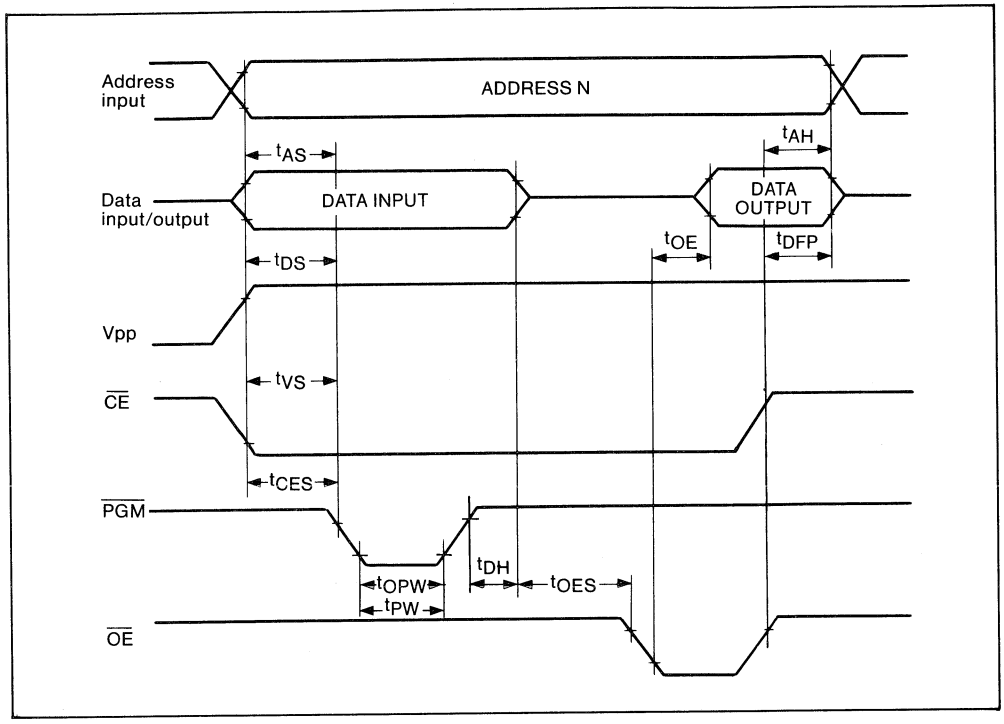
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5 °C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



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CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

MSM27128A

16384 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

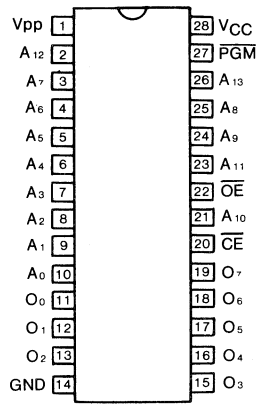
The MSM27128A is a 16834 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27128A is ideal for microprocessor programs, etc. The MSM27128A is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

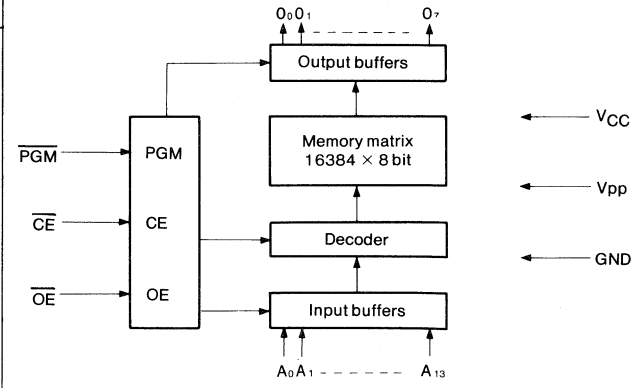
- +5V single power supply
- 16384 words × 8 bit configuration
- Access time:
  - MAX 100 ns (MSM27128A-10)
  - MAX 120 ns (MSM27128A-12)
  - MAX 150 ns (MSM27128A-15)
  - MAX 200 ns (MSM27128A-20)
  - MAX 250 ns (MSM27128A-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	−10°C ~ 80°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

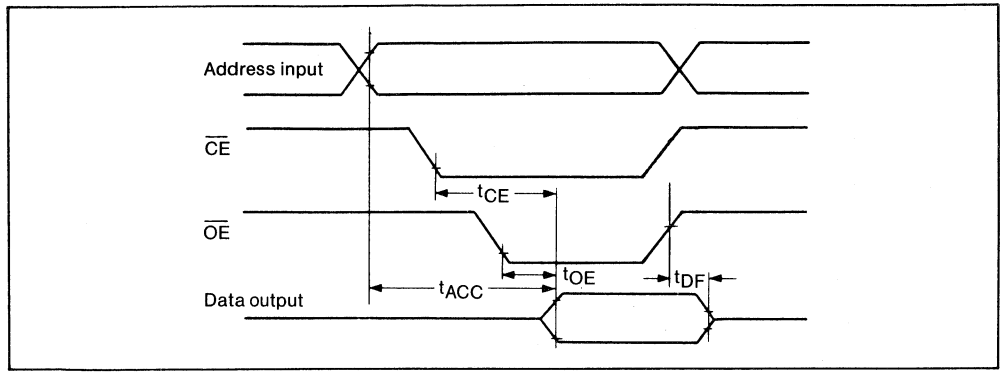
Parameter	Symbol	Conditions	27128A-10		27128A-12		27128A-15		27128A-20		27128A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, PGM = V_{IH}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, PGM = V_{IH}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, PGM = V_{IH}	–	50	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, PGM = V_{IH}	0	40	0	40	0	50	0	55	0	60	ns

Measurement condition

Input pulse level ..... 0.45V and 2.4V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1 TTL GATE + 100pF
Output timing reference level ..... 0.8V and 2.0V

7

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ±0.5V, Ta = 25°C±5°C)

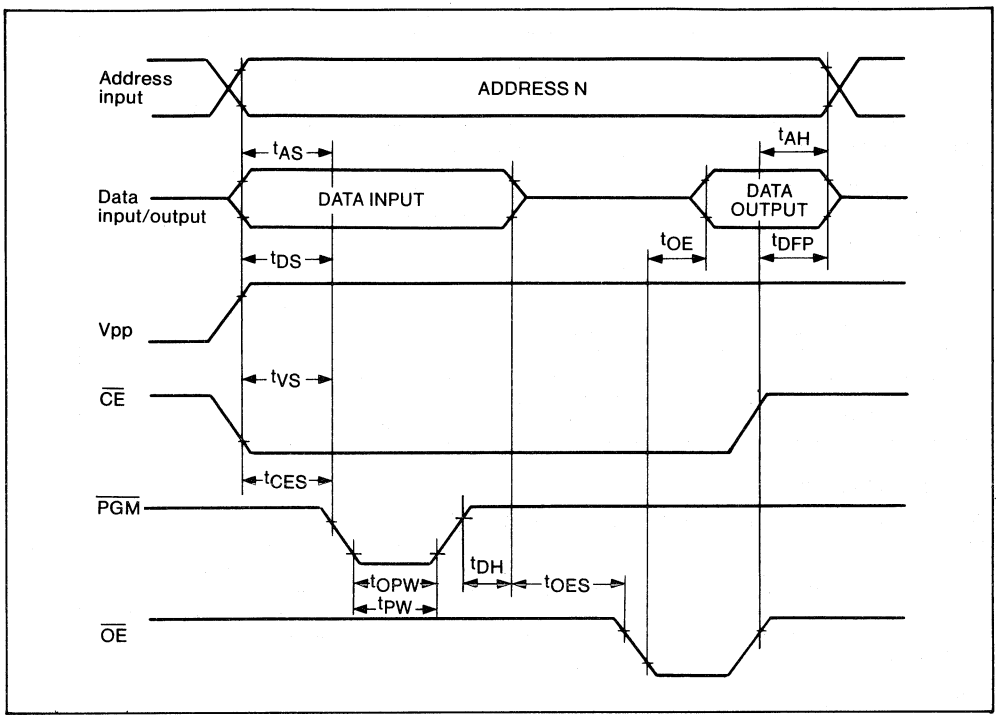
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	–0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = –400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	Vcc = 6V ±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	Vcc =6.25V ±0.25V	95	100	105	μs
Overprogram Pulse Width	t_{PW}	Vcc = 6V ±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from OE	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

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MSM27256

32768 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

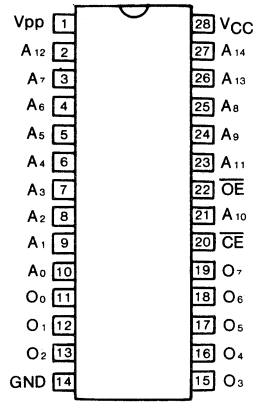
The MSM27256 is a 32768 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27256 is ideal for microprocessor programs, etc. The MSM27256 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

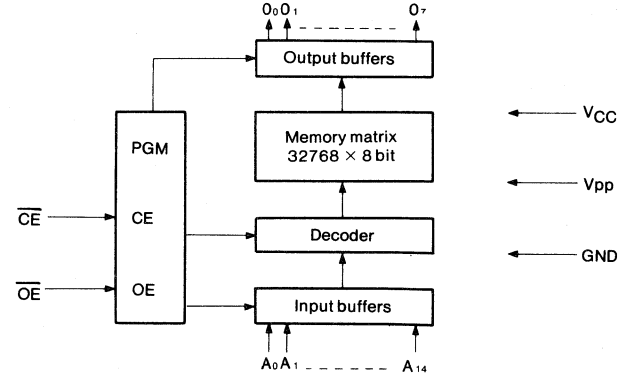
- +5V single power supply
- 32768 words × 8 bit configuration
- Access time:
  - MAX 100ns (MSM27256-10)
  - MAX 120 ns (MSM27256-12)
  - MAX 150 ns (MSM27256-15)
  - MAX 200 ns (MSM27256-20)
  - MAX 250 ns (MSM27256-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.0	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

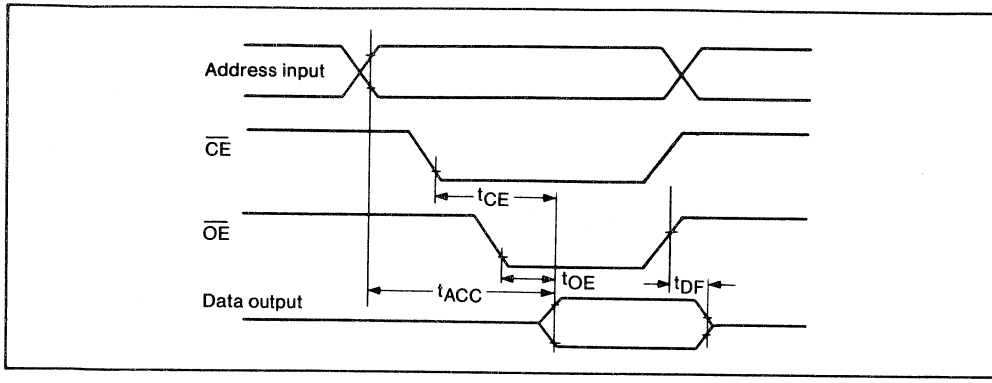
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27256-10		27256-12		27256-15		27256-20		27256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

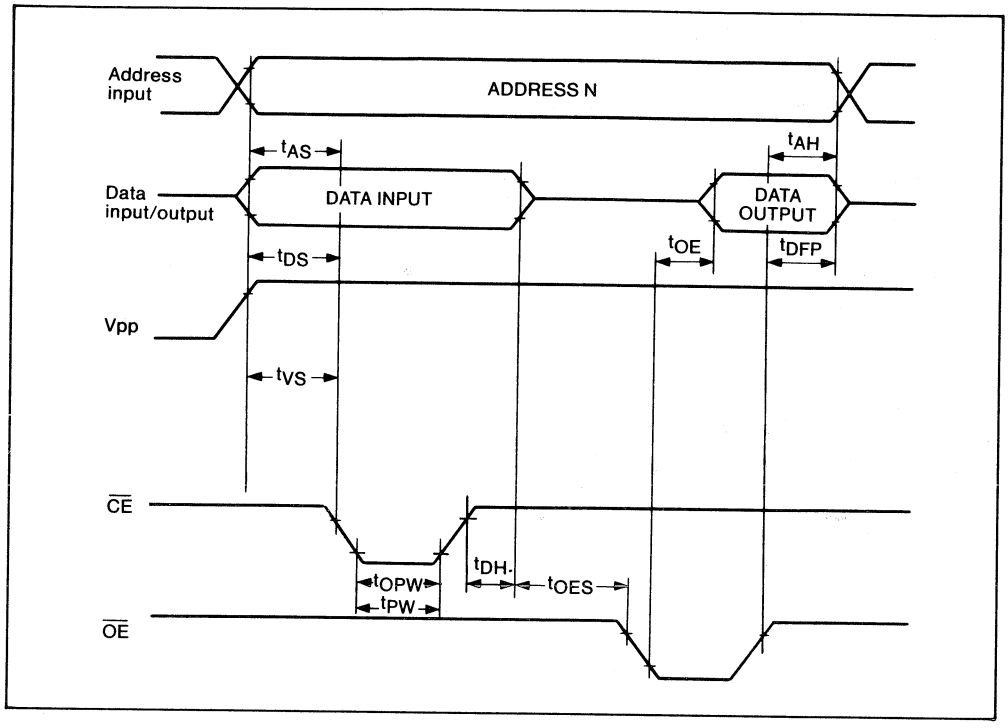
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

Preliminary

OKI semiconductor

MSM27512

65536 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

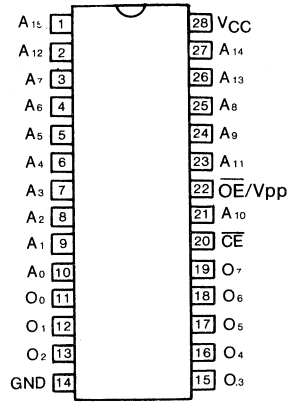
The MSM27512 is a 65536 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27512 is ideal for microprocessor programs, etc. The MSM27512 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

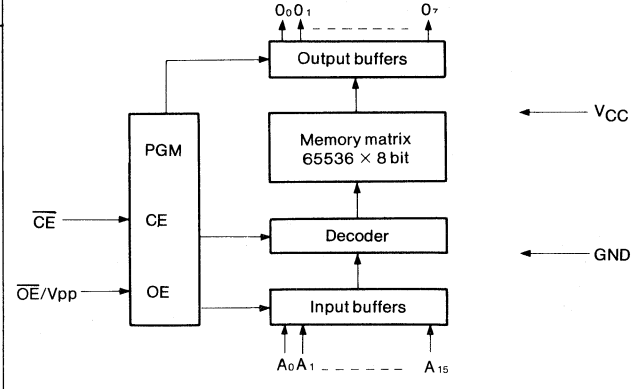
- +5V single power supply
- 65536 words × 8 bit configuration
- Access time:
  - MAX 120 ns (MSM27512-12)
  - MAX 150 ns (MSM27512-15)
  - MAX 200 ns (MSM27512-20)
  - MAX 250 ns (MSM27512-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	High impedance
Stand-by	V_{IH}	–	+5V	High impedance
Program	V_{IL}	12.5V	+6V	D_{IN}
Program Inhibit	V_{IH}	12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

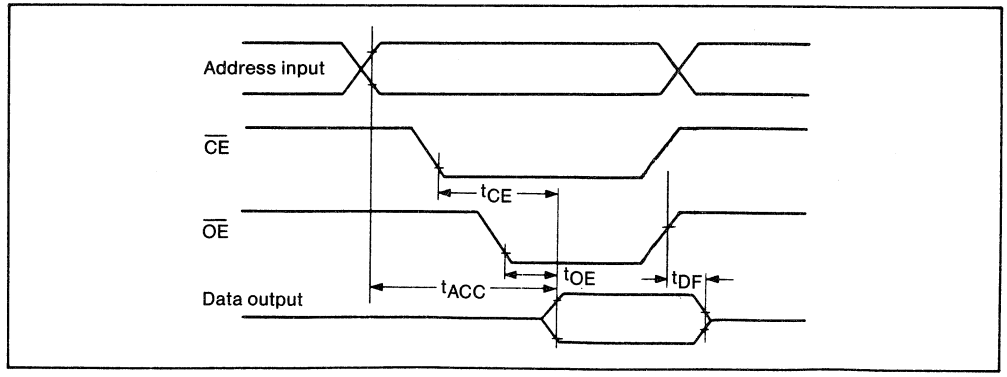
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27512-12		27512-15		27512-20		27512-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$=$\overline{OE}$/Vpp=V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$/Vpp=V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART



< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

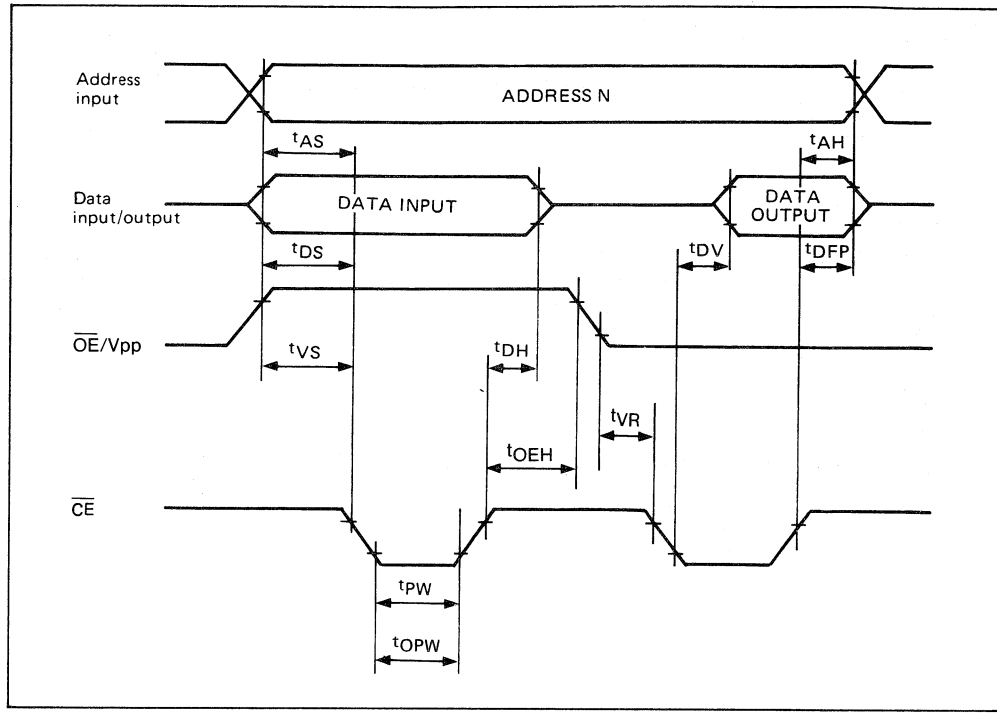
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
$\overline{CE}$ Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC}=6V±0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	V_{CC}=6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC}=6V±0.25V	2.85	–	78.75	ms
$\overline{OE}$/Vpp Hold Time	t_{OEH}	–	2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}	–	–	–	1	μs
$\overline{OE}$/Vpp Recovery Time	t_{VR}	–	2	–	–	μs

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

Preliminary

OKI semiconductor

MSM271000

131072 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

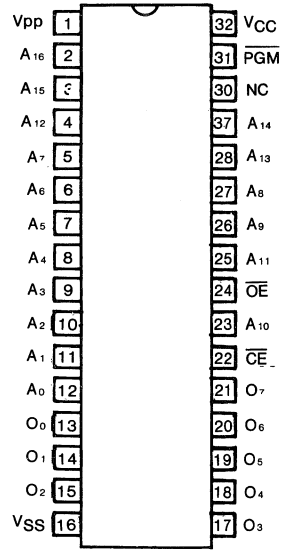
GENERAL DESCRIPTION

The MSM271000 is a 131072 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM271000 is ideal for microprocessor programs, etc. The MSM271000 is manufactured by the N channel double silicon gate MOS technology and is contained in the 32 pin package.

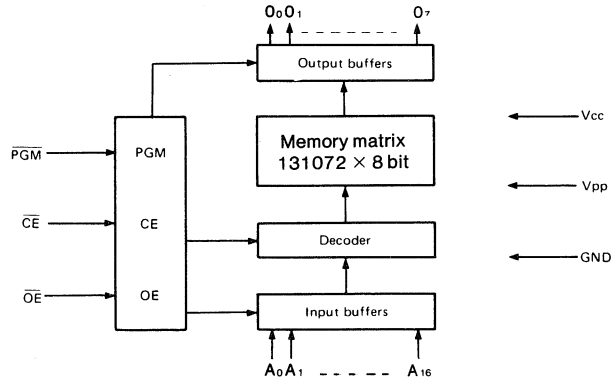
FEATURES

- +5V single power supply
- 131072 words × 8 bit configuration
- Access time:
  MAX120 ns (MSM271000-12)
  MAX150 ns (MSM271000-15)
  MAX200 ns (MSM271000-20)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	Vpp (1)	V_{CC} (32)	Outputs
Read	V_{IL}	V_{IL}	–	–	+5V	Dout
Output Disable	V_{IL}	V_{IH}	–	–	+5V	High impedance
Stand-by	V_{IH}	–	–	–	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V± 5%	V
Vpp Voltage	Vpp	- 0.1	–	Vcc + 1			V
"H" Level Input Voltage	V_{IH}	2.0	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

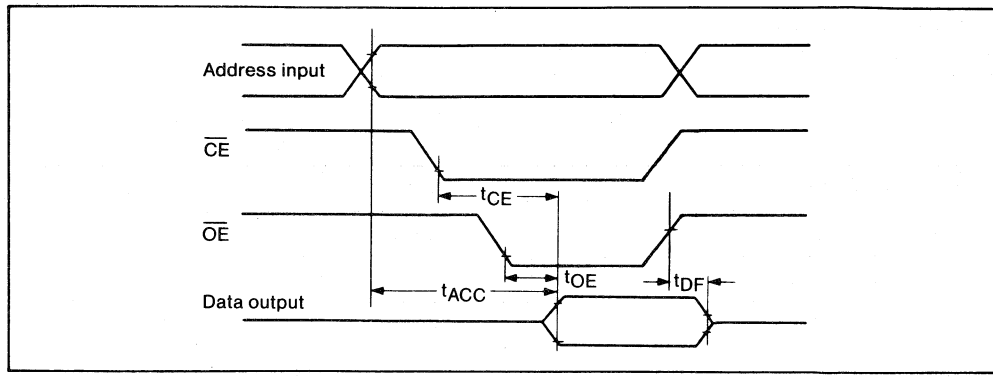
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	271000-12		271000-15		271000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
$\overline{OE}$
Data output
t_{CE}
t_{OE}
t_{DF}
t_{ACC}

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.25V ~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

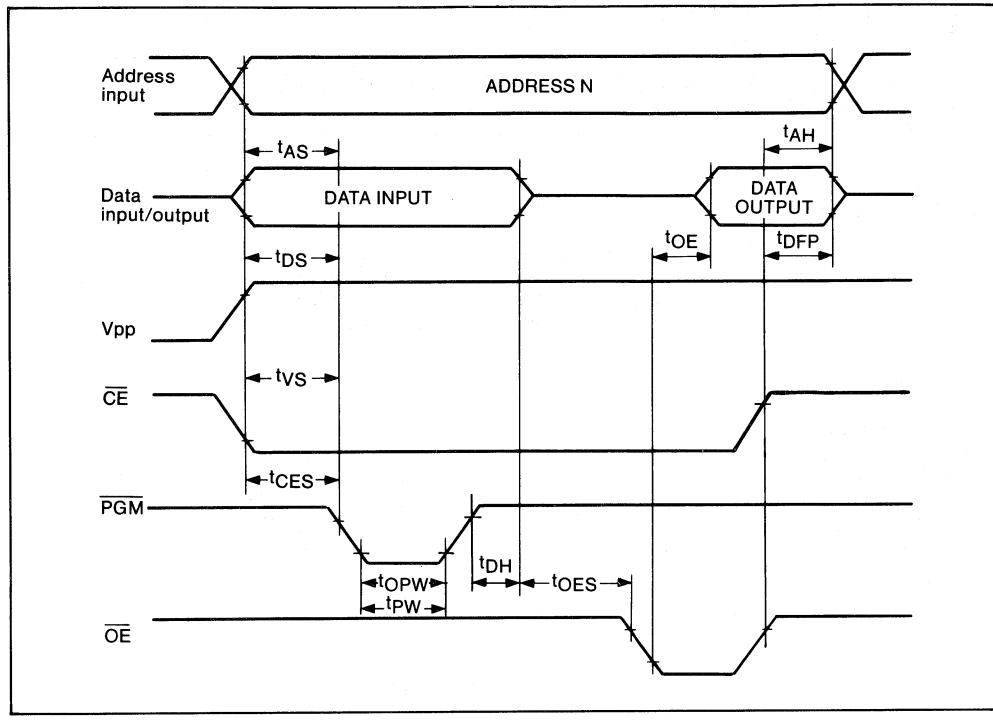
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} =5.25 ~6.5V,Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
Over Program Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85		78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}		2		–	μs
Data Valid from $\overline{OE}$	t_{OE}			–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

MSM271024

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

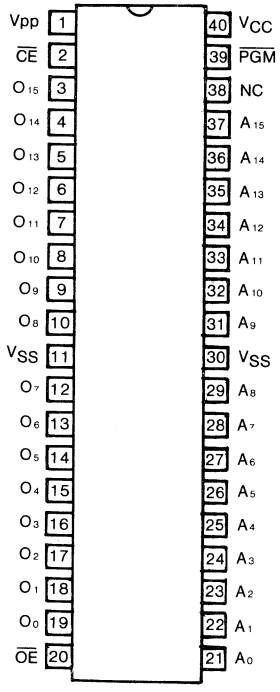
GENERAL DESCRIPTION

The MSM271024 is a 65536 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM271024 is ideal for microprocessor programs, etc. The MSM271024 is manufactured by the N channel double silicon gate MOS technology and is contained in the 40 pin package.

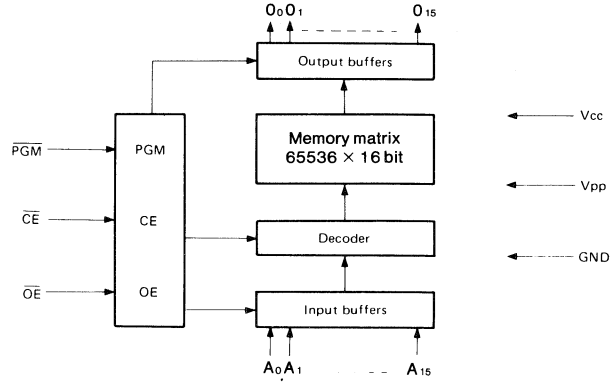
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX120 ns (MSM271024-12)
  MAX150 ns (MSM271024-15)
  MAX200 ns (MSM271024-20)
- Power consumption:
  MAX630 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Pins / Mode	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	Vpp (1)	V_{CC} (40)	Outputs
Read	V_{IL}	V_{IL}	–	–	+5V	Dout
Output Disable	V_{IL}	V_{IH}	–	–	+5V	High impedance
Stand-by	V_{IH}	–	–	–	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V	V
Vpp Voltage	Vpp	−0.1V	–	V_{CC} +1			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	120	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

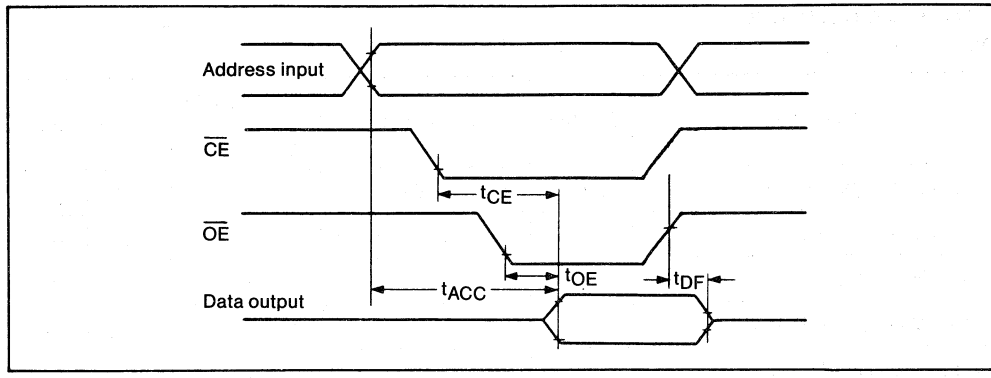
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	271024-12		271024-15		271024-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL},	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL},	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

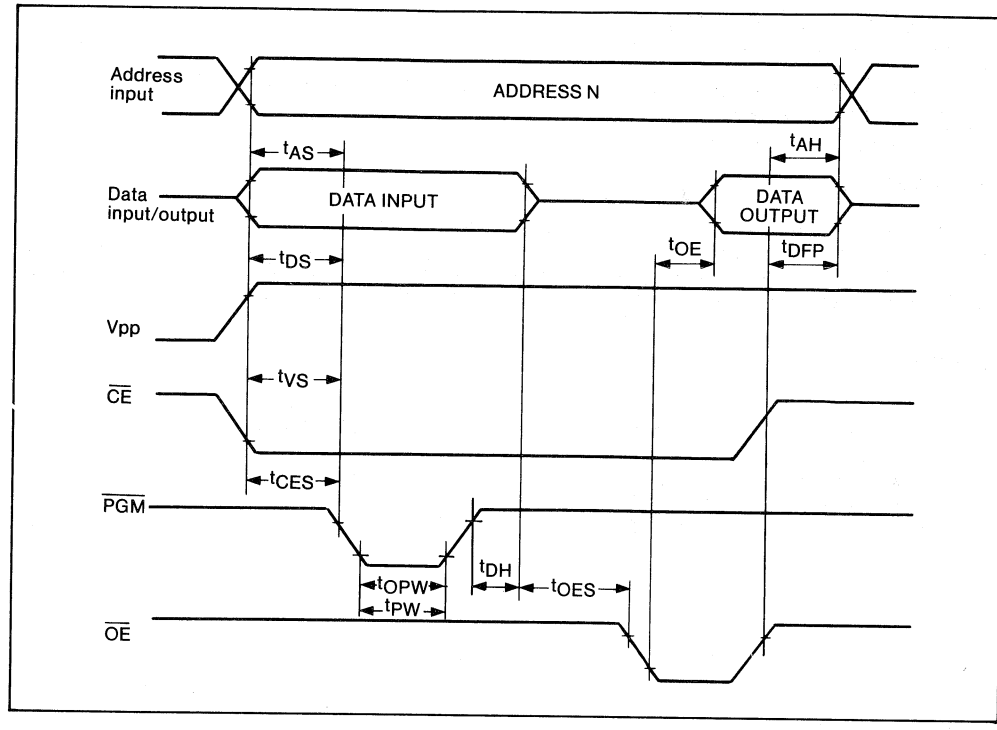
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	V_{CC} = 6.25V±0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

Preliminary

OKI semiconductor

MSM27C1024

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

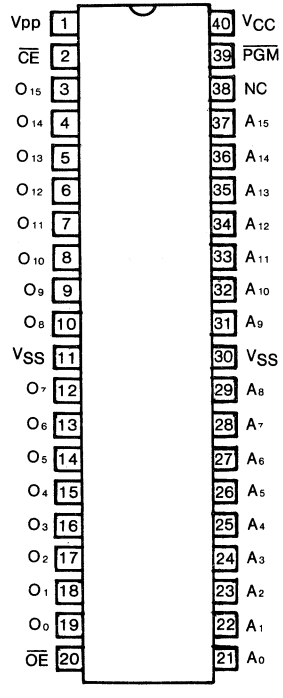
GENERAL DESCRIPTION

The MSM27C1024 is a 65536 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27C1024 is ideal for microprocessor programs, etc. The MSM27C1024 is manufactured by the CMOS double silicon gate technology and is contained in the 40 pin package.

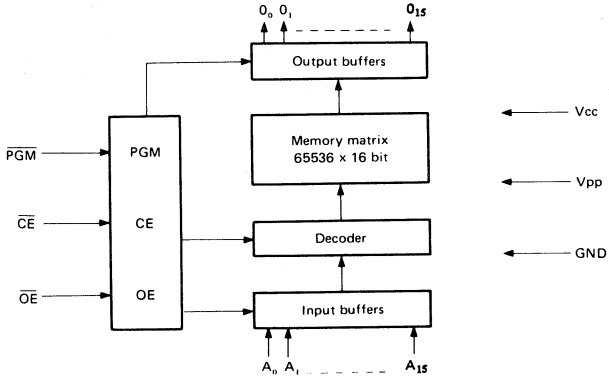
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX120 ns (MSM27C1024-12)
  MAX150 ns (MSM27C1024-15)
  MAX200 ns (MSM27C1024-20)
- Power consumption:
  MAX 165 mW (during operation)
  MAX0.55 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	Vpp (1)	V_{CC} (40)	Outputs
Read	V_{IL}	V_{IL}	–	–	+5V	Dout
Output Disable	V_{IL}	V_{IH}	–	–	+5V	High impedance
Stand-by	V_{IH}	–	–	–	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	V_{IN} = −0.6V ~ 13V, V_{OUT} = −0.3V ~ V_{CC} + 1V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±0.5V	V
Vpp Voltage	Vpp	−0.1	–	V_{CC}+1			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I^{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH} = V_{CC}	–	–	1	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	10	μ
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

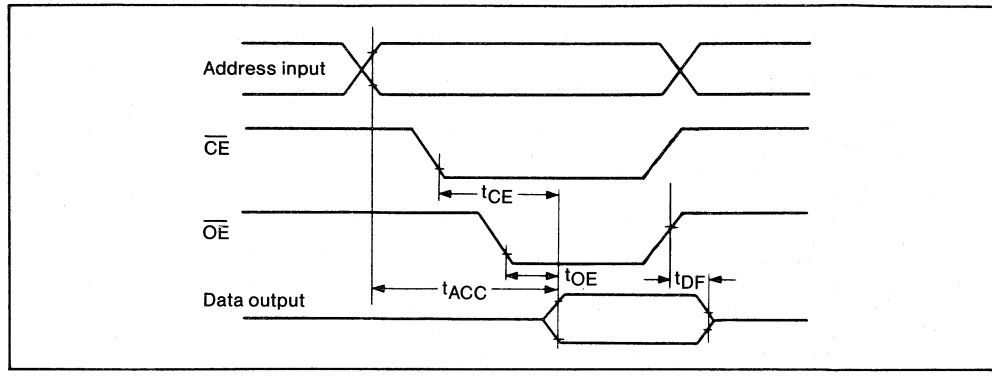
(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C1000-12		27C1000-15		27C1000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	40	0	50	0	55	ns

Measurement condition

Input pulse level ..... 0.45V and 2.4V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1TTL GATE + 100pF
Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

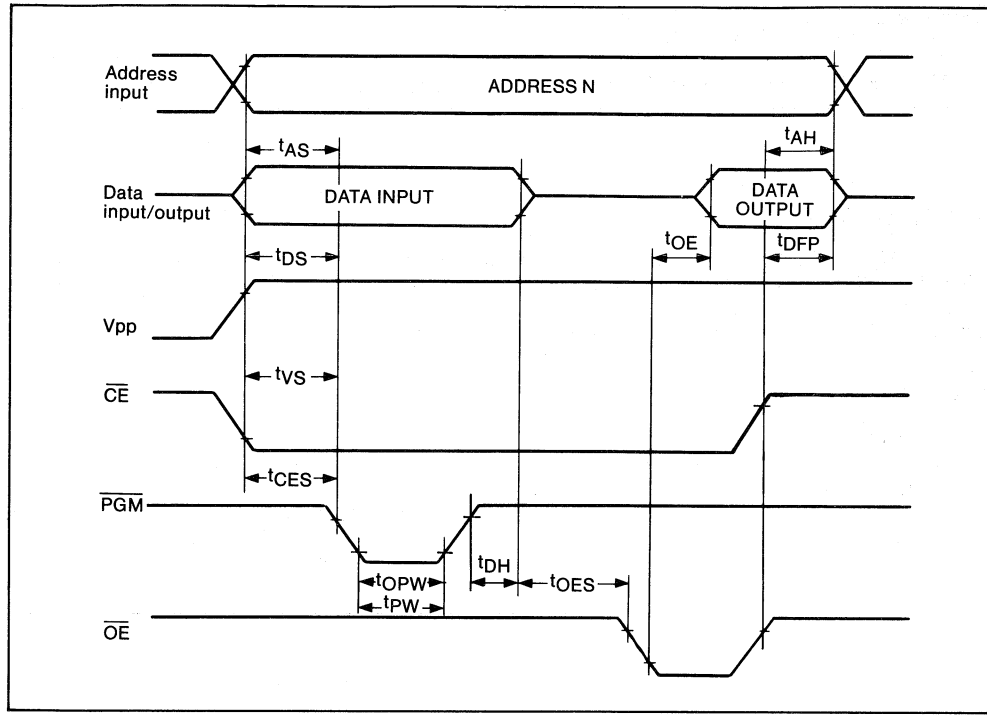
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	30	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC}=6V±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	V_{CC}=6.25V±0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC}=6V±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

MSM2764AZB-RS

8,192 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

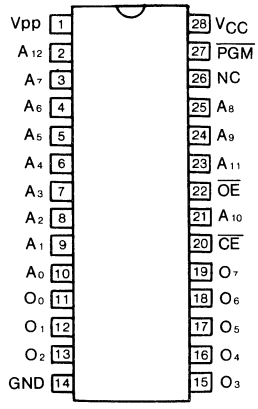
The MSM2764AZB is a 8,192 words × 8-bit electrically programmable read-only memory. The MSM2764AZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

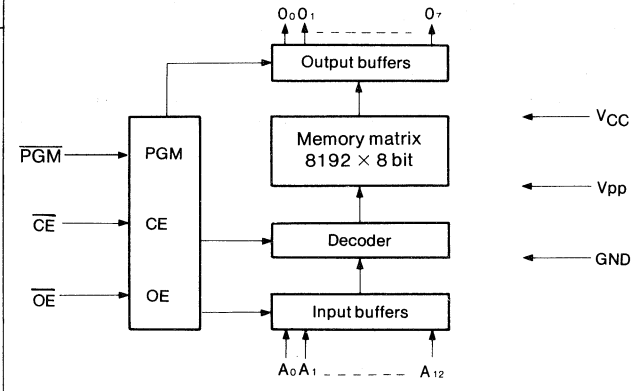
- +5V single power supply
- 8,192 words × 8-bit configuration
- Access time: MAX150 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND.

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

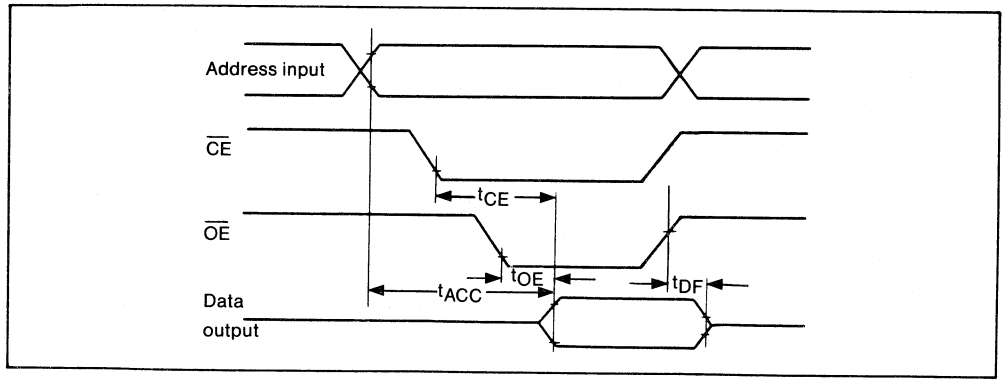
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	ns

TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

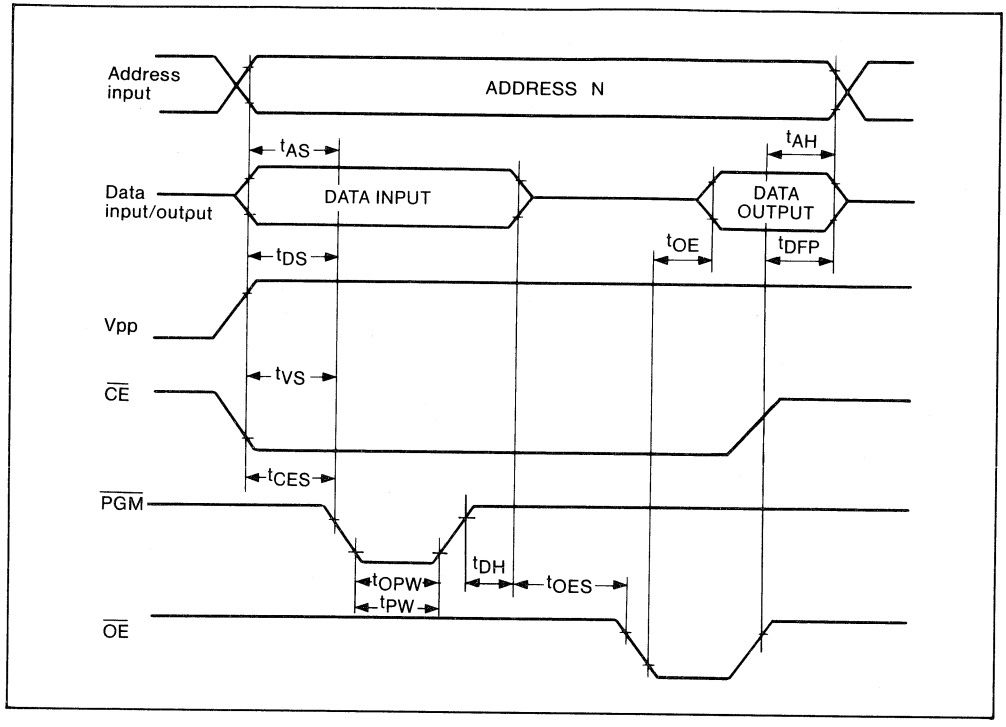
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART


Address input
ADDRESS N
tAS
tAH
Data input/output
DATA INPUT
DATA OUTPUT
tDS
tOE
tDFP
Vpp
tVS
CE
tCES
PGM
tDH
tOPW
tOES
tPW
OE

OKI semiconductor

MSM27128AZB-RS

16,384 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

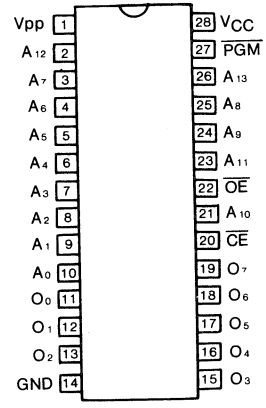
The MSM27128AZB is a 16,384 words × 8-bit electrically programmable read-only memory. The MSM27128AZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

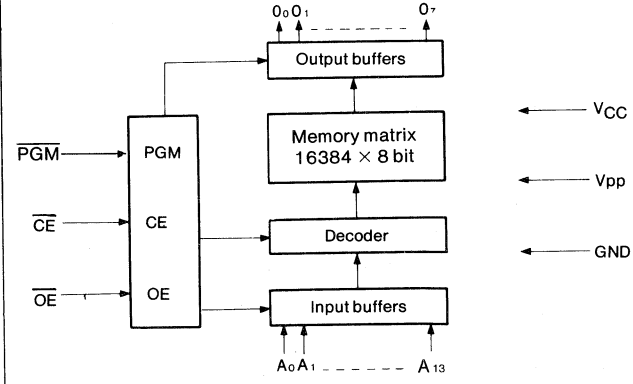
- +5V single power supply
- 16,384 words × 8-bit configuration
- Access time: MAX150 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL level
  (three state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND.

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

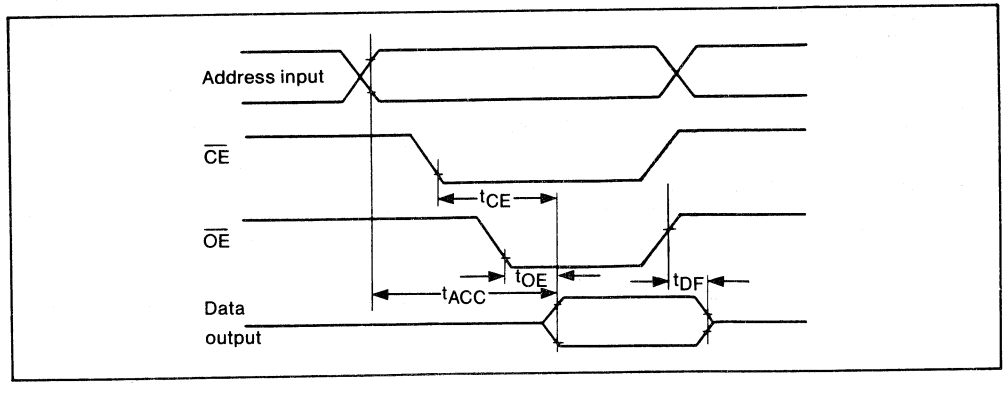
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	ns

TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

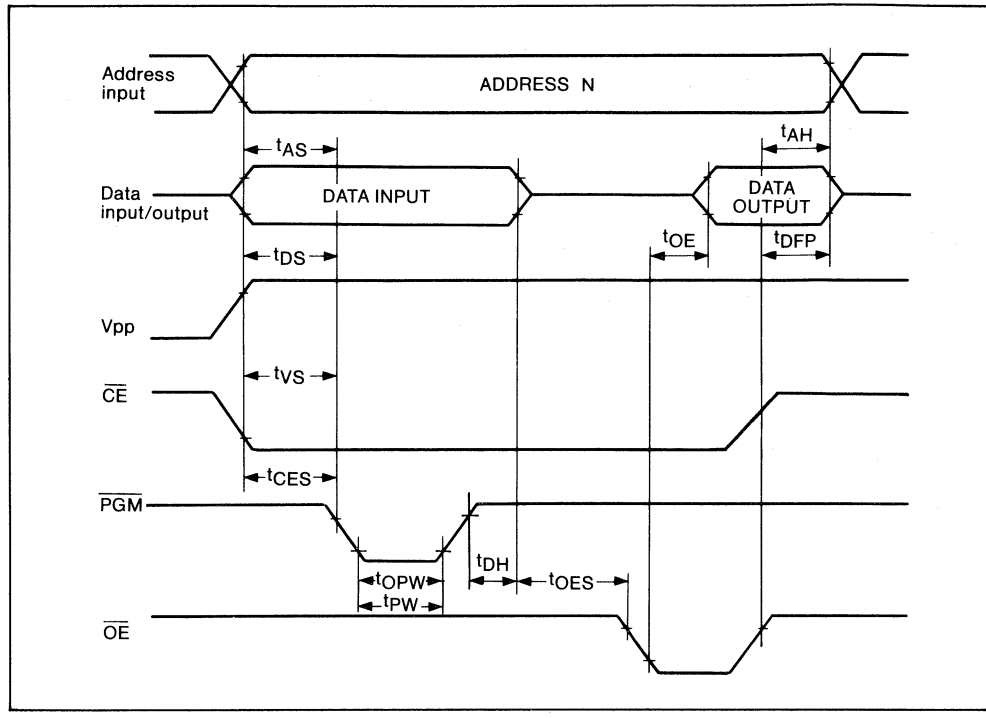
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART


Address input
ADDRESS N
tAS
tAH
Data input/output
DATA INPUT
DATA OUTPUT
tOE
tDFP
tDS
Vpp
tVS
CE
tCES
PGM
tDH
tOPW
tOES
tPW
OE

MSM27256ZB-RS

32,768 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

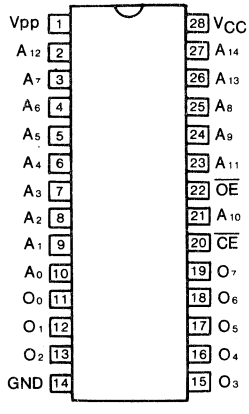
The MSM27256ZB is a 32,768 words × 8-bit electrically programmable read-only memory. The MSM27256ZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

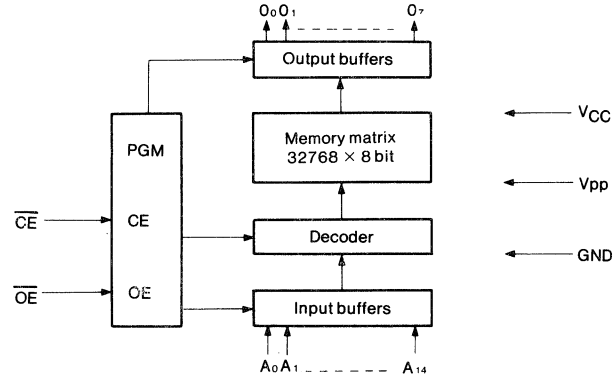
- +5V single power supply
- 32,768 words × 8-bit configuration
- Access time: MAX170 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

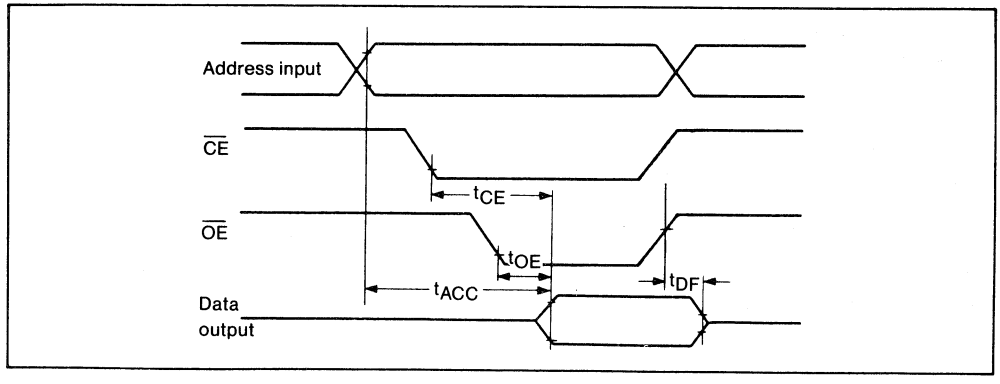
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	ns

TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

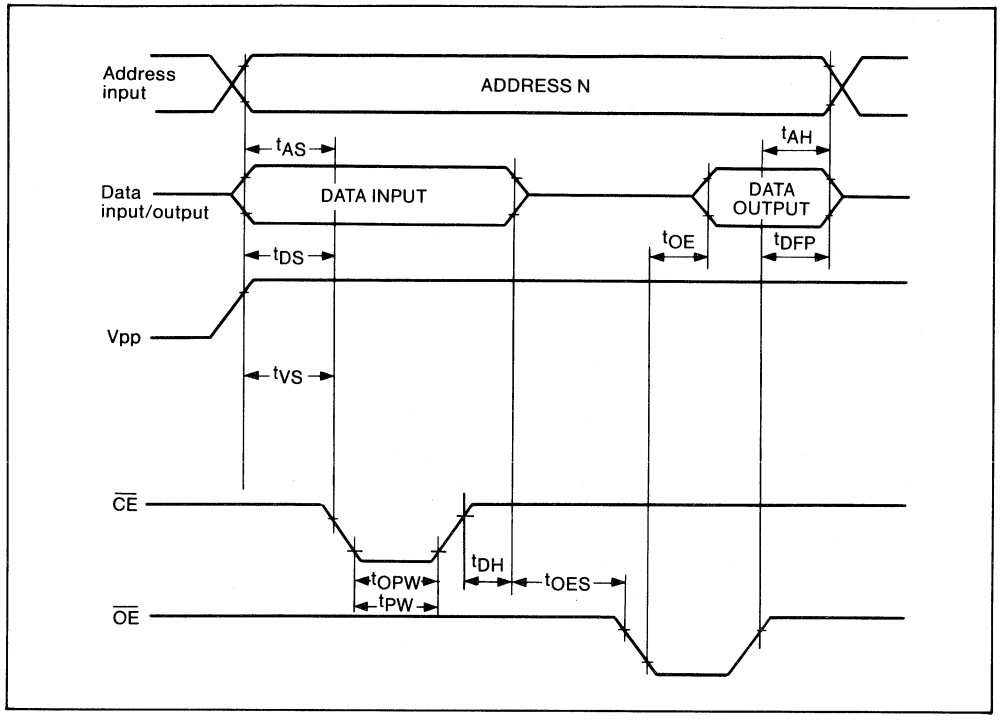
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART


Address input
ADDRESS N
tAS
tAH
Data input/output
DATA INPUT
DATA OUTPUT
tOE
tDFP
tDS
Vpp
tVS
CE
tDH
tOPW
tOES
tPW
OE

MSM27512ZB-RS

65,536 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

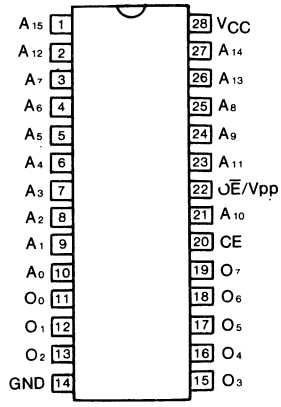
The MSM27512ZB is a 65,536 words × 8-bit electrically programmable read-only memory. The MSM27512ZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

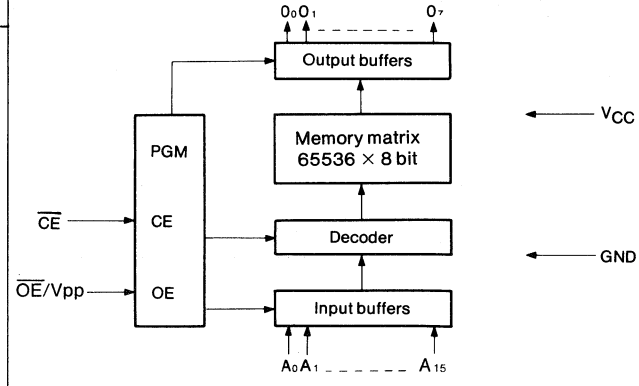
- +5V single power supply
- 65,536 words × 8-bit configuration
- Access time: MAX200 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	High impedance
Stand-by	V_{IH}	–	+5V	High impedance
Program	V_{IL}	12.5V	+6V	D_{IN}
Program Inhibit	V_{IH}	12.5V	+6V	High impedance

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

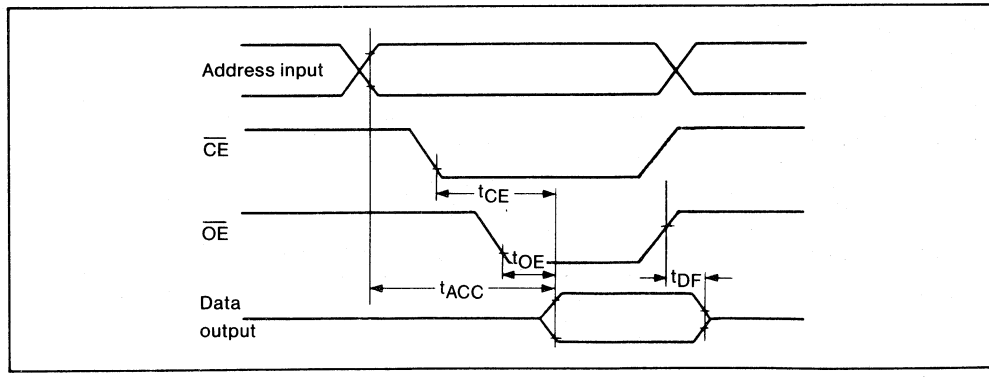
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	–0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = –400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	55	ns

TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

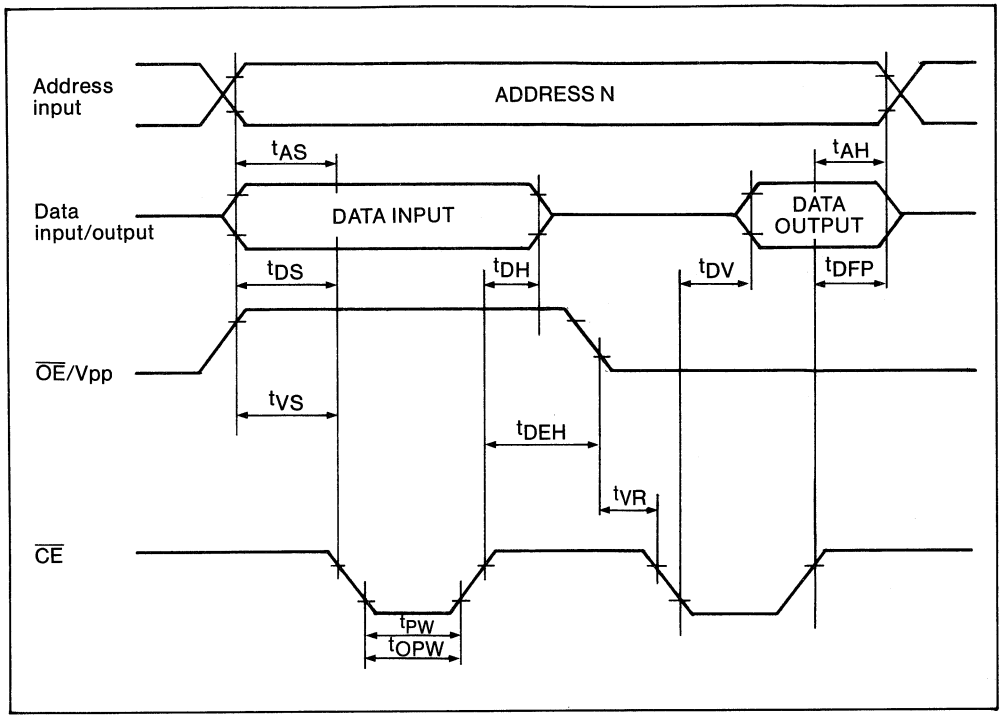
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$/Vpp Hold Time	t_{DEH}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{CE}$	t_{DV}	–	–	–	1	μs
$\overline{OE}$/Vpp Recovery Time	t_{VR}	–	2	–	–	μs

TIME CHART


Address input
ADDRESS N
tAS
tAH
Data input/output
DATA INPUT
DATA OUTPUT
tDS
tDH
tDV
tDFP
OE/Vpp
tVS
tDEH
tVR
CE
tPW
tOPW

MOS E^2 PROMS

8 MOS E^2 PROMS

MSM16811RS	1,024-Word x 1-Bit E^2 PROM	471
MSM16911RS	1,024-Word x 1-Bit E^2 PROM	478

MSM16811RS

1,024 BIT SERIAL EEPROM

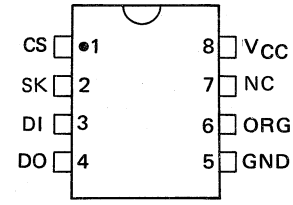
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with NS9346
- Self timed programming cycle
- Word and chip erasable
- Operating Range 0° C to 70° C

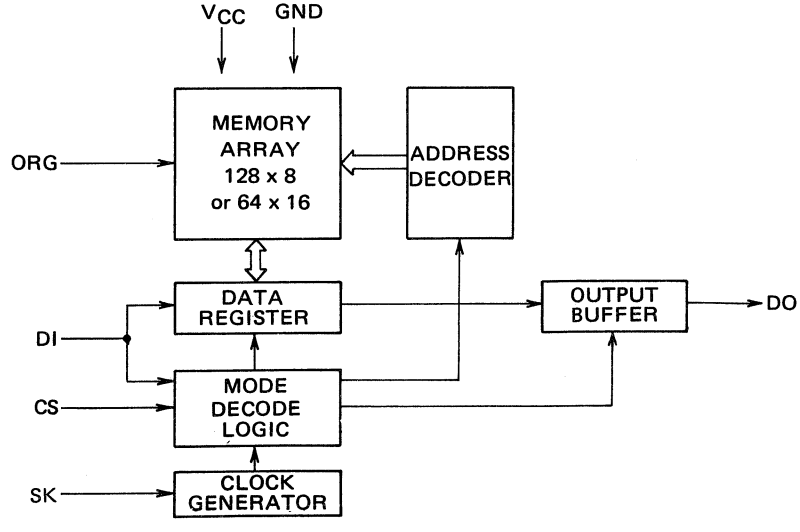
PIN CONFIGURATION

8 Pin Dual-In-Line

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	Non Connection		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0	A_6–A_0	A_5–A_0			Read Address A_N–A_0
ERASE	1	1 1	A_6–A_0	A_5–A_0			ERASE Address A_N–A_0
WRITE*	1	0 1	A_6–A_0	A_5–A_0	D_7–D_0	D_{15}–D_0	WRITE Address A_N–A_0
EWEN	1	0 0	11XXXXX	11XXXXX			Program Enable
EWDS	1	0 0	00XXXXX	00XXXXX			Program Disable
ERAL	1	0 0	10XXXXX	10XXXXX			Erase All Addresses
WRAL	1	0 0	01XXXXX	01XXXXX	D_7–D_0	D_{15}–D_0	Program All Addresses

*Write instruction is a self timed program instruction. The selected byte (word) gets erased before being written.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_i		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10 %	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

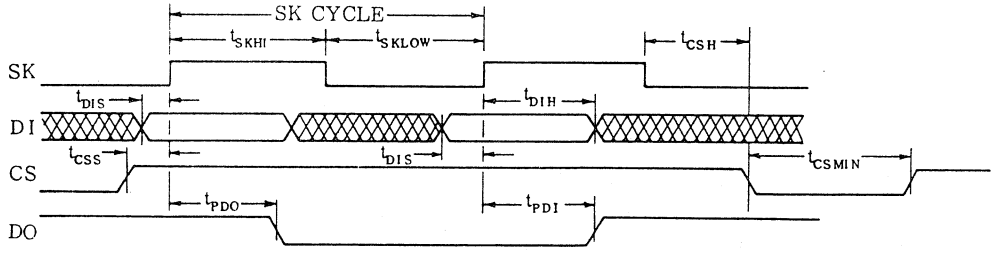
(V_{CC} = 4.5 V to 5.5 V, Ta = 0 ~ 70° C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.1		
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

Parameter	Description	Test Condition	Min	Typ	Max	Units
t_{CSS}	CS Setup Time		0.2			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIS}	DI Setup Time		0.4			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to 1	CL = 100pF			2	μs
t_{PD0}	Output Delay to 0	V_{OL} = 0.8V, V_{OH} = 2.0			2	μs
t_{HZ}	Output Delay to HiZ	V_{IL} = 0.45V, V_{IH} = 2.4			0.4	μs
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		1			μs
t_{SKHI}	Min SK High Time		1			μs
t_{SKLOW}	Min SK Low Time		1			μs
t_{SV}	Output Delay to Status Valid	C_L = 100 pF			1	μs
SK_{MAX}	Maximum Frequency		0		250	kHz



Synchronous Timings

8

DEVICE OPERATION

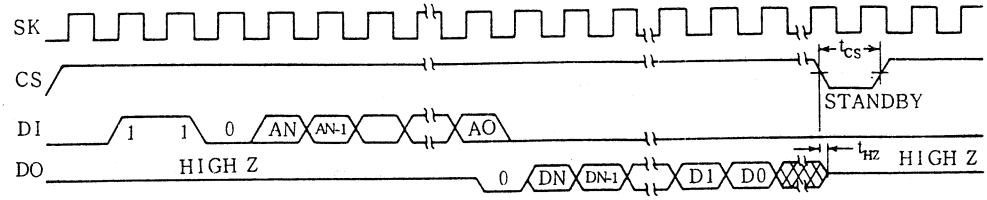
The MSM 16811 RS has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical '1', an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction has to be issued before starting to program.

At power-down, when V_{CC} falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

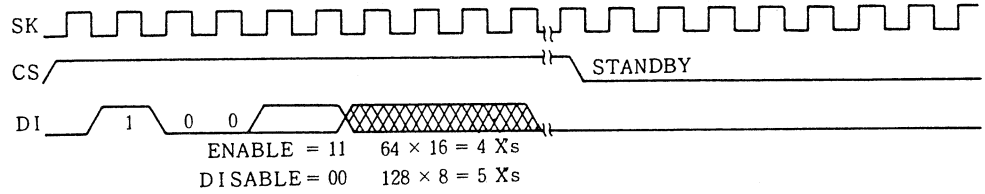
READ MODE



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

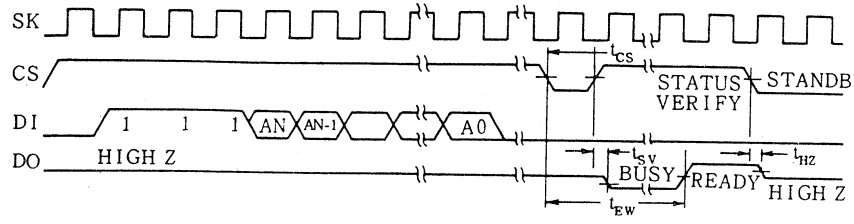
ERASE/WRITE ENABLE AND DISABLE



After power-up and before starting any programming instruction the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

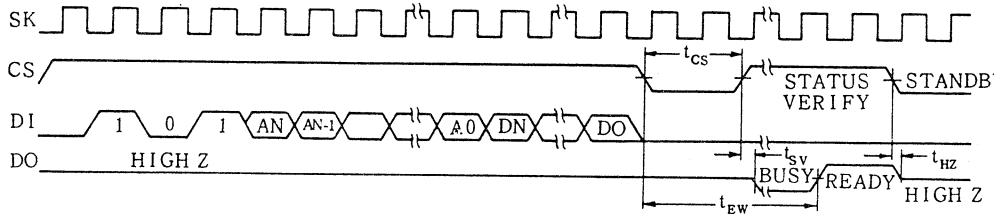
8

ERASE MODE



After an ERASE instruction has been shifted in. CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to a logical '1'.

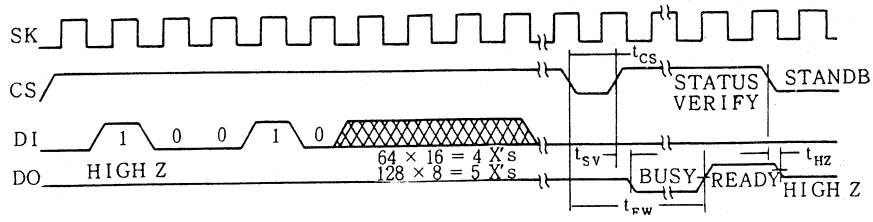
WRITE MODE



After a WRITE instruction has been shifted in with ite corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming sequence. The addressed register will first be erased and then the previously shifted data will be written in the register. If CS is brought high during the programming time (after observing the t_{CS} specification), the DO pin will act as a status indicator – it will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to their proper value.

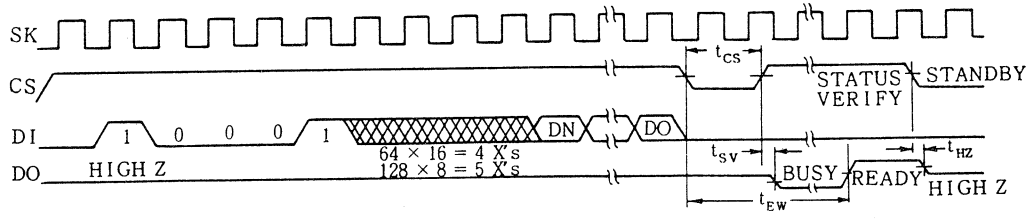
Configuration	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

ERASE ALL



This instruction is provided to erase the whole chip. Besides its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRITE ALL



This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. Besided its different opcode, the WRAL instruction is identical to the WRITE instruction.

8

OKI semiconductor

MSM16911RS

1,024 BIT SERIAL EEPROM

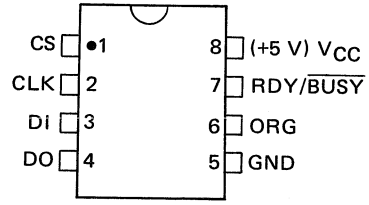
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with GI5911
- Self timed programming cycle
- Word and chip erasable
- Operating Range 0°C to 70°C

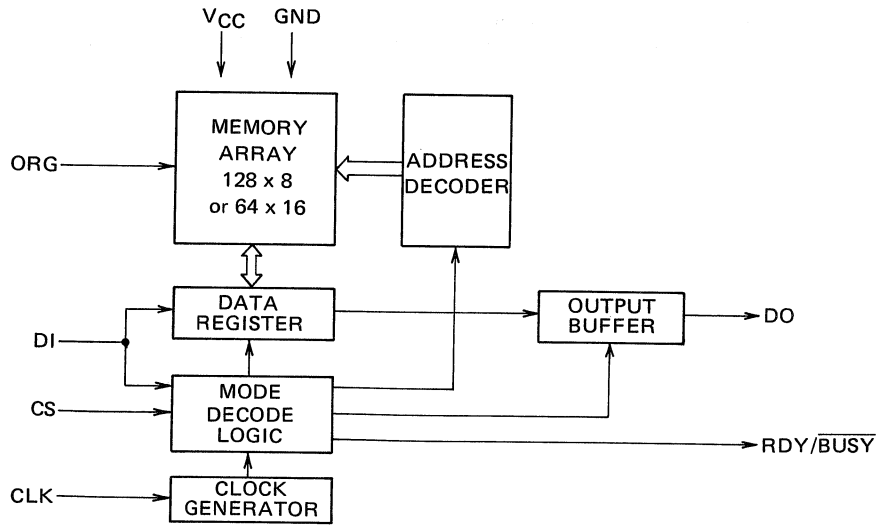
PIN CONFIGURATION

8 Pin Dual-In-Line

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
RDY/$\overline{BUSY}$	Status Output		
GND	Ground		

			INSTRUCTION SET				
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6-A_0	A_5-A_0			Read Address A_N-A_O
PROGRAM	1	x100	A_6-A_0	A_5-A_0	D_7-D_0	$D_{15}-D_0$	Program Address A_N-A_O
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	0 ~ 70	°C

DC CHARACTERISTICS

(V_{CC} = 4.5 V to 5.5 V, Ta = 0 ~ 70° C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.1		
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

(V_{CC} = 4.5 V to 5.5 V, Ta = 0 ~ 70°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	CLK Frequency	0		250	kHz	1
t_{CSS}	CS Setup Time with respect to CLK Falling	0.2			μs	
t_{CSH}	CS Hold Time with respect to CLK Rising	0			μs	
t_{DIST}	DI Setup Time with respect to CLK Rising	0.4			μs	
t_{DIH}	DI Hold Time with respect to CLK Rising	0.4			μs	
t_{CPH}	CLK Pulse High Time	1.0			μs	
t_{CPL}	CLK Pulse Low Time	1			μs	
t_{PD1}	Delay Time of DO Rising with respect to CLK Rising			2.0	μs	2
t_{PDO}	Delay Time of DO Falling with respect to CLK Rising			2.0	μs	2
t_P	"L" Time of Status (Programming Time)			10	ms	

Note: Condition: C_L = 100 pF and V_{OL}/OH = 0.8/2.0

Figure 1. Synchronous Data Timing

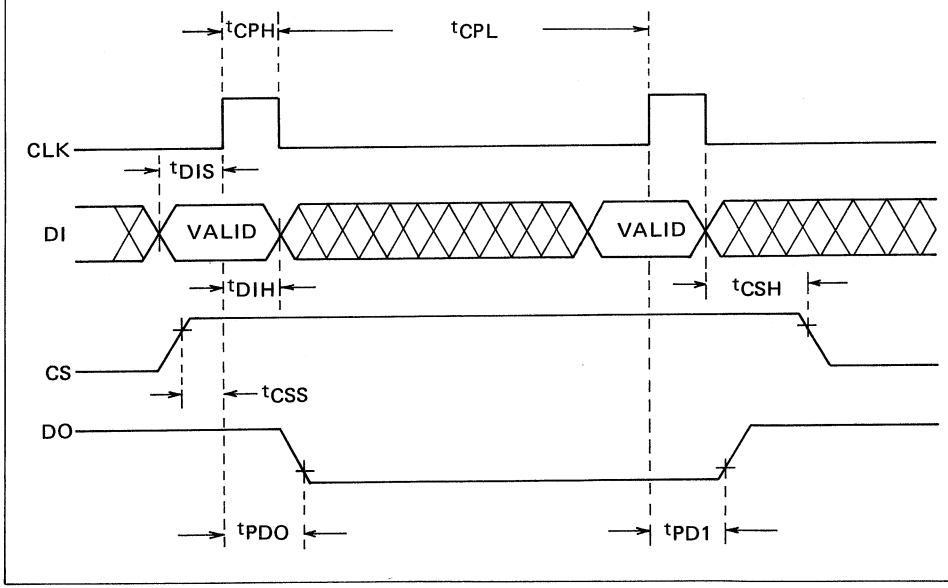
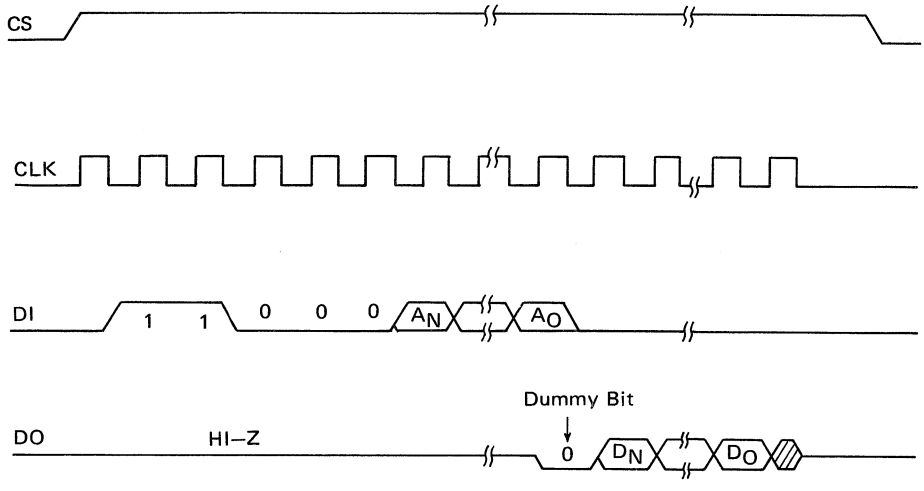


Figure 2. READ Mode

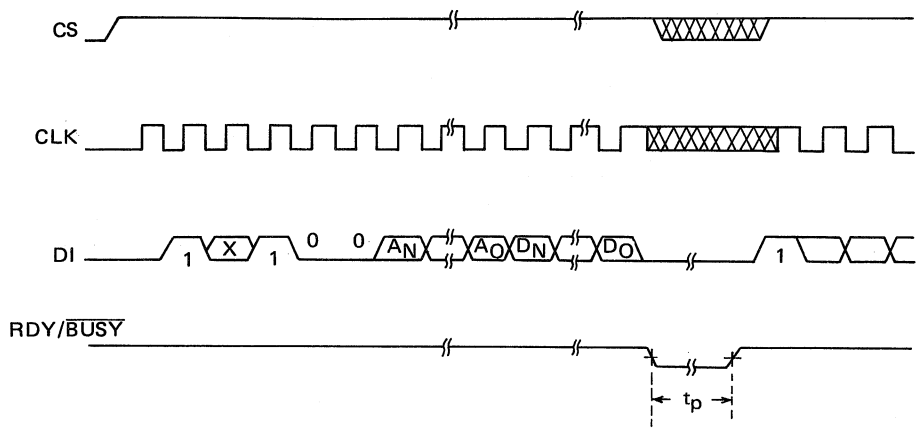


Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") procedes the data output string. The output data changes during the high states of the system clock.

Figure 3. PROGRAM Mode



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Program Mode

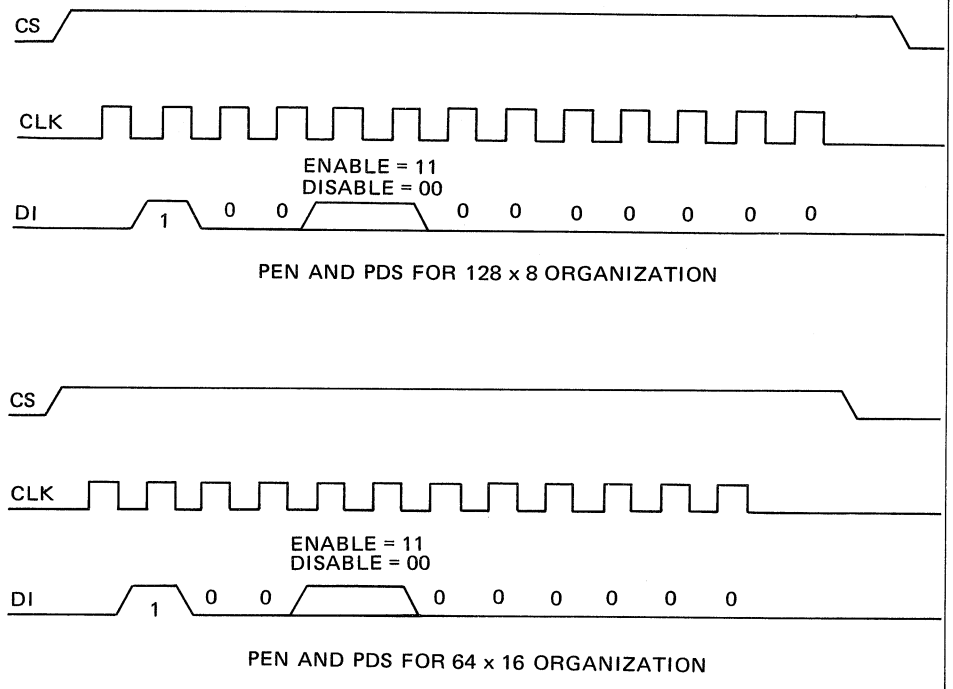
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

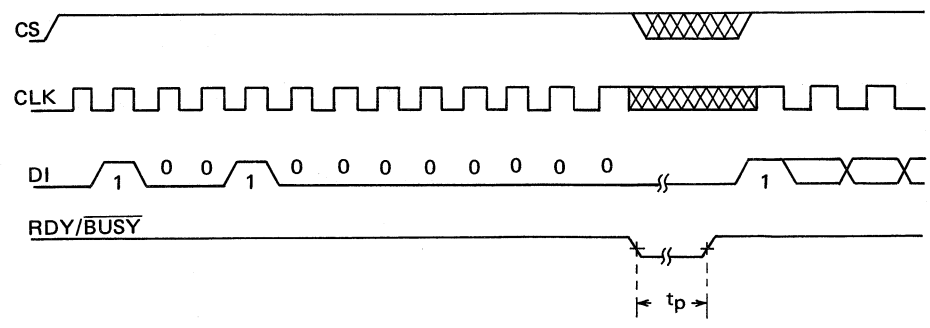
Figure 4. PEN (Program Enable) and PDS (Program Disable)



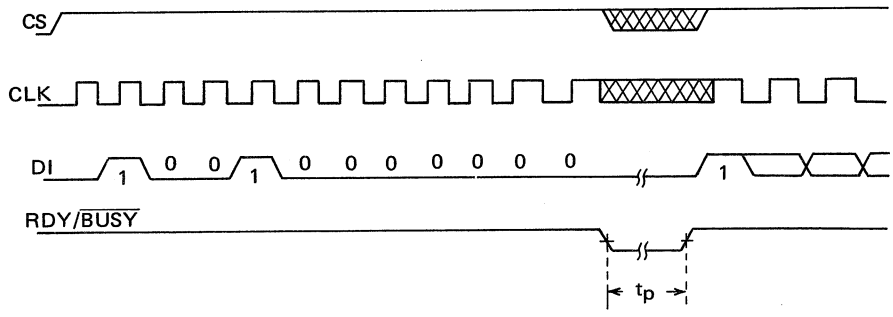
Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Figure 5. ERAL (Erase All) Mode (128 x 8)



ERAL (Erase All) Mode (64 x 16)



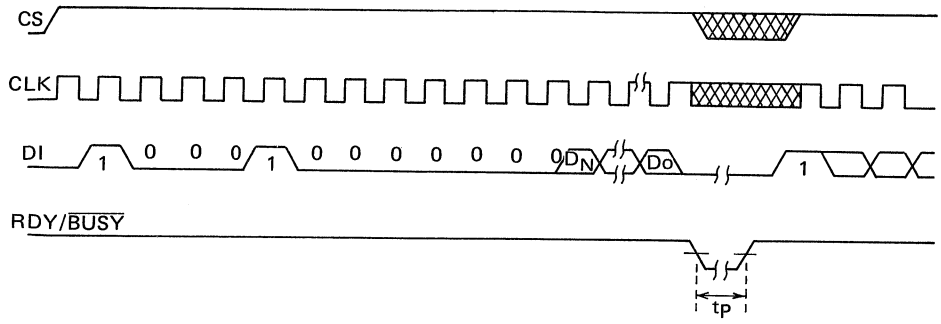
Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a "1"

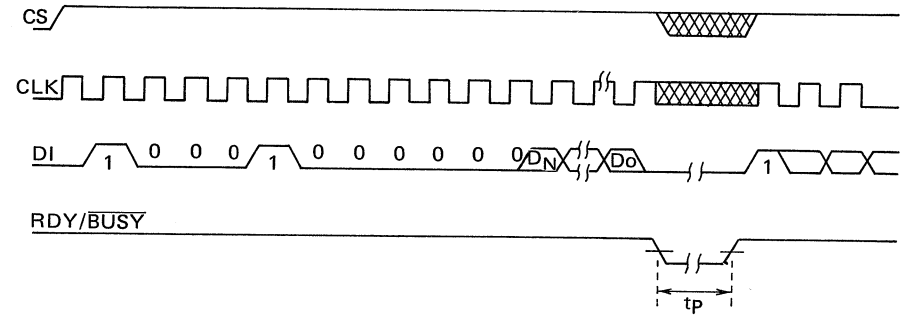
All specifications and details published are subject to change without notice.

Figure 6. WRITE ALL

WRAL (Write All) Mode (128 x 8)



WRAL (Write All) Mode (64 x 16)



	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Write All

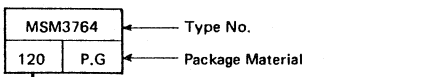
This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. After a WRAL instruction has been shifted in, the RDY/BUSY pin goes low and the self timed write sequence starts. The RDY/BUSY pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the array have been set to their proper value.

CROSS REFERENCE LIST

9 CROSS REFERENCE LIST

1. DYNAMIC RAM 489
2. STATIC RAM 493
3. MASK ROM 494
4. EPROM 495
5. E^2 PROM 497

(Note)



1. DYNAMIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	65536 x 1	16/18	MSM3764A-12	HM4864A-1		TMS4164A-12		MCM6665A-12	μPD4164A-4	TMM4164A-2	M5K4164A-12	MB8264A-12
				120 P.J	120 P.G		120 P.C		120 C	120 P.G.C	120 P	120 P.C	120 P.G
				MSM3764A-15	HM4864A-2		TMS4164A-15	MK4564	MCM6665A-15	μPD4164A-3	TMM4164A-3	M5K4164A-15	MB8264A-15
				150 P.J	150 P.G		150 P.C	150 P	150 C	150 P.G.C	150 P	150 P.C	150 P.G
NMOS	256k	262144 x 1	16/18						MCM6256-10				MB81256-10
									100 P.C				100 P
				MSM41256-12	HM50256-12		TMS4256-12	MK4556-12	MCM6256-12	μPD41256-12	TMM41256C-12	M5M4256S-12	MB81256-12
				120 P.J	120 P.G		120 P	120 P	120 P.C	120 P.G.C	120 P.G	120 P.C	120 P
				MSM41256-15	HM50256-15		TMS4256-15	MK4556-15	MCM6256-15	μPD41256-15	TMM41256C-15	MSM4256S-15	MB81256-15
				150 P.J	150 P.G		150 P	150 P	150 P.C	150 P.G.C	150 P.G	150 P.C	150 P
				MSM41256A-10					MCM6256-10				MB81256-10
				100 P.J					100 P.C				100 P
				MSM41256A-12	HM50256-12		TMS4256-12		MCM6256-12	μPD41256-12	TMM41256C-12	M5M4256S-12	MB81256-12
				120 P.J	120 P.G		120 P		120 P.C	120 P.G.C	120 P.G	120 P.C	120 P
				MSM41256A-15	HM50256-15		TMS4256-15		MCM6256-15	μPD41256-15	TMM41256C-15	MSM4256S-15	MB81256-15
				150 P.J	150 P.G		150 P		150 P.C	150 P.G.C	150 P.G	150 P.C	150 P
				MSM41257A-10						μPD41257-10			MB81257-10
				100 P.J						100 P.C			100 P.C
				MSM41257A-12	HM50257-12		TMS4257-12		MCM6257-12	μPD41257-12	TMM41257-12	M5M41257-12	MB81257-12
				120 P.J	120 P.C		120 P		120 P.C	120 P.C	120 P.C	120 P.C	120 P.C
				MSM41257A-15	HM50257-15		TMS4257-15		MCM6257-15	μPD41257-15	TMM41257-15	M5M41257-15	MB81257-15
				150 P.J	150 P.C		150 P		150 P.C	150 P.C	150 P.C	150 P.C	150 P.C

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	256k	65536 x 4	18	MSM41464-10 100 P,J	HM50464P-10 100 P,J					μPD41464C-10 100 P,J			MB81464-10 100 P,J
				MSM41464-12 120 P,J	HM50464P-12 120 P,J					μPD41464C-12 120 P,J	TMM41464P-12 120 P,J		MB81464-12 120 P,J
				MSM41464-15 150 P,J	HM50464P-15 150 P,J					μPD41464C-15 150 P,J	TMM41464P-15 150 P,J		MB81464-15 150 P,J
	1M	1048576 x 1	18	MSM411000 100 P						μPD411000 100 P			
				MSM411000 120 P						μPD411000 120 P			MB81100 120 P
				MSM411001 100 P									
				MSM411001 120 P									MB811001 120 P
		262144 x 4	20	MSM414256-10 100 P									
				MSM414256-12 120 P									
		1048576 x 1	18	MSM511000-10 100 P	HM511000-10 100 P		TMS4C1024-10 100 P				TC511000-10 100 P	M5M4C1000-10 100 P	MB81C1000-10 100 P
				MSM511000-12 120 P	HM511000-12 120 P		TMS4C1024-12 120 P				TC511000-12 120 P	M5M4C1000-12 120 P	MB81C1000-12 120 P
				MSM511001-10 100 P			TMS4C1025-10 100 P				TC511001-10 100 P	M5M4C1001-10 100 P	MB81C1001-10 100 P
				MSM511001-12 120 P	HM511001-12 120 P		TMS4C1025-12 120 P				TC511001-12 120 P	M5M4C1001-12 120 P	MB81C1001-12 120 P

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	1M	1048576 x 1	18	MSM511002-10	HM511002-10		TMS4C1027-10				TC511002-10	M5M4C1002-10	MB81C1002-10
				100 P	100 P		100 P				100 P	100 P	100 P
				MSM511002-12	HM511002-12		TMS4C1027-12				TC511002-12	M5M4C1002-12	MB81C1002-12
				120 P	120 P		120 P				120 P	120 P	120 P
		262144 x 4	20	MSM514256-10	HM514256-10						TC514256-10	M5M44C256-10	MB81C4256-10
				100 P	100 P						100 P	100 P	100 P
				MSM514256-12	HM514256-12						TC514256-12	M5M44C256-12	MB81C4256-12
				120 P	120 P						120 P	120 P	120 P
				MSM514258-10	HM514258-10						TC514258-10	M5M44C258-10	MB81C4258-10
				100 P	100 P						100 P	100 P	100 P
				MSM514258-12	HM514258-12						TC514258-12	M5M44C258-12	MB81C4258-12
				120 P	120 P						120 P	120 P	120 P
	2048k	262,144 x 8	30	MSC2304-10									
				100 YS.KS									
				MSC2304-12									
				120 YS.KS									
				MSC2304-15									
				150 YS.KS									
	2304k	262,144 x 9	30	MSC2304-10									
				100 YS.KS									
				MSC2304-12	HM561003-12							MH25609-12	
				120 YS.KS	120 YS.KS							120 YS	
				MSC2304-15	HM561003-15							MH25609-15	
				150 YS.KS	150 YS.KS							150 YS	

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	9216k	524,288 x 9	30	MSC2305-10 100 YS									
				MSC2305-12 120 YS									
				MSC2305-15 150 YS									
	2048k	262,144 x 8	30	MSC2307-10 100 YS.KS									
				MSC2307-12 120 YS.KS									
				MSC2307-15 150 YS.KS									
	2304k	262,144 x 9	30	MSC2307-10 100 YS.KS									
				MSC2307-12 120 YS.KS									
				MSC2307-15 150 YS.KS									
	8M	1048,576 x 8	30	MSC2311-10 100 YS.KS									
				MSC2311-12 120 YS.KS									
	9M	1048,576 x 9	30	MSC2310-10 100 YS.KS									
				MSC2310-12 120 YS.KS									

2. STATIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	64k	8192 x 8	28	MSM5165-12	HM6264-12							M5M5165-12	
				120 P	120 P							120 P	
				MSM5165-15	HM6264-15					μPD4364-15	TC5565-1		MB8464-15
				150 P	150 P					150 P	150 P		150 P
				MSM5165-20						μPD4364-20			
				200 P						200 P			
		16384 x 4	22	MSM5188-45						μPD4362-45			
				45 P						45 P			
				MSM5188-55						μPD4362-55			
				55 P						55 P			
				MSM5188-70						μPD4362-70			
				70 P						70 P			
	256k	32768 x 8	28/30	MSM51257-85									
				85 P.J									
				MSM51257-10									
				100 P.J									
				MSM51257-12									
				120 P.J									

3. MASK ROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	8192 x 8	28	MSM3864 250 P		2364A 450 P.G				μPD2364 450 P.G	TMM2364 250 P		
	128k	16384 x 8	28	MSM38128A 250 P							TMM23128 200 P		
NMOS	256k	32768 x 8	28	MSM38256 250 P				MK38000 250 P.G				M5M23256 250 P	
				MSM38256A 150 P									
CMOS	256k	32768 x 8	28	MSM53256 150 P									
	1M	131072 x 8	28	MSM531000 250 P									

4. EPROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	8192 x 8	28	MSM2764A-20	HN482764G-20	D2764-2				μPD2764D 2	TMM2764D-2		MBM2764-20
				200 G	200 G	200 G				200 G	200 G		200 G
				MSM2764A-25	HN482764G	D2764				μPD2764D	TMM2764D		MBM2764 25
				250 G	250 G	250 G				250 G	250 G		250 G
				MSM2764A-30	HN482764G 30	D2764-3				μPD2764D-3			MEM2764-30
				300 G	300 G	300 G				300 G			300 G
						D2764A						TMM2764AP	
						G						G	
						P2764A						TMM2764AP	
						250 P						200 P	
	128k	16384 x 8	28	MSM27128A-20						μPD27128D-2	TMM27128D-20	M5L27128K-2	
				200 G						200 G	200 G	200 G	
				MSM27128A-25	HN4827128G-25	D27128				μPD27128D	TMM27128D-25	M5L27128K (-1)	MBM27128-25
				250 G	250 G	250 G				250 G	250 G	250 G	250 G
				MSM27128A-30	HN4827128G-30	D27128-3				μPD27128D-3		M5L27128K-3	MBM27128-30
				300 G	300 G	300 G				300 G		300 G	300 G
						D27128A					TMM27128AD		MBM27128A
						G					G		200 G
						P27128A					TMM24128AP		
						250 P					200 P		

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	256k	32768 x 8	28	MSM27256-15 150 G							TMM27256D-15 150 G		
				MSM27256-20 200 G							TMM27256AD-20 200 G	M5L27256K-2 200 G	MBM27256-20 200 G
						P27256 250 P					TMM24256AP 200 P		
				MSM27256-25 250 G	HN27256G-25 250 G	27256 250 G						M5L27256K 250 G	MBM27256-25 250 G
										μPD27256D 200 G	TMM27256D 150 G		
	512k	65536 x 8	28	MSM27512-15 150 G									
				MSM27512-20 200 G								M5L27512K-2 200 G	
				MSM27512-25 250 G	HN27512G-25 250 G	27512 250 G						M5L27512K 200 G	MBM27512-25 250 G
	1M	131072 x 8	32	MSM271000-12 120 G									
				MSM271000-15 150 G									
				MSM271000-20 200 G		27010-200V05 200 G							

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	1M	65536 x 16	40	MSM271024-12 120 G									
				MSM271024-15 150 G		27210-150/05 150 G							
						27210-170/05 170 G							
				MSM271024-20 200 G		27210-200/05 200 G							

5. EEP ROM

Structure	Total Bit	Organization	Number of Pin	Oki	NS	GI	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	1,024	64 x 16 or 128 x 8	8	MSM16811 – P	NS9346 – P								
				MSM16911 – P		G15911 – P							

APPLICATIONS

10 APPLICATIONS

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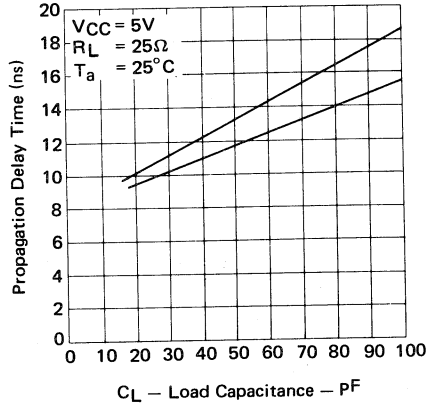
64K 256K BIT DYNAMIC RAM APPLICATION NOTES

1. MEMORY DRIVER

There are problems in driving MOS ICs by a TTL driver: increase of driver delay time due to capacitive load and ringing waveform at the falling edge.
An example of the increase of delay time due to capacitive load is shown in the following figure.
The number of load memory elements must be taken into consideration when designing the timing.

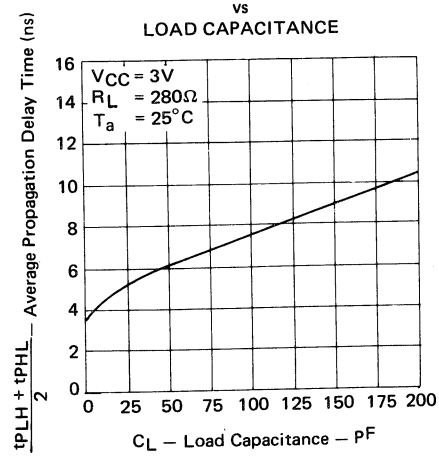
In case of LS type

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE



In case of L type

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE



- If the number of load memory elements is 20 ~ 40 (150 ~ 300pF) on a two layer board, an undershoot of −2 to −3V (peak voltage) occurs. Therefore, measures against ringing must be taken as described in the following.

- Measures against ringing
  (1) No consideration is required for the rising edge since there is a margin.
  (2) Since ringing may be considered as a reflection due to mismatching between the driver output impedance and signal line impedance, it can be prevented by line matching (termination).
  For memory arrays, however, termination with pull up or bleeder resistance is not effective. Instead, series resistance (damping resistance) is suitable for memory arrays.
  (3) The optimal value of series resistance differs depending upon the speed, pattern status, and driver. Experience will help in determining the optimal series resistance.
  As a general rule, a resistance of 10 ~ 100Ω is suitable.
  However the speed will be lowered if the resistance is too large. An example is shown in attached drawing 3.
  (4) Make the signal lines as short as possible. Multilayer board design is effective in reducing the undershoot (as the signal line impedance is lowered).

2. DECOUPLING CAPACITORS

The dynamic MOS RAM is featured by the great power current at the active time in comparison to that at the standby time.
For example, the rated value (Icc1) of the mean power current of the MSM3764 is 45mA, while the standby current (Icc2) of the MSM3764-15 (150ns version) is 5mA. The former is approximately 10 times greater than the latter. The peak current of the MSM3764 approaches 90mA in the worst case. It is approximately 20 times as great as the standby current Icc2.
Therefore, the power circuit must be designed so as to prevent the above current variation from causing an erroneous operation of the memory. A by-pass capacitor must be inserted for this purpose. There are two types of by-pass capacitors: high frequency capacitor and low frequency capacitor.

2.1 High Frequency Capacitor

In the Icc current waveform, the peak current rises at a high speed such as 10ns, and a high frequency noise represented by the following expression is caused to occur by the L component of the current applied to the capacitor:

$$\triangle V = L\frac{\triangle i}{\triangle t}$$

To reduce the fluctuation $\triangle V$, the value of L must be reduced.
For this purpose, the capacitor must be placed as close as possible to the power pin of the IC. Further, sufficient capacity for supplying the peak current is required. The standard capacity for a double sided circuit board (two layer circuit board) is $0.05 \sim 0.1\mu F$ or more. The capacity may be less than this value for a multi layer circuit board since the L component is less than the former.
When designing a board, mount one capacitor with excellent high frequency characteristics for every two or three MOS IC memory chips, near the power pins of these IC chips.

2.2 Low Frequency Capacitor

A low frequency capacitor is required for suppressing the power fluctuation due to a sudden current variation (for example, current variation caused by a status change from the standby status to the continuous access status or concurrent refreshment of the entire board) in a board unit. The power fluctuation in this case is a slow variation of several handred ns.
For this reason, the low frequency capacitor must have a capacity larger than the high frequency capacitor.
Though the capacity requirement depends upon the number of memories which operate simultaneously (bit width), $50\mu F$ is enough for a 16 ~ 32 bit system in a practical use.
As an example of capacitor which satisfies the requirements in both 2.1 and 2.2 above, a small-sized tantalum capacitor with excellent high frequency characteristics is shown in the following table. It is desirable to mount a low frequency capacitor near the power input pin in order to suppress the fluctuation of power supplied from outside, even if this capacitor is mounted.

Manufacturer	Model	Capacity (μF)
Oki Ceramic Co.	Model CA tantalum capacitor Model CB	$0.1 \sim 20\mu F$

The frequency characteristics of the above capacitor and the power bus bar are illustrated in attached figure 1.

3. PRINTED CIRCUIT BOARD

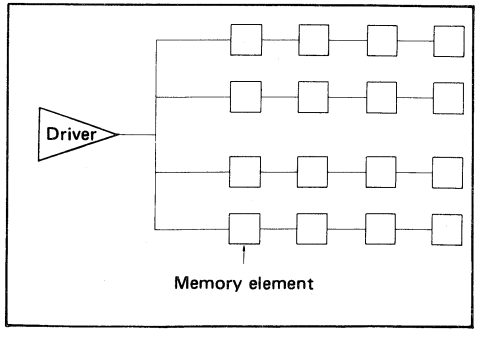
3.1 Number of Layers

Considering the measures against power noise which was described in 2. above and the routing to be described in 3.2, two layers are enough in principle.

3.2 Routing

An example of routing on a two-layer circuit board is shown in attached drawing 2. In designing the routing, note the following four points:

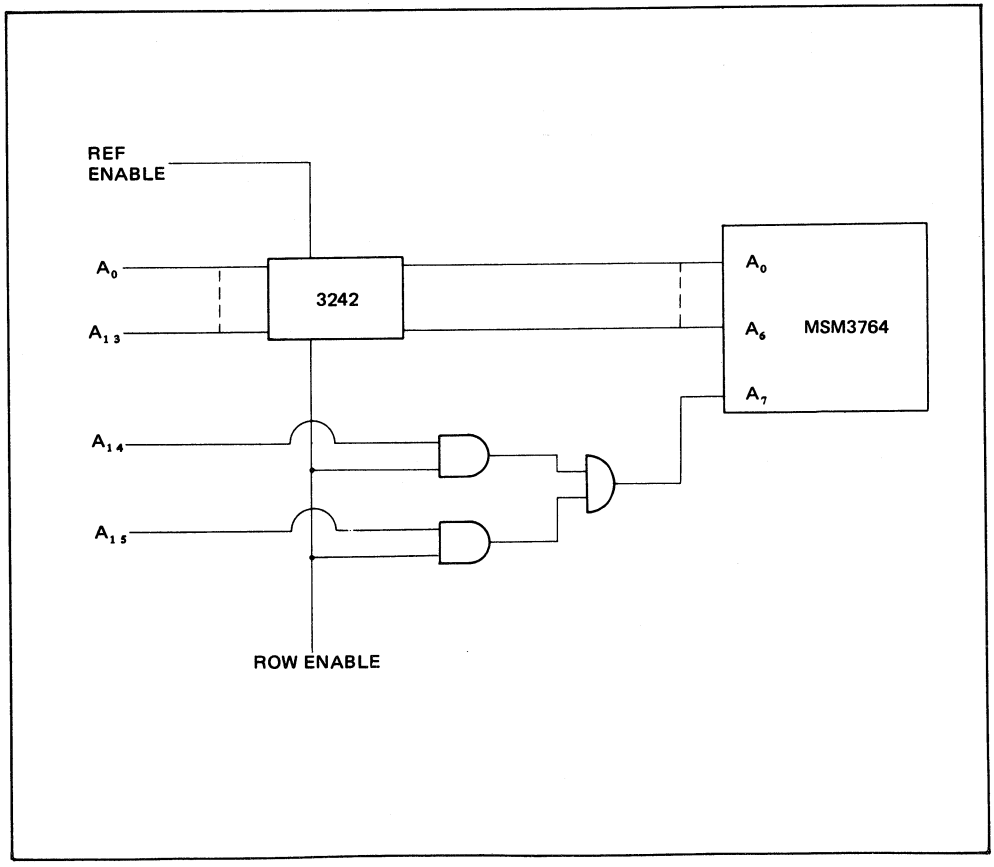
(I) The MOS drive line based on the TTL must be as short as possible to prevent ringing (reflection) and reduce crosstalk.
(II) Considerations are required to lower the impedance of the power line (including the ground). (For example, make a solid or grid-formed power line pattern. It is desirable that the power line pattern has width of at least 1.27mm.)
(III) If a signal line is to be branched for multi drive, the line must be branched at the driving end. (See the following figure.) And, the memory matrix must be designed in an integrated form, and peripheral drivers must be placed near the memory matrix.



4. PERIPHERAL CONTROL CIRCUIT

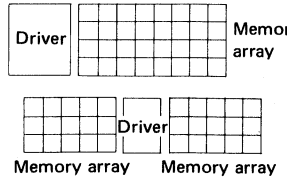
The three types of dynamic RAM control ICs shown in the following table are available at present.

Manufacturer	Model	Functions
Intel	i-3242	○ Seven-bit address multiplexer (for 16K bit dynamic RAM) ○ Seven-bit refresh address count function ○ Direct dirving capability of memory elements (for approx. 20 elements. 250 pF/25 ns 15 pF/9 ns) ○ Application to a 64K bit dynamic RAM, example (see the following figure)
Motorola	MC-3242	
Texas Instruments (T. I)	74LS601 603	○ Refresh timer using an RC multivibrator ○ Timing generation ○ Refresh address (7-bit address)
Advanced Micro Device (AMD)	Am2964A	○ Address latch/multiplex function (16-bit address) ○ Refresh address counter ○ $\overline{RAS}$ decoder (2 ~ 4)
Intel	i-8203	○ 8-bit address multiplexer (for 16K/64K DRAM) ○ Direct dring capability of memory element ○ Including timing control



5. NOTES ON MOUNTING 1 MB MEMORY ON A BOARD

The advent of a 64K bit dynamic RAM such as the MSM3764 has made it extremely easy to mount 1 MB memory on a board from the viewpoint of mounting space. In this case, however, note the following points since the number of memory elements mounted is so large as 128 ~ 176 (when redundant bits are provided).

<table>
<tr><th>Point to be noted</th><th>Consideration</th><th>Practical example</th></tr>
<tr><td>Mounting of memory elements</td><td>Memory elements may be integrated or divided.
(Design the memory array(s) to make the drive lines shortest.)</td><td> 
</td></tr>
<tr><td>Memory element driving method</td><td>Take care about the delay time and undershoot noise of the drive element.
(If the condition $V_{ILmin} = -1V$ recommended for the MOS dynamic RAM operation is satisfied, the memory elements will display the full reliability.)</td><td>Drive element
<table>
<tr><th>Parameter / Element</th><th>Delay time</th><th>(mA) IOL</th><th>Noise</th></tr>
<tr><td>7404</td><td>Medium speed</td><td>16</td><td>○</td></tr>
<tr><td>74S04</td><td>High speed</td><td>20</td><td>X</td></tr>
</table></td></tr>
<tr><td rowspan="3">Measures against noise</td><td>○ Two layers are enough for a board.
(Pay attention to the power line pattern.)</td><td></td></tr>
<tr><td>○ High frequency noise</td><td>Mount a 0.1 ~ 1 μF capacitor for every two memory elements.</td></tr>
<tr><td>○ Low frequency noise</td><td>Mount a tantalum capacitor etc. of 50 μF or more near the power input pin of the memory package.</td></tr>
<tr><td rowspan="2">Timing design</td><td>○ Prevent skew between each timing in order to enhance the system access speed.</td><td>Use ICs of the same tipe for racing timing (for example, $\overline{RAS}$ or $\overline{CAS}$).</td></tr>
<tr><td>○ Make a sufficient margin in timing design.</td><td>Skew and mounting delay</td></tr>
<tr><td>Thermal design</td><td>Thermal design under the worst condition is required.</td><td>Operation at a case temperature of 70°C must be guaranteed.</td></tr>
</table>

6. MEMORY SYSTEM RELIABILITY

6.1 Reliability Determination Factors

The memory system reliability depends upon the four factors shown in the left column of the following table. These factors are determined as shown in the right column of this table.

Memory system reliability factor	Factor determination
System-required reliability	Determined by the user-required specifications (MTBF).
Unit capacity	α [MB] = [word depth] x [bit count]
Parts reliability	Logic element ——— Hard error Memory element ——— Soft error
Cost	

6.2 Hard Error and Soft Error

(I) Hard error

A hard error is a permanent error which occurs each time a certain address is accessed.

(II) Soft error

A soft error is a transient error that does not repeat. The following are the three causes for soft errors:

(1) Insufficient power margin
(2) Insufficient system noise margin
(3) Particle failure
(4) Insufficient power margin
(5) Insufficient system noise margin
(6) particle failure

Items (1) through (5) are largely influenced by the system design. For item (6), it is required to consider whether a remedy such as ECC should be taken or not to satisfy the system-required reliability based on the parts reliability (pertaining to hard errors and soft errors). See 1.3 and 1.4 for details.

6.3 Measures for Reliability Enhancement

The following are the two typical means for the enhancement of system reliability.

(1) Parity..... Error detection only (makes no contribution to the MTBF enhancement)
(2) ECC..... The SEC-DED* is used in general

*Single Error Correct – Double Error Detect
(one bit error correction and two bit error detection)

6.4 Reliability Calculation Method

MTBF for a hard error and a soft error

(1) Memory element reliability

Hard error $r_H = e^{-\lambda_H \cdot t}$ (λ_H: Hard error rate)
Soft error $r_S = e^{-\lambda_S \cdot t}$ (λ_S: Soft error rate)

Reliability

$$R = \underbrace{(r_H)^n}_{①} + \underbrace{nC_1 \cdot (r_H \cdot r_S)^{n-1} \cdot (1 - r_H)}_{②}$$

① Probability of no hard error
② Probability of one bit hard error followed by no hard or soft error

Find a value for t when the value of R is e^{-1}.
The following calculations are based on the assumption that there is a low probability of two bit soft error occurrence.

(2) Memory unit reliability

Assume a memory unit whose size is n bits in bit width and k blocks in address capacity. The memory element reliability is expressed as follows:

$$r = e^{-\lambda t}$$ (λ: error rate)

① One bit correction

Find a value for t which satisfies the following expression:

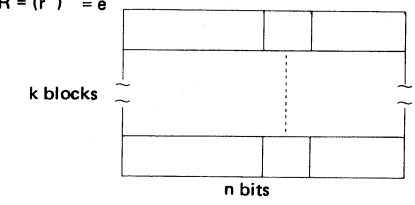
$$R = \left\{ \underbrace{(r)^n}_{①} + \underbrace{nC_1 \cdot r^{n-1}(1 - r)}_{②} \right\}^k = e^{-1}$$

① Probability of all bits being correct
② Probability of error occurrence for only one bit

② Only parity error detection without bit correction

Find a value for t which satisfies the following expression:

$$R = (r^n)^k = e^{-1}$$



6.5 Reliability Calculation Result Example

(1) Comparison of 64k byte, 128k byte, and 256k byte configurations (without ECC)

① 64kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	11.5
16k	100	200	10.6
		100	15.9
		50	21.1
	50	200	12.7
		100	21.1
		50	31.7

10

② 128kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	5.8
16k	100	200	5.3
		100	7.9
		50	10.6
	50	200	6.3
		100	10.6
		50	15.9

③ 256kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	2.9
16k	100	200	2.6
		100	4.0
		50	5.3
	50	200	3.2
		100	5.3
		50	7.9

Notes: 1. The bit width is 9 bits for each case.
2. 1 bit is used for parity error detection.

(2) Comparison of 1M byte configurations (with ECC)

Element	λH (Fit)	λS (Fit)	Reliability (years)	
			Bit width: 22 bits	Bit width: 39 bits
64k	100 (100%)	1000	8.2 (0.76)	7.9 (0.79)
	100 (50% 50%)	1000	13.9 (0.76)	14.5 (0.79)
16k	100 (100%)	100	8.3 (1.05)	6.8 (1.08)
	100 (50% 50%)	100	13.0 (1.05)	10.7 (1.08)

Notes: 1. When the bit width is 22 bits, six bits are used for the ECC.
2. When the bit width is 39 bits, seven bits are used for the ECC.
3. Values in parentheses are the reliabilities in the case of parity error detection without ECC.
4. The (50%, 50%) in the λH column means that 50% of the hard error rate λH is handled as the total bit hard error rate and the remaining 50% is handled as the one bit hard error rate (which reflects the hard error mode analysis result confirmed so far).

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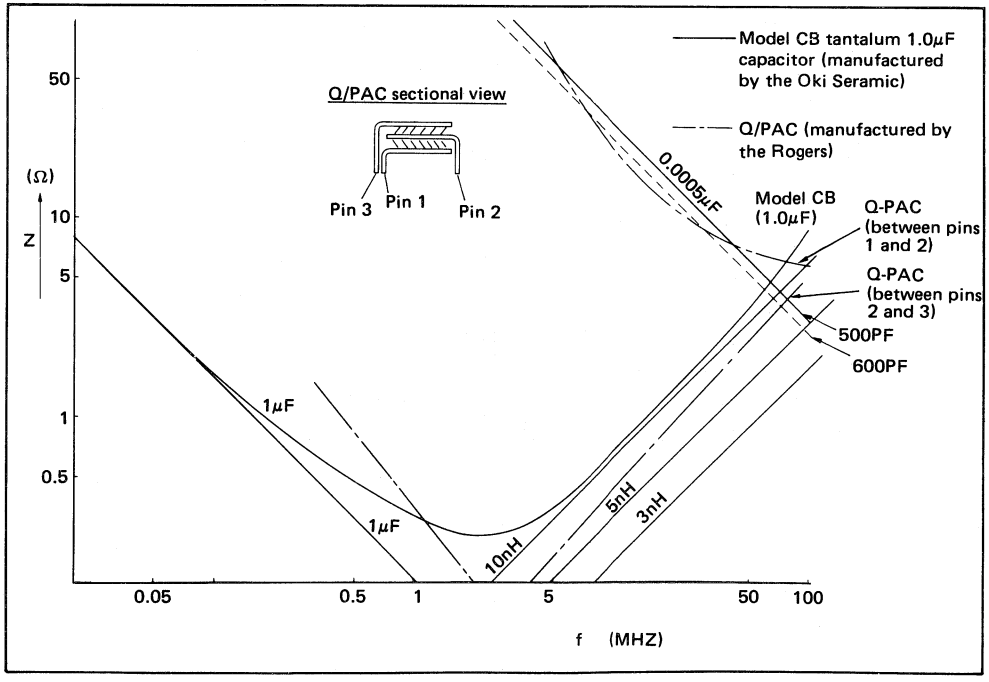
7. MEMORY COMPARISON STANDARD

In general, power, speed, and usability are required for memory elements. At present, 64K bit dynamic RAMs can be supplied by a lot of manufacturers, and these elements have almost unified specifications.

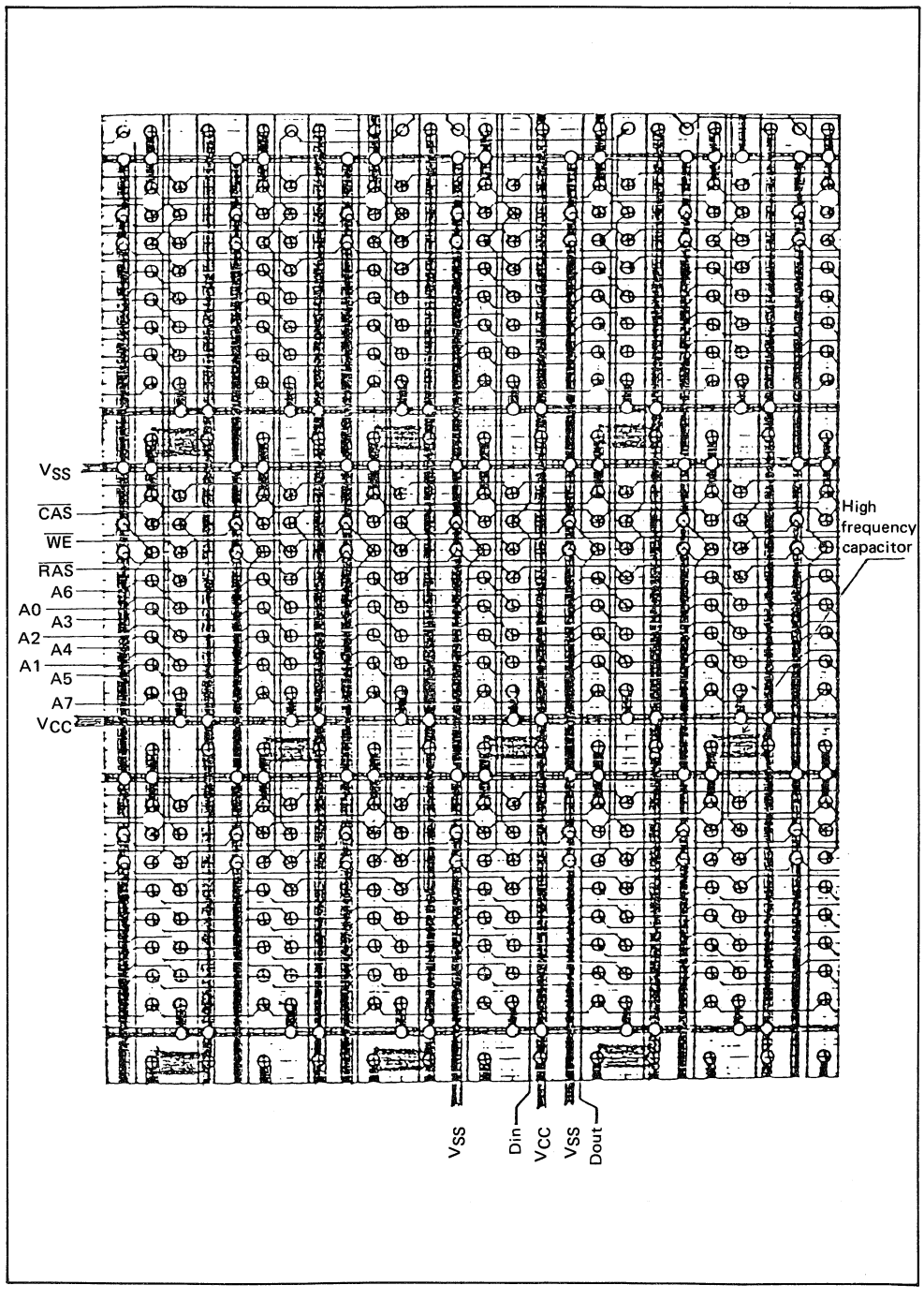
In designing a circuit board to achieve stable system operation, however, considerations must be given to the specification values and margins against the specification values, pertaining to the points shown in the following table. Factors that will affect the stable system operation are power, temperature, aging, clock skew, uneven operation of peripheral ICs, and so forth.

Point to be noted	Actual item to be considered	Reason
Power	○ Currents (Icc1, Icc3, and Icc4) at the operating time and current (Icc2) at the standby time	The power system must be noted. (example: with battery backup)
	○ Current waveform (especially the peak current value)	The noise margin must be strict for memories with large peak current.
Timing margin	○ Address setup (t_{ASR}, t_{ASC}) and hold (t_{RAH}, t_{CAH}) timing	In system designing, these timing pulses are directly related to the access time.
	○ Data setup (t_{DS}) timing and write pulse width (t_{WP})	These timing pulses are related to the cycle time in writing.
	Voltage, temperature, and dependability of each timing (especially the t_{REF} and t_{RAC})	The temperature inclination must be little for the timing pulses t_{REF} and t_{RAC}.
Voltage margin	It is impossible to achieve the ideal voltage status when used within a system.	A sufficient voltage margin must be provided under consideration of various factors which will affect the system operation stability.

Attached drawing 1
Frequency characteristics of capacitor and Q/PAC

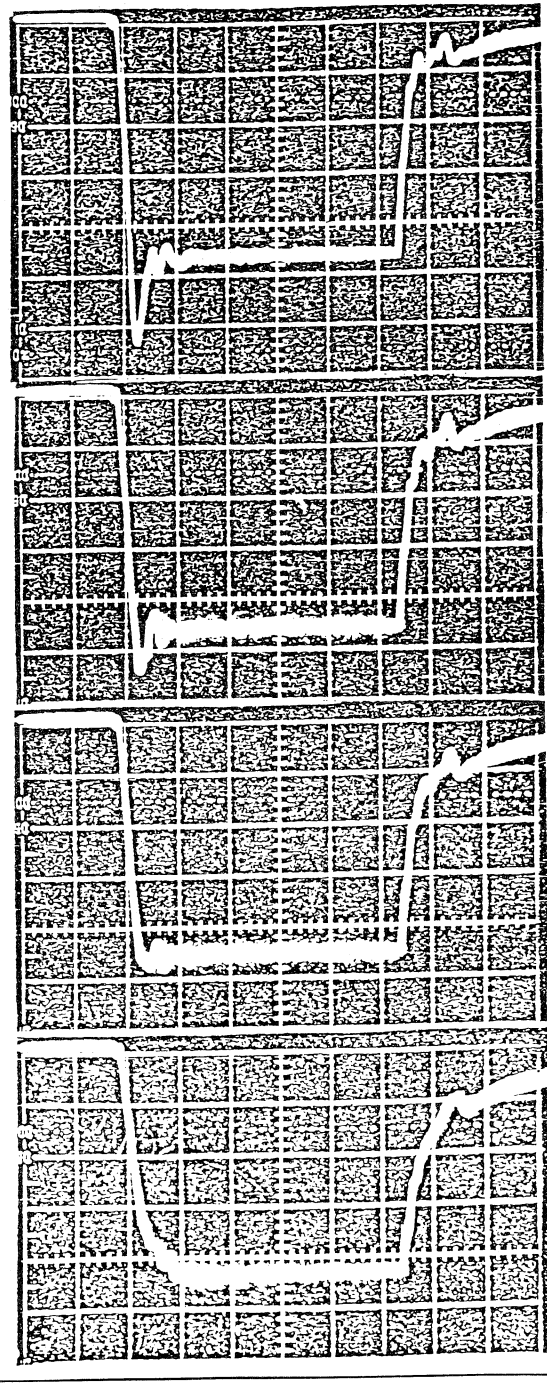


Attached drawing 2
Two layer board circuit pattern example



Attached drawing 3
Input waveform example

Horizontal: 50 ns/div
Vertical: 1 volt/div



10

CMOS RAM BATTERY BACK-UP

A practical example of formation of non-volatile data by CMOS static RAM battery back-up is outlined below.

1. System power and battery switching circuit

The simplest RAM power supply (CMOS Vcc) is outlined in Fig. 1. In this case, the CMOS Vcc for normal operation is kept at a voltage 0.7V below the system voltage by the voltage drop across a diode (forward direction).

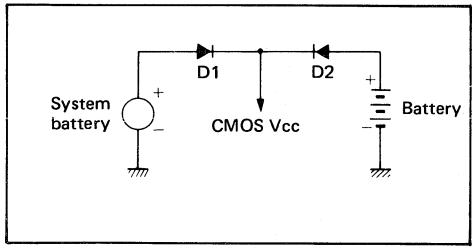


Fig. 1

Fig. 2 is an example of use of a chargeable Ni-Ca battery as the back-up battery. While the system power is being employed, the Ni-Ca battery is gradually charged up via Rc. As in Fig. 1, the diode voltage drop also poses a problem in this circuit.

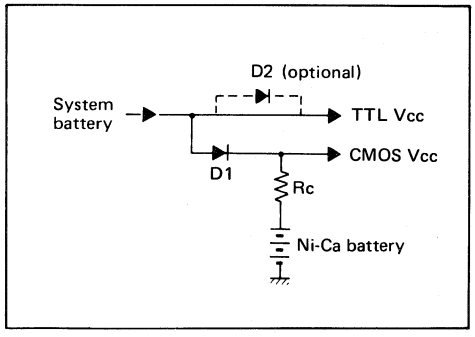


Fig. 2

The conditions for formation of non-volatile data (data retention) by battery back-up are listed below.

(1) The input signal H level must not exceed Vcc + 0.3V when the CMOS RAM Vcc power voltage is dropped.

(2) $\overline{CE}$ (or $\overline{CS}$) must maintain CMOS Vcc "H" level.

(3) In order to minimize power consumption, $\overline{WE}$, AD, DIN (or I/O) must be set to GND level or to the same "H" level as CMOS Vcc. (This is not necessary, however, for CMOS RAMs with chip select floating capability).

Note: $\overline{CS}$ floating capability
Power down possible irrespective of other input levels when memory has not been selected (i.e. when $\overline{CS}$ = H).

Consequently, if the TTL Vcc level is greater than the CMOS RAM supply voltage, and the RAM driver is at the TTL Vcc level, the CMOS RAM input voltage will exceed CMOS Vcc + 0.3V (a situation which must be avoided). Therefore, in order to reduce the voltage difference between CMOS Vcc and TTL Vcc with the battery voltage set to at least 4.5V or 4.75V (due to the RAM operating supply voltage range), the D2 diode may be added to abtain a system voltage level at least 0.7V above 4.5 ~ 4.75V (which will keep CMOS Vcc and TTL Vcc within the respective CMOS and TTL operating supply voltage ranges).
To cope with (1) and (3), a CMOS driver which will also operate at a low voltage Vcc during data hold may be employed, or else, the open collector and open drain buffer may be pulled up to CMOS Vcc in order to drive the RAM.
A control circuit for coping with (2) when an abnormal system power supply is detected is also required.

2. Switching Circuit Modifications

Modification of the diode switching circuit can employ PNP transistors. Voltage drops by PNP transistor V_{CE} are smaller by about 0.2V, and this can lead to the generation of a system "power fail" signal.

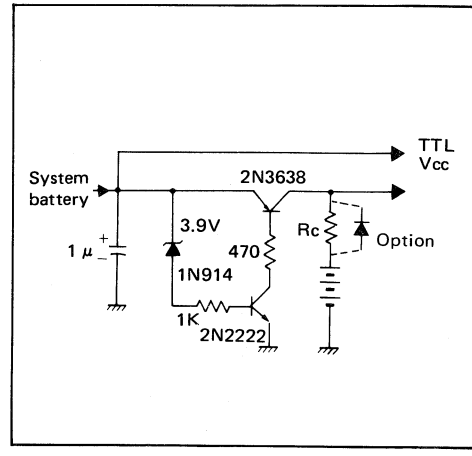
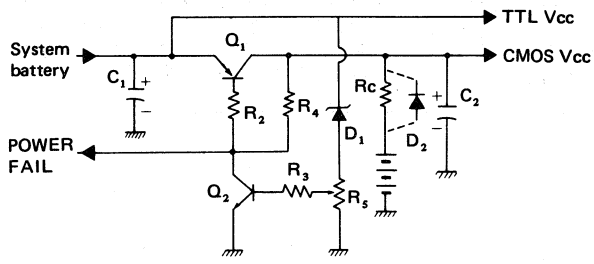


Fig. 3

Fig. 3 outlines a switching circuit employing a PNP transistor. The Rc used when a chargeable battery is employed is replaced by a diode when a non-chargeable battery is used. In this case, switching occurs at the zener diode voltage, so "power fail" must be detected by another circuit, and $\overline{CE}$ set to CMOS Vcc "high" level.

10

Figs. 4 and 5 are examples of circuits capable of generating a POWER FAIL output signal. In these circuits, the C2 capacitance must be rather large, the important point being the need for a smooth gradual change in CMOS Vcc when the system power is cut. See next page for further details.



Q_1 : 2N2907 or 2SA495
Q_2 : 2N2222 or 2SC372
R_3 : 1K R2 : 100
R_5 : 500 R4 : 47K
D_1 : 3.6V Rc : 200
Ni-Cad : 3.6V (70mAH)

Fig. 4

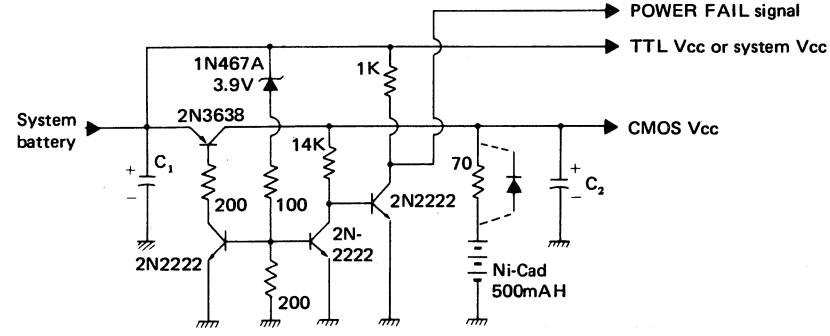


Fig. 5

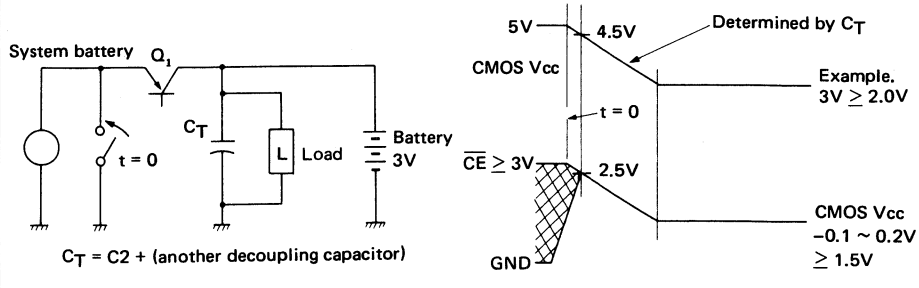


Fig. 6

3. Data Retention Mode

The RAM driver (peripheral circuit) is determined according to conditions (1) and (3) required for data retention. In Oki Electric CMOS RAMs, the power voltage during data retention is kept at a minimum of 2.0V. The $\overline{CE}$ (or $\overline{CS}$) voltage at this time has to be kept at about Vcc −0.2V. And as was mentioned earlier, the CMOS Vcc must drop smoothly when the system power is cut until it reaches the power voltage for data retention (practically equivalent to the battery voltage, or else reduced by the diode voltage drop). And although $\overline{CE}$ traces the slope of CMOS Vcc reduction at this time, a smooth change in $\overline{CE}$ is also a necessary condition for actual circuits.

(4) When switching to retention mode, or from retention mode to operation mode, $\overline{CE}$ must exhibit a smooth change. If noise is generated in $\overline{CE}$ in this case, the data will be subject to rewriting.

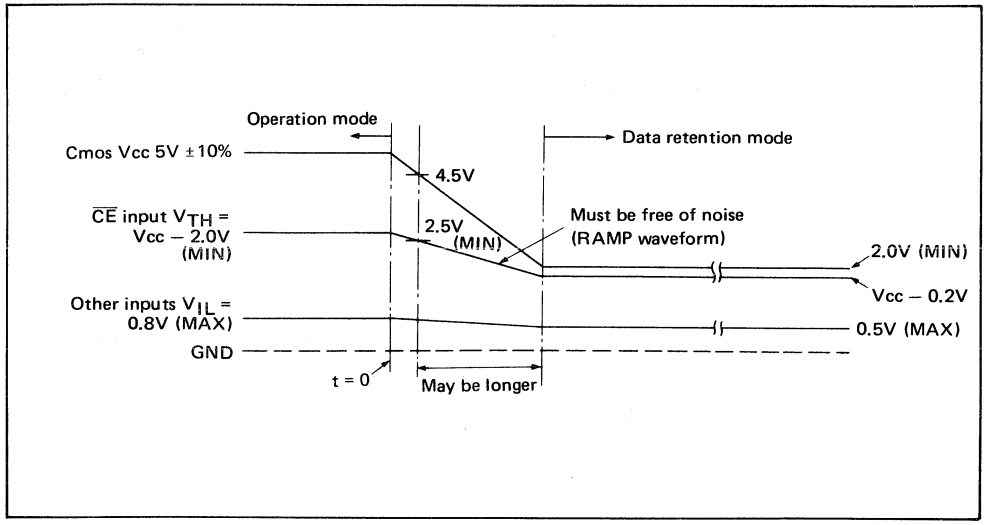


Fig. 7

(5) When switching to operation mode, commence operation after elapse of t_{RC} (read cycle time) following Vcc reaching the operating power voltage range.

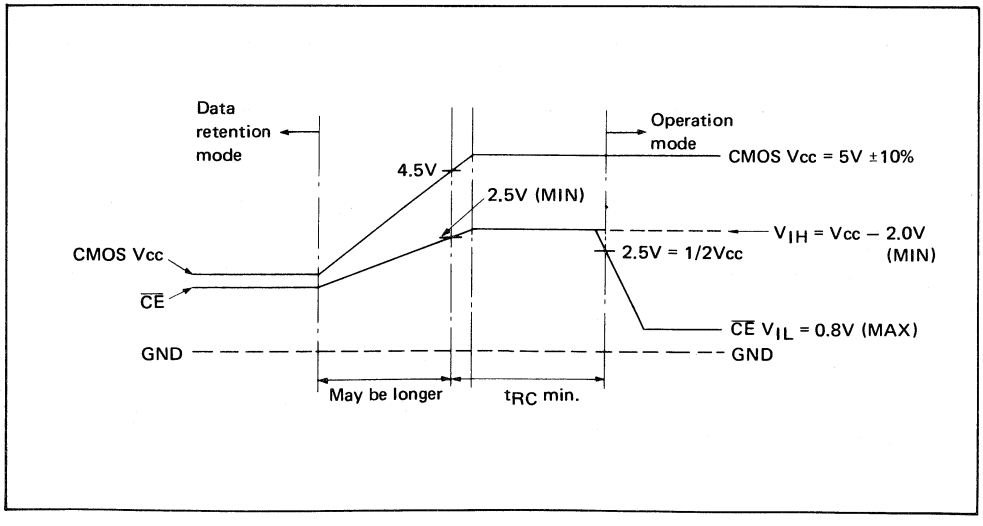


Fig. 8

4. Interfacing

A) TTL Interface

In the case of CMOS RAM drive by TTL, use an open-collector type TTL according to conditions (1) and (3).

When the system power line (i.e. TTL Vcc) is cut, the open-collector TTL Q2 in Fig. 9 is turned off, followed by Q1 also being turned off, resulting in the CMOS RAM input being pulled-up to CMOS Vcc.

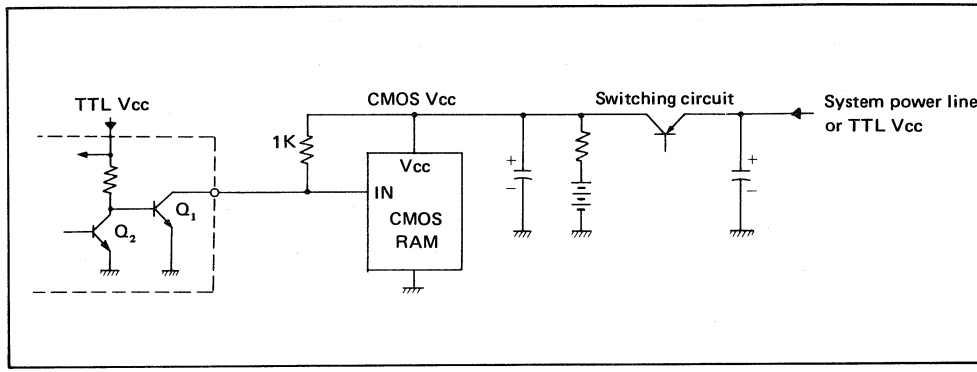


Fig. 9

When the power line voltage in LS type TTL is dropped to ground, the output is also dropped to ground, thereby making the pull-up resistors for address line buffers etc no longer necessary. In this case, however, it will not be possible to employ this as a control line buffer which must be switched to "high" during $\overline{CE}$ (or $\overline{CS}$) data retention.

(6) In order to minimize the consumption current during data retention, all inputs except $\overline{CE}$ (or $\overline{CS}$, this being designated as either "high" or "low") must be maintained at either GND or CMOS Vcc. (This does not apply, however, for CMOS RAMs equipped with $\overline{CS}$ floating function).

B) CMOS Interface

In systems where the CMOS RAM is driven by CMOS buffer, operation must be at the data retention power voltage, and the corresponding output voltage must satisfy the requirements indicated in Figs. 7 and 8.

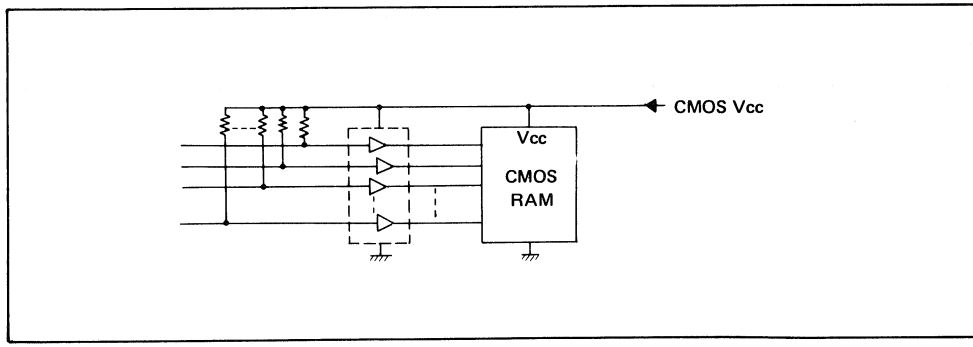


Fig. 10

5. Miscellaneous

In order to further reduce power consumption during data retention by even a small margin, the use of a MOS FET as the transistor generating the POWER FAIL output signal is recommended. This is in order to prevent flow of current from the 14kΩ resistor.

MASK ROM KANJI GENERATION MEMORY DESCRIPTION

1. KANJI GENERATION MEMORIES

	IC models	Number of codes	Character storing capacity	Config-uration	Character style	Bit capacity	Access time
High speed memories	MSM38256-19 MSM38256-22	4	JIS standard No. 1 3418 characters	15 x 16	Gothic style	25yK bits	250ns max
	MSM38256-32 MSM38256-35	4	JIS standard No. 2 3418 characters	15 x 16	Gothic style	256K bits	250ns max
	MSM38256-10 MSM38256-18	9	JIS standard No. 1 3418 characters	24 x 24	Ming style	256K bits	250ns max
	MSM38256-38 MSM38256-46	9	JIS standard No. 2 3418 characters	24 x 24	Ming style	256K bits	250ns max
Middle speed memories	MSM38128-00 MSM38128-17	18	JIS standard No. 1 3418 characters	24 x 24	Ming style	128K bits	450ns max
	MSM38128-18 MSM38128-27	10	JIS standard No. 1 3418 characters	16 x 18	Gothic style	128K bits	450ns max
Low speed memories	MSM28101A	1	JIS standard No. 1 3418 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)
	MSM28201A	1	JIS standard No. 2 3384 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)

2. MSM38256 SERIES

2-1 15 x 16 Font

(1) Model names

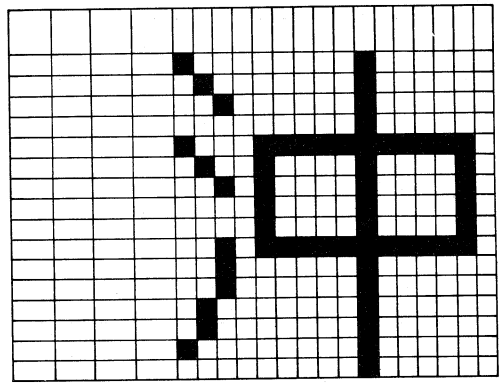
MSM38256-19~22 (four codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters)

MSM38256-32~35 (four codes); JIS standard No. 2 (3,384 characters)

These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals are active low.

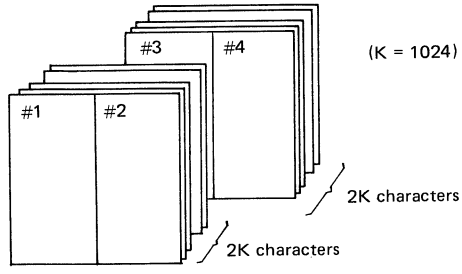
(2) Split character patterns, and their storage

• Split character patterns



- The character patterns are standard OKI character patterns.
- Each character consists of two chips.
- Character data is generated at high level, and background data is generated at low level.
- Character data is stored in a 16 x 16 dot pattern area, left-justified.

• Storage



- Each group of four chips forms one set to store about 4K characters.

	#1	#2	#3	#4
JIS standard No. 1	MSM38256-19	MSM38256-20	MSM38256-21	MSM38256-22
JIS standard No. 2	MSM38256-32	MSM38256-33	MSM38256-35	

(3) Address code conversions

The following address code conversions are required to access character patterns with the JIS C6226 kanji code:

(i) Converting JIS standards Nos. 1 and 2 (byte 1 = 50H ~ 6FH area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

⇩

	Byte 1								Byte 2							
ROM address				A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Conversion address				X_5	X_4	X_3	X_2	X_1		Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

(ii) Converting non-kanji and JIS standard No. 2 (byte 1 = 70H ~ 74H)

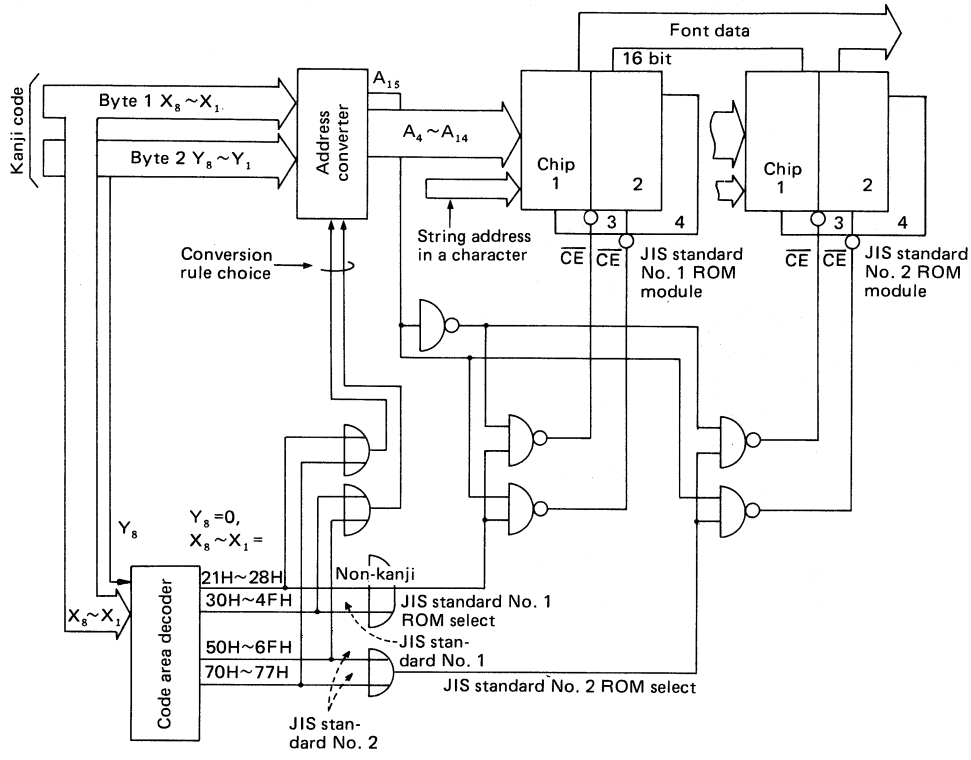
	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

⇩

	Byte 1								Byte 2							
ROM address				A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Conversion address				Y_7	Y_6	X_3	X_2	X_1		0	0	Y_5	Y_4	Y_3	Y_2	Y_1

* Use A_{15} as a CE control signal because it is not supported as a ROM address. (For further details, see the circuit example.)

15 x 16 font circuit configuration example



2-1 24 x 24 Font

(1) Model names

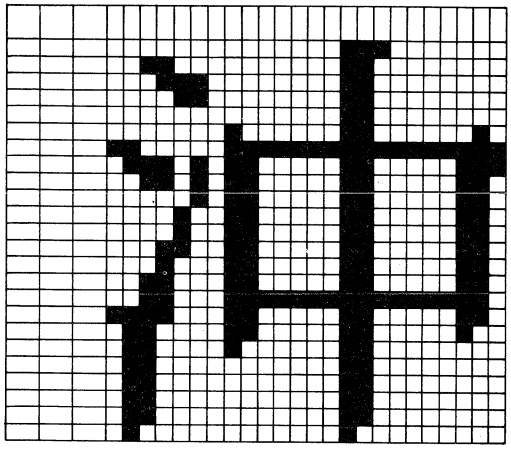
MSM38256-10~18 (nine codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters) + Half-size characters (159).

MSM38256-38~46; JIS standard No. 2 (3,384 characters)

These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals are active low.

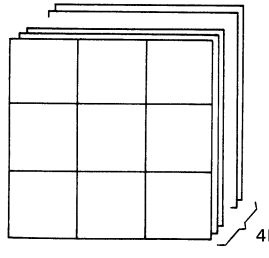
(2) Split character patterns, and their storage

• Split character patterns



- The character patterns are standard JIS character patterns.
- Each character consists of nine chips.
- Character data is generated at high level, and background data is generated at low level.

• Storage



	JIS standard No. 1	JIS standard No. 2
#1	MSM38256-10	MSM38256-38
#2	MSM38256-11	MSM38256-39
#3	MSM38256-12	MSM38256-40
#4	MSM38256-13	MSM38256-41
#5	MSM38256-14	MSM38256-42
#6	MSM38256-15	MSM38256-43
#7	MSM38256-16	MSM38256-44
#8	MSM38256-17	MSM38256-45
#9	MSM38256-18	MSM38256-46

(3) Address code conversions

The following address code conversions are required to access character patterns with the JIS C6226 and C6229 kanji code:

(i) Converting JIS standards Nos. 1 and 2 (byte 1 = 50H~6FH area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				X_5	X_4	X_3	X_2	X_1		Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

(ii) Converting non-kanji and JIS standard No. 2 (byte 1 = 70H~74H area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

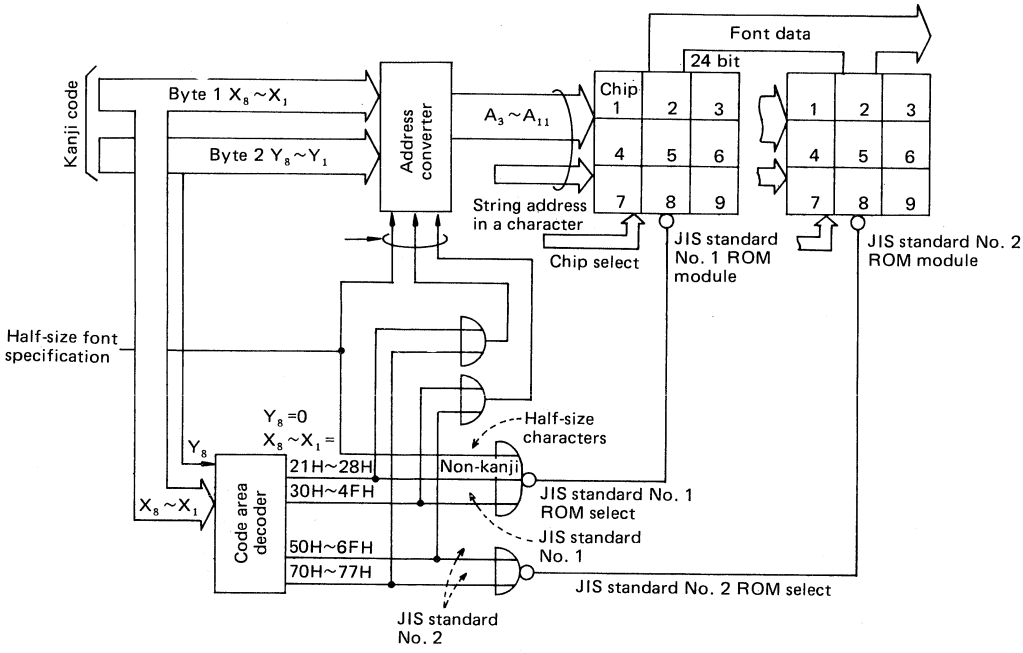
	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				Y_7	Y_6	X_3	X_2	X_1		0	0	Y_5	Y_4	Y_3	Y_2	Y_1

(iii) Converting half-size characters (C6220 code)

C6220	Z_8	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1

	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				0	0	Z_8	Z_7	Z_6		0	0	Z_5	Z_4	Z_3	Z_2	Z_1

(4) 24 x 24 font circuit configuration example



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